Decision-Directed Phase Noise Compensation for Millimeter-Wave Single Carrier Transmission Systems with Frequency-Domain Equalization

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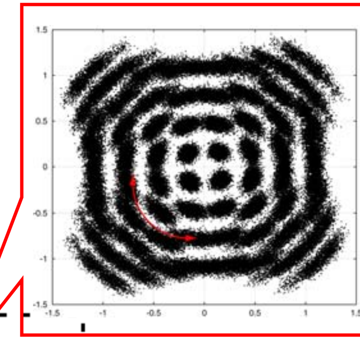
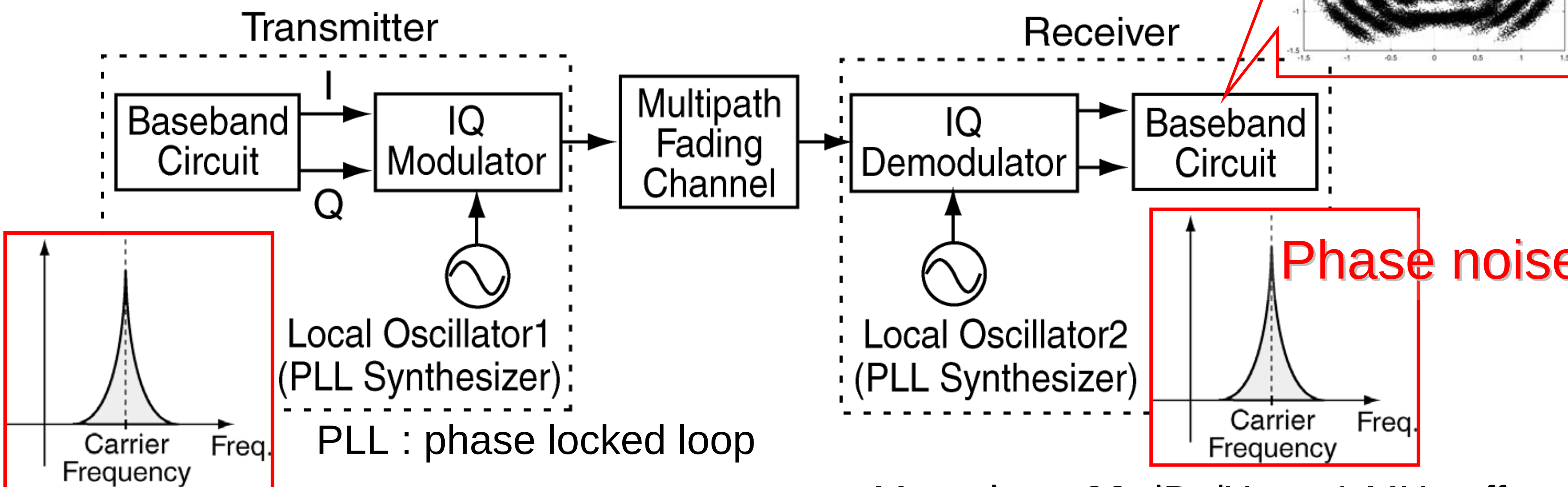
Research of Suzuki-Fukawa Lab. for Millimeter-Wave Project

Research Topic

60-GHz transmission by Si-CMOS IC





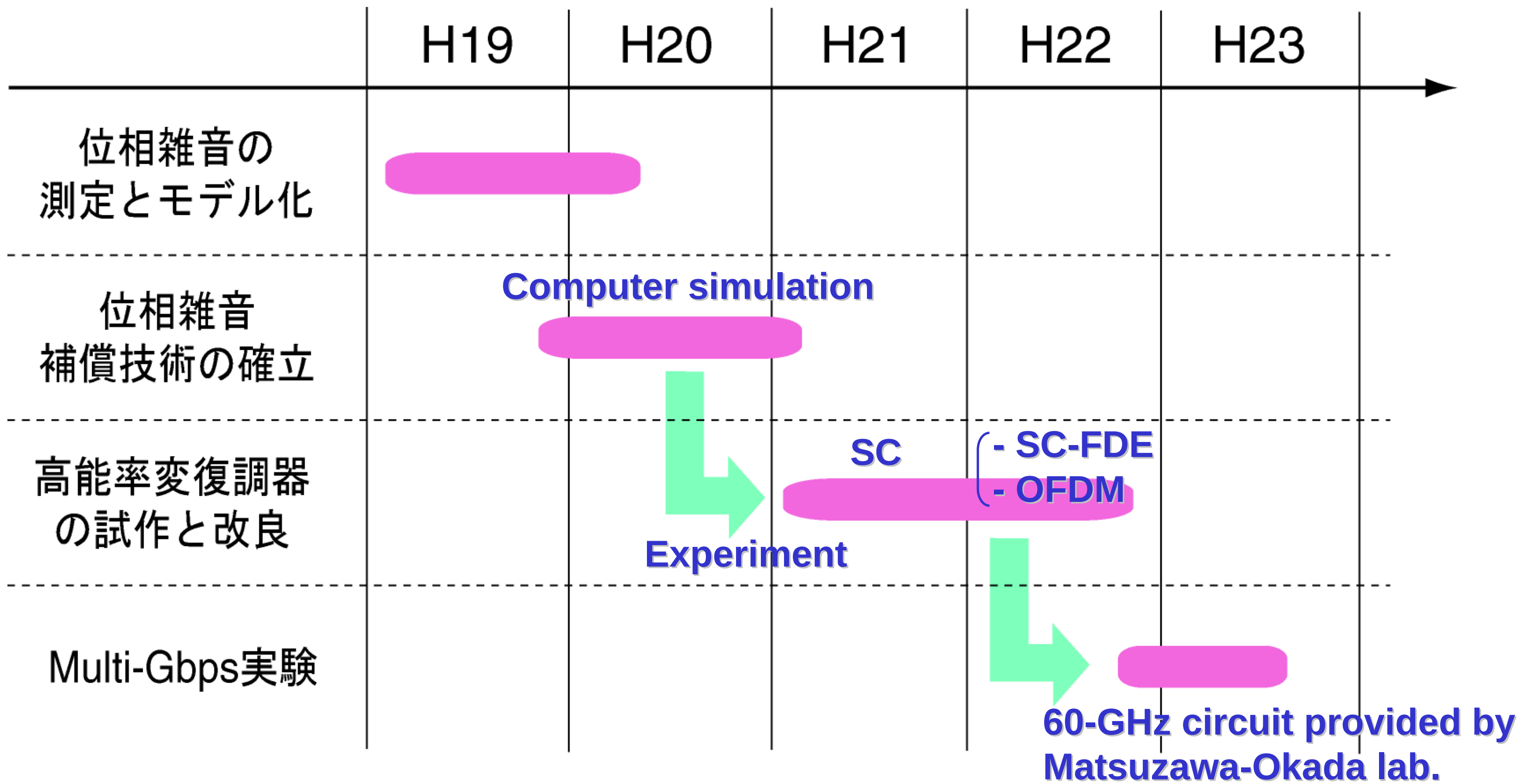
More than -90 dBc/Hz at 1 MHz offset

Overcome of relatively large phase noise in PLL

Establishment of phase noise compensation method :

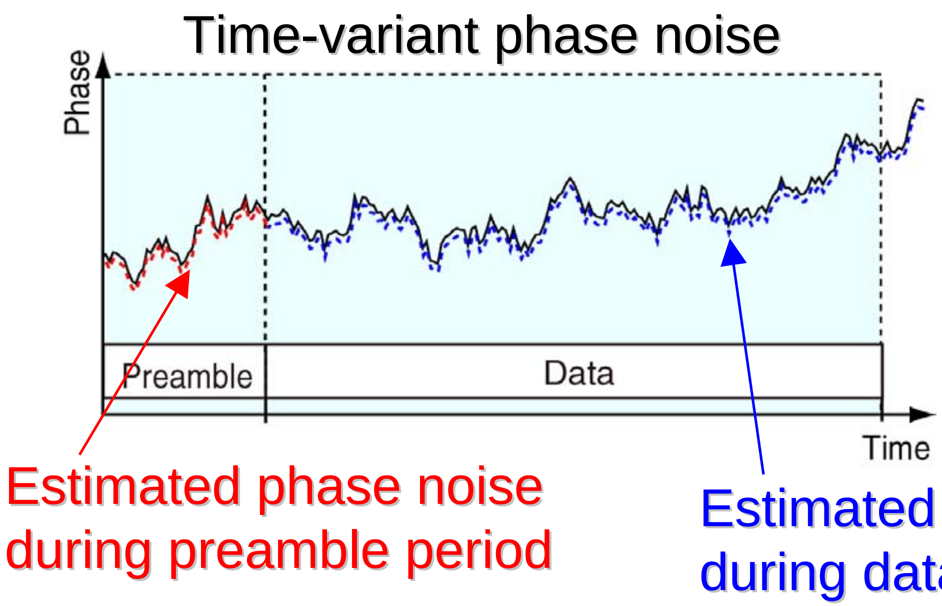
1. Measurement of phase noise and modeling
2. Phase noise compensation by digital signal processing
3. Hardware verification of the proposed compensation method

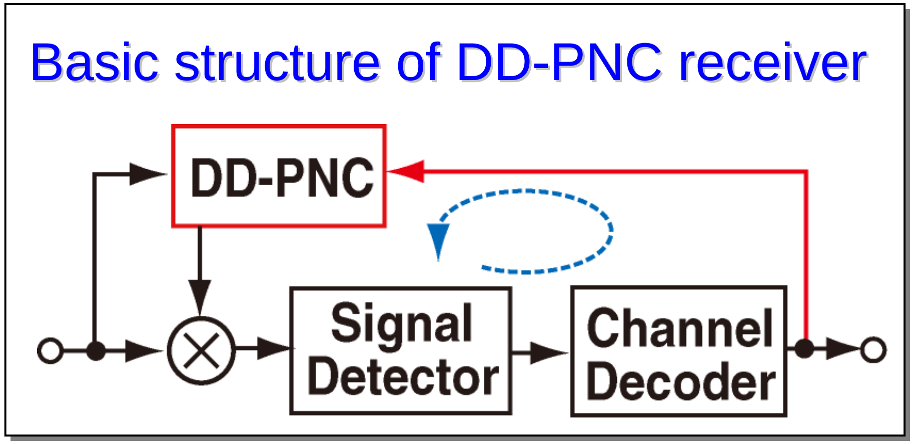
Schedule of This Research



Phase Noise Compensation

Decision-directed phase noise compensation (DD-PNC)



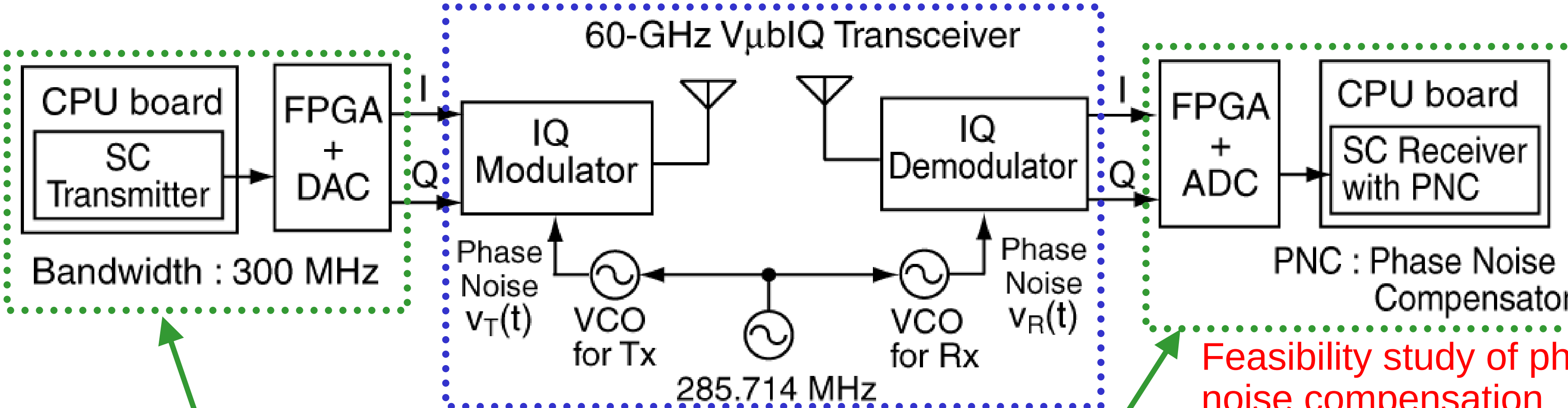


Research results:

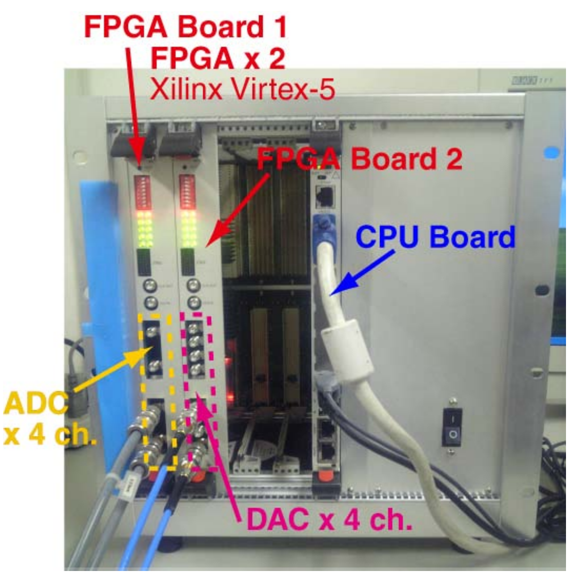
- Proposal of DD-PNC receiver
  - Orthogonal frequency division multiplexing (OFDM)
  - Single-carrier with frequency domain equalization (SC-FDE)
- Verification by computer simulations and experiments

60-GHz Experimental System

Millimeter-Wave Single Carrier (SC) Transmission



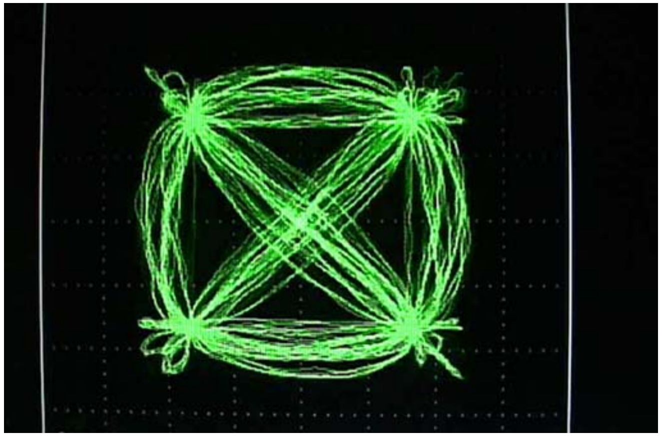
Feasibility study of phase noise compensation method by experiment



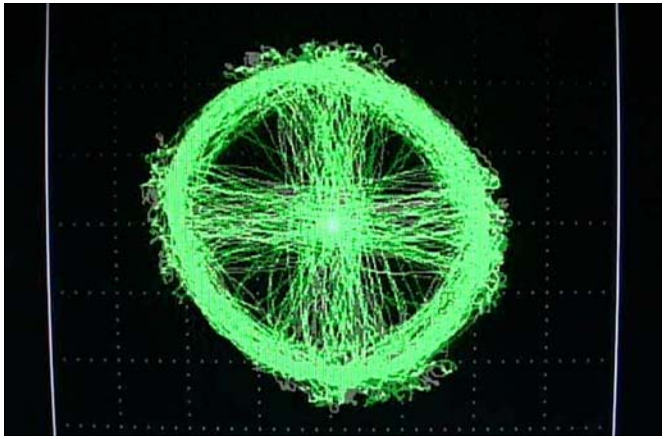
CPU board performs transmit and reception processes.

60-GHz Transceiver

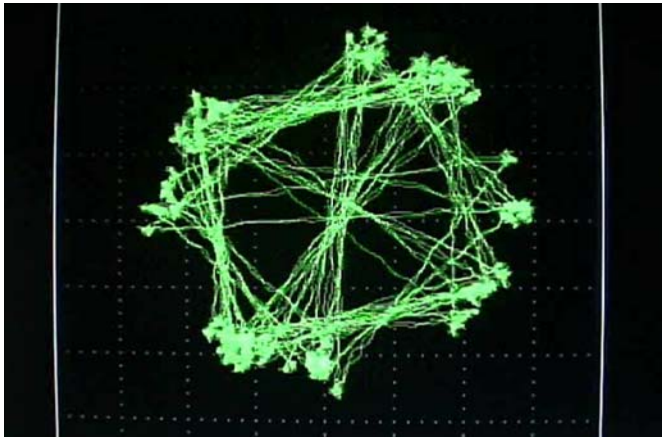
Effect of Phase Noise Compensation



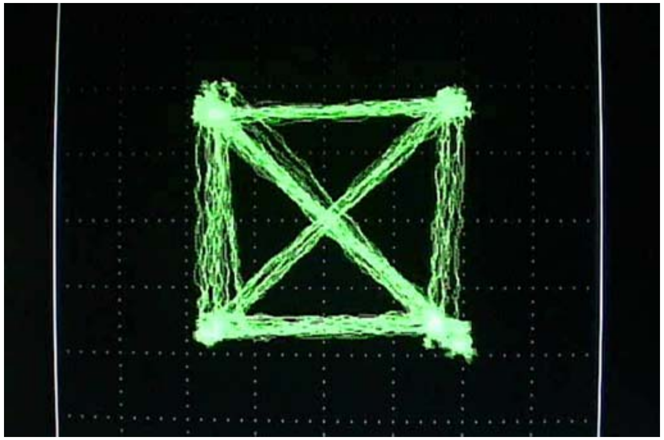
Transmitted signal



Received signal



Output of coherent detector
without DD-PNC



Output of coherent detector
with DD-PNC

Phase Noise Compensation for SC-FDE

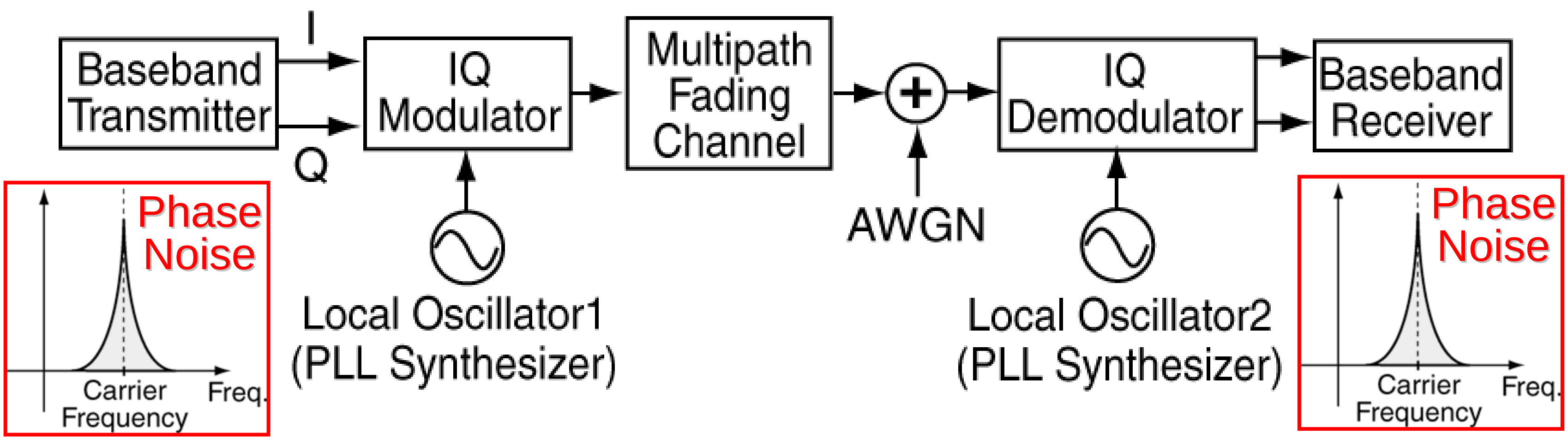
Outline

- Background
- Effect of phase noise
- Proposed receiver with decision-directed phase noise compensation
- Simulation results
- Conclusion

Background

- 60-GHz WPAN standard in IEEE802.15.3c:
  - SC-FDE (single carrier with frequency-domain equalization)
  - OFDM (orthogonal frequency division multiplexing)
- 60-GHz single-chip transceivers based on Si-CMOS IC:
  - Lower power consumption and cost

60-GHz transmission system

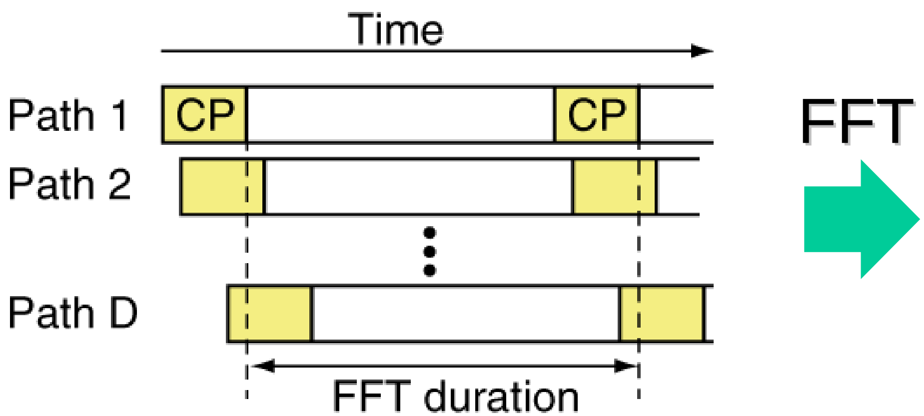


In WPAN systems, the relatively large phase noise occurs, and degrades transmission performances of SC-FDE and OFDM.

SC-FDE and OFDM

1. Insertion of cyclic prefix (CP)

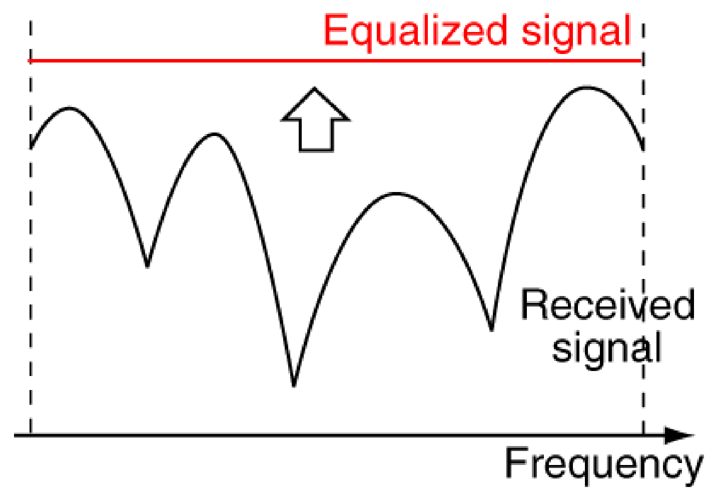
Received signal in time domain



Periodic function in FFT duration

2. FDE :

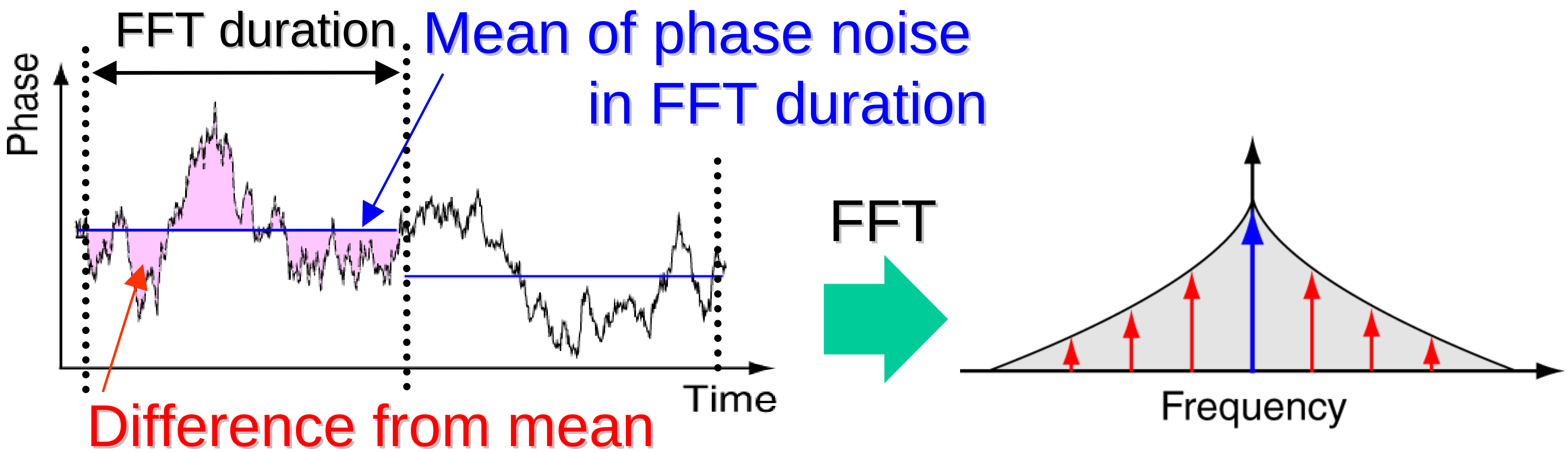
Received signal is divided by channel frequency response.



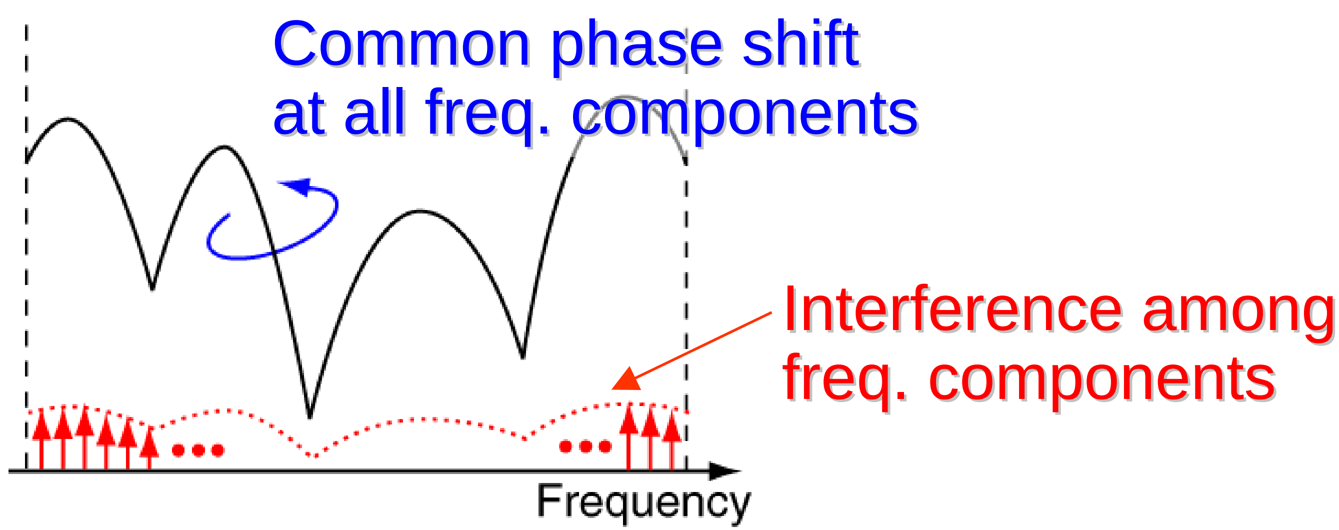
- Both OFDM and SC-FDE receivers employ FDE process to combat multipath delay.
- FDE process requires that time-domain received signal in FFT duration is time-invariant.

Effect of Phase Noise

- **Phase noise**



- **Post-FFT received signal with phase noise**



Phase Noise Compensation for SC-FDE

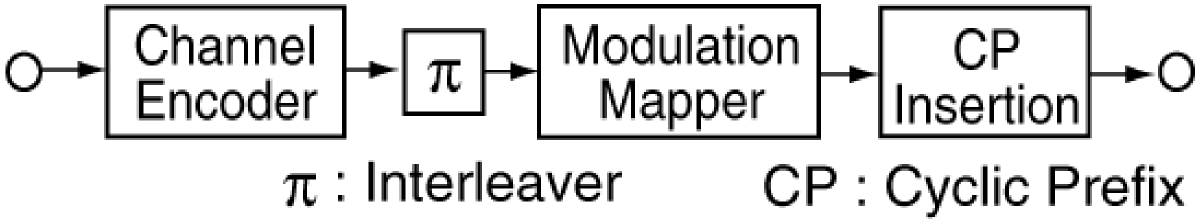
- **OFDM transmission**
  - More sensitive to the phase noise than the normal SC transmission
  - Decision-directed phase noise compensation (DD-PNC) has been proposed as the effective solution

- **SC-FDE transmission**
  - Similarly to OFDM, severe degradation due to the phase noise
  - Conventional method for SC: combination of DFE and the phase noise compensation, which cannot be applied to SC-FDE
  - SC-FDE cannot easily compensate for the phase noise before FDE
  - Effective phase noise compensation has not been proposed

⇒ We propose a SC-FDE receiver employing DD-PNC

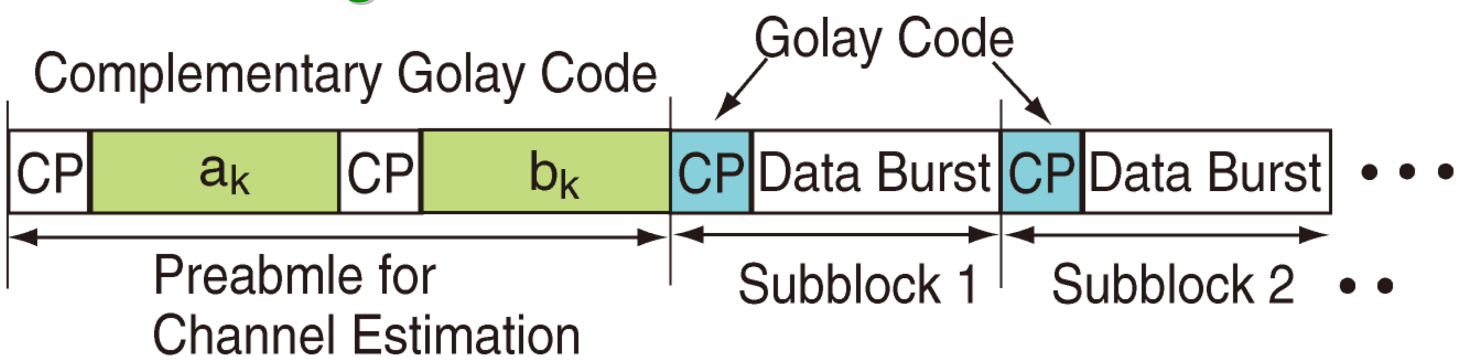
SC-FDE Transmitter

- **Block diagram of SC-FDE transmitter**



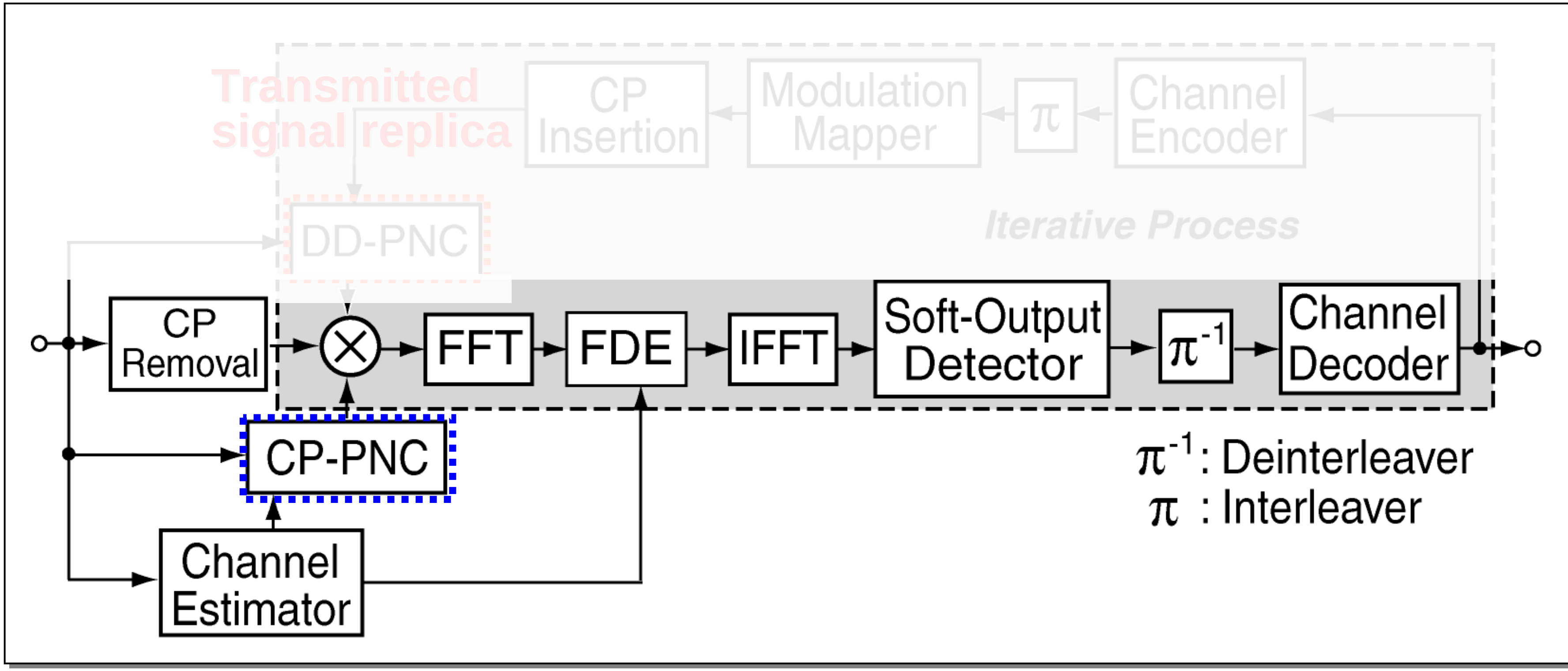
- CP is inserted for FDE

- **Packet Configuration**



- Complementary Golay code is CAZAC (constant amplitude zero autocorrelation) sequence
- 1 subblock consists of CP and data symbols
- Another Golay code is used as CP, which is known to the receiver

SC-FDE Receiver with DD-PNC



- Initial process:
  CP-PNC (CP-based phase noise compensation)
- Iterative process:
  DD-PNC (decision-directed phase noise compensation)

Channel Estimation

- **Received signal at the *k*-th symbol of the *i*-th subblock:**

$$r_{i,k} = \boxed{e^{j\phi_{i,k}}} \sum_{d=0}^{D-1} \underbrace{h_d}_{\text{Complex amplitude of the } d\text{-th path}} s_{i,k-d} + n_{i,k}$$

Transmitted signal: $s_{i,k-d}$

$n_{i,k}$: noise

Phase noise: $\Phi_{i,k} = \underbrace{\bar{\Phi}_i}_{\text{Mean}} + \underbrace{\psi_{i,k}}_{\text{Difference from mean}}$

- **Estimated channel impulse response:**

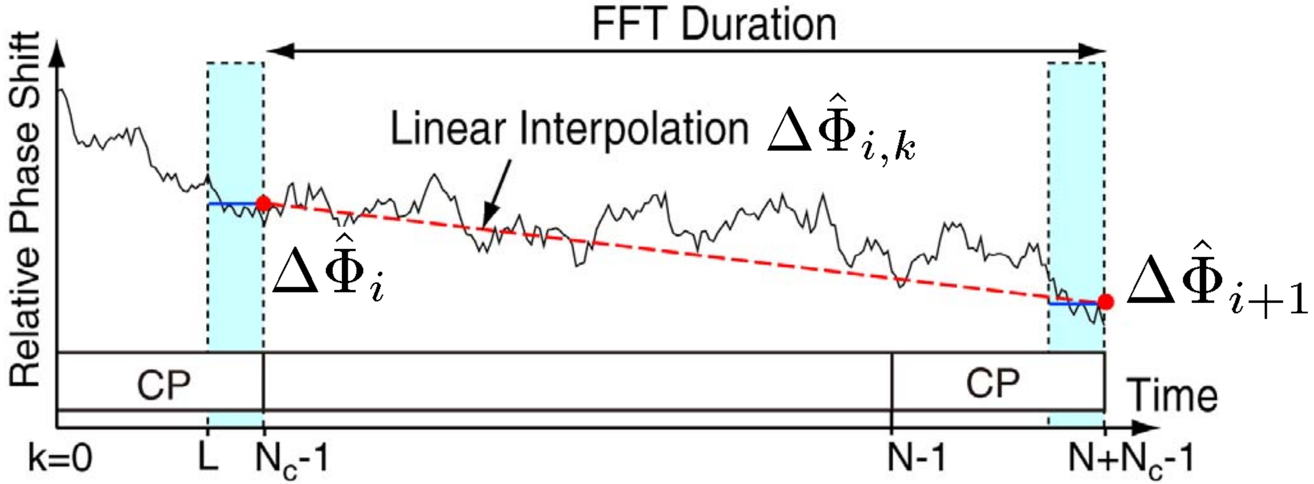
Crosscorrelation between the received signal and the preamble of the complementary Golay code

$$g_{i_p,l} = h_l \underbrace{\bar{\Phi}_{i_p}}_{\text{Mean of phase noise during preamble}} + \nu_{i_p,l}$$

i_p : subblock number of preamble

$\nu_{i_p,l}$: estimation error

CP-PNC



- **CP-PNC estimates relative phase noise during CP of the *i*-th subblock:**

$$\Delta\hat{\Phi}_i = \frac{\bar{\Phi}_i}{\bar{\Phi}_{i_p}} = \frac{1}{N_c - L} \sum_{k'=-N_c+L}^{-1} \frac{r_{i,k'}}{\hat{r}_{i,k'}}$$

Received signal replica :

$$\hat{r}_{i,k} = \sum_{l=0}^{L} g_{i_p,l}\, c_{k-l}$$

c_k : known CP

- **Relative phase noise $\Delta\hat{\Phi}_{i,k}$ during data symbols is estimated by linearly interpolating $\Delta\hat{\Phi}_i$ and $\Delta\hat{\Phi}_{i+1}$**

- **CP-PNC removes the estimate as $r'_{i,k} = r_{i,k}\ \Delta\hat{\Phi}^*_{i,k}$**

DD-PNC

- **DD-PNC generates the received signal replica during data symbols by using a transmitted signal replica $\hat{s}_{i,k}$ as**

$$\hat{r}_{i,k} = \sum_{l=0}^{L} g_{i_p,l} \, \underline{\hat{s}_{i,k-l}}$$

$\hat{s}_{i,k}$ is generated from decoded bits

- **It estimates the relative phase noise by one-tap LMS (least-mean-square) algorithm:**

$$e_{i,k} = r_{i,k} - w_{i,k}^{*} \hat{r}_{i,k}$$

$$w_{i,k+1} = w_{i,k} + \underbrace{\mu_{\phi}}_{\text{Step-size parameter}} \hat{r}_{i,k} \, e_{i,k}^{*}$$

$w_{i,k}^{*}$: an estimate of relative phase noise $\Delta\hat{\Phi}_{i,k}$

- **DD-PNC performs smoothing for the estimates by backward exponential weighting as**

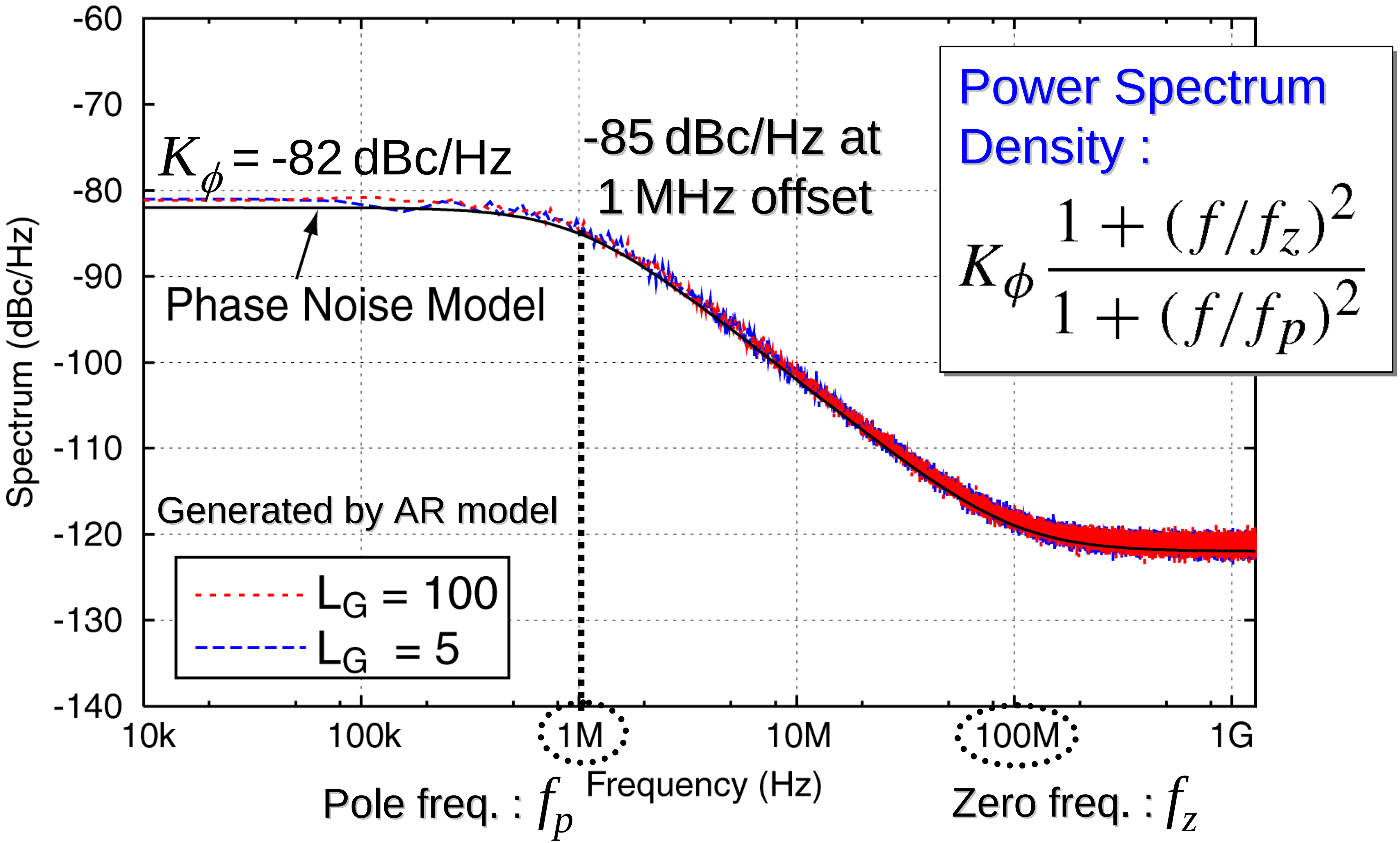
$$\Delta\tilde{\Phi}_{i,k} = \mu_{\phi} \, w_{i,k}^{*} + (1 - \mu_{\phi}) \, \Delta\tilde{\Phi}_{i,k+1}$$

Simulation Conditions

Parameters of SC-FDE basically follow 60-GHz WPAN.

Modulation	SC-FDE / 64QAM
Sampling rate	1.73 GHz
No. of subblocks	preamble : 4, data : 14
No. of FFT points N	256
No. of symbols in subblock	CP (N_c) : 16, data : 240
Channel coding	convolutional code ($R = 3/4$)
Maximum bit-rate	7.29 Gbps ($R = 3/4$, 64QAM)
Channel decoding	soft decision Viterbi decoding
No. of iterations	5 (except the initial process)
Step-size parameter μ_ϕ	0.03 – 0.13
Channel model	Nakagami-Rice fading LOS : $K = 10$ dB NLOS : 5-path with equal power

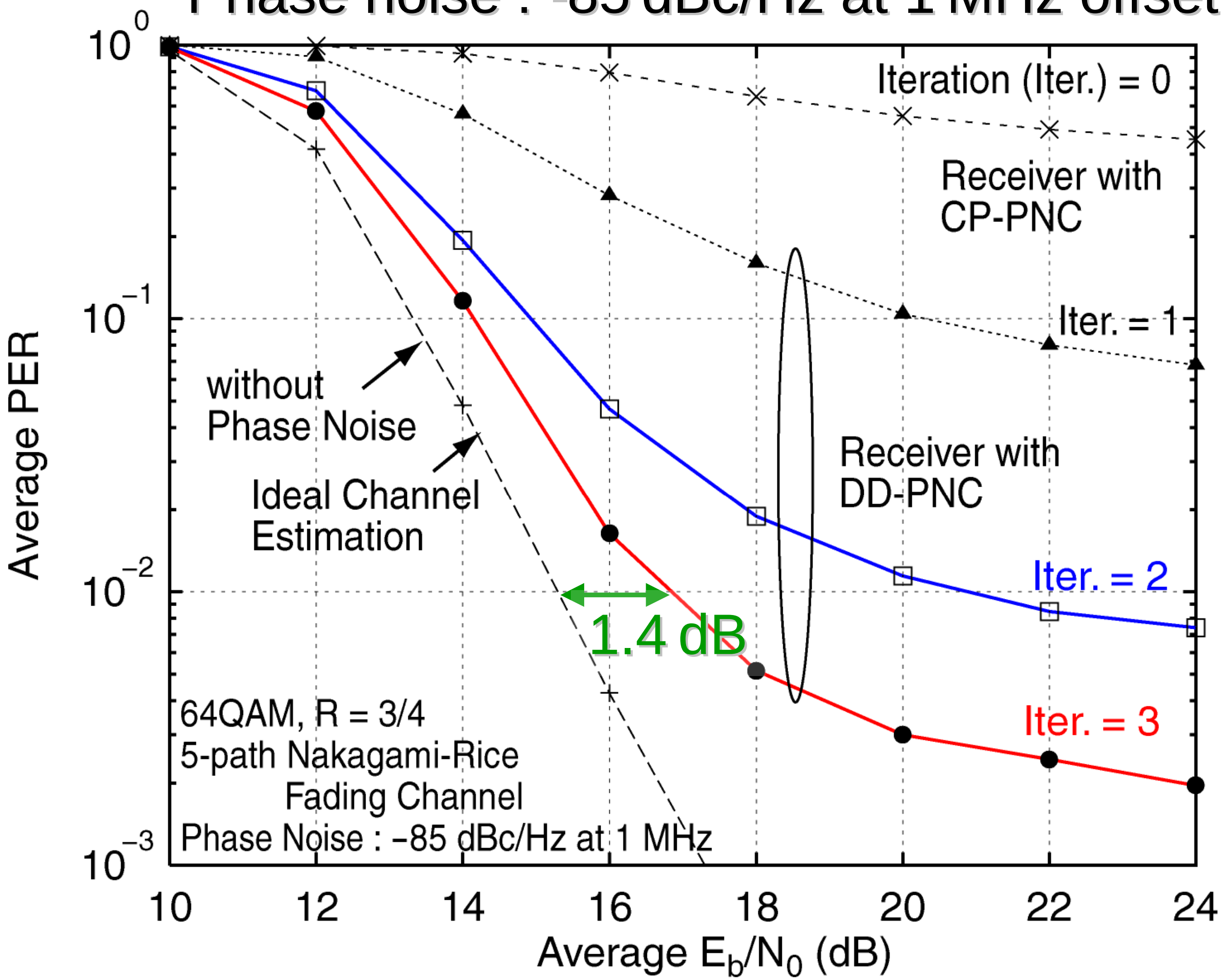
Phase Noise Model



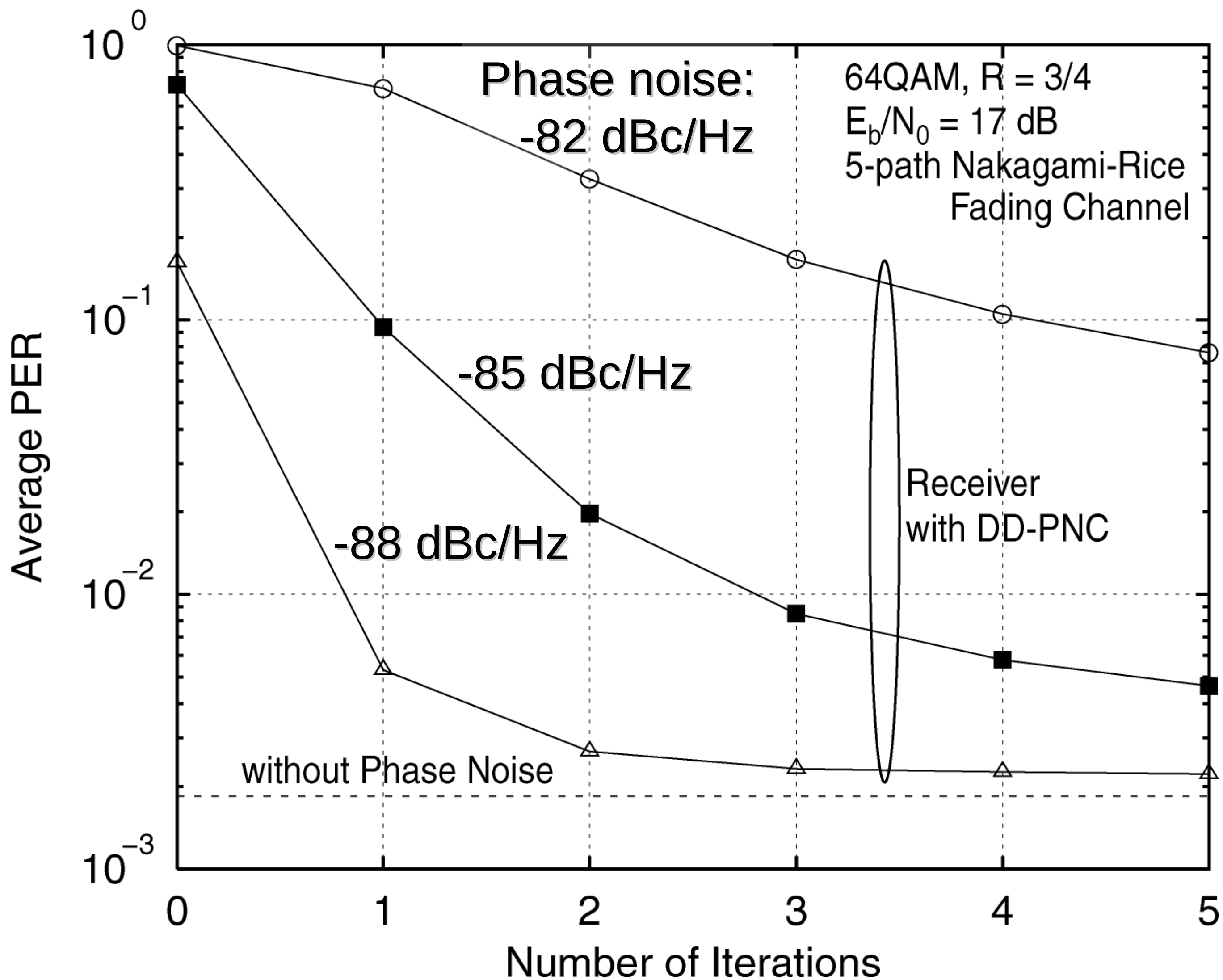
K_ϕ was changed as a parameter.

PER Performance

Phase noise : -85 dBc/Hz at 1 MHz offset



Iteration Performance



Conclusion

- We have proposed the SC-FDE receiver employing DD-PNC in the millimeter-wave SC transmission:

  - The receiver iterates DD-PNC and FDE by exploiting the output of the channel decoder
  - DD-PNC recursively estimates phase noise by one-tap LMS algorithm with smoothing

- Computer simulations have demonstrated :

  In the 64QAM modulation with R = 3/4,

  - When phase noise is -85 dBc/Hz, the receiver with 3 iterations can reduce E_b/N_0 degradation from ideal performance to 1.4 dB at PER = 10^{-2}.
  - When phase noise is -88 and -85 dBc/Hz, 1 and 3 iterations can achieve PER = 10^{-2} at E_b/N_0 = 17 dB, respectively.