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TPA6120A2 High Fidelity Headphone Amplifier

1 Features

- SNR of 128dB A-Weighted.
- THD of 112.5dB
- Current-Feedback Architecture
- Output Voltage Noise of 0.9µV_{rms} at Gain = 1V/V (16Ω Load)
- Power Supply Range: ±5V to ±15V
- 1300V/µs Slew Rate
- Can be configured for Single Ended or Differential Inputs
- Independent Power Supplies for Low Crosstalk

2 Applications

- Professional Audio Equipment
- HiFi Smartphone
- Consumer Home Audio Equipment
- Headphone Drivers

3 Description

In applications requiring a high-power output, very high fidelity headphone amplifier, the TPA6120A2 replaces a costly discrete design and allows music, not the amplifier, to be heard. The TPA6120A2's current-feedback AB amplifier architecture delivers high bandwidth, extremely low noise, and up to 128dB of dynamic range.

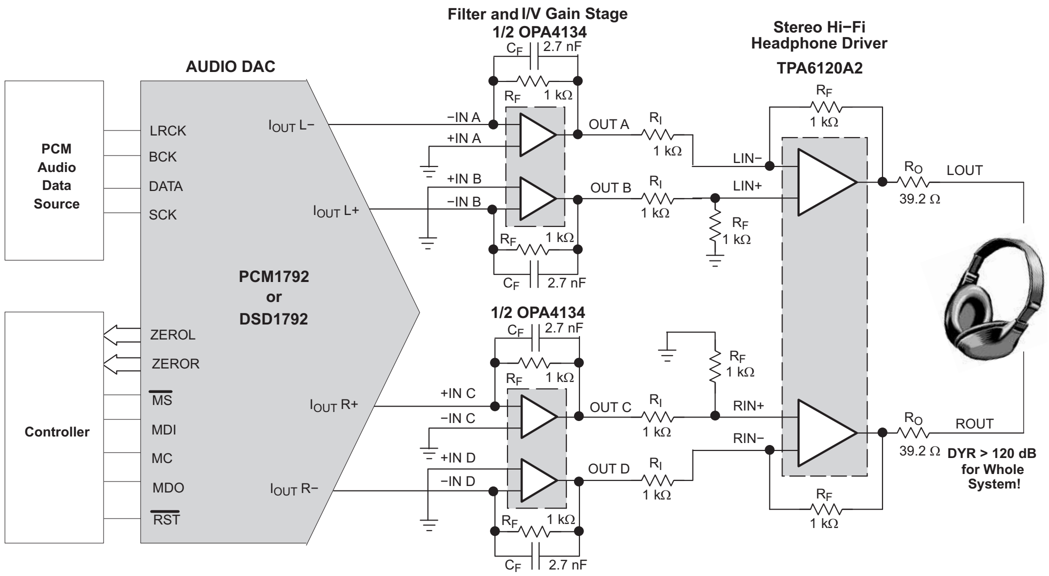
Three key features make current-feedback amplifiers outstanding for audio. The first feature is the high slew rate that prevents odd order distortion anomalies. The second feature is current-on-demand at the output that enables the amplifier to respond quickly and linearly when necessary without risk of output distortion. When large amounts of output power are suddenly needed, the amplifier can respond extremely quickly without raising the noise floor of the system and degrading the signal-to-noise ratio. The third feature is the gain-independent frequency response that allows the full bandwidth of the amplifier to be used over a wide range of gain settings.

Table 1. Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA6120A2	DWP (20)	7.5mm x 12.82mm
	RGY (14)	3.5mm x 3.5mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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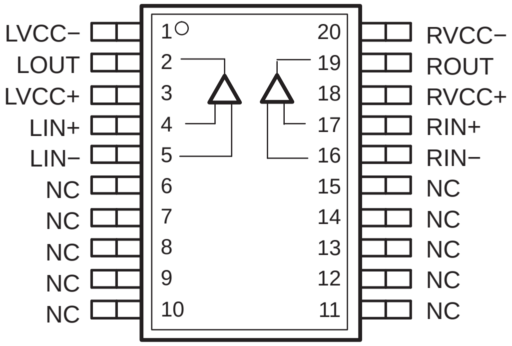
5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision Initial (March 2004) to Revision A	Page
• Changed format of data sheet to new 2014 layout	1
• Added VQFN package information	1
• Updated Pin descriptions to clarify power supply.	3
• Lowered minimum V_{IC}(±5Vcc) from ±3.6 to ±3.4	5
• Lowered minimum V_{IC}(±15Vcc) from ±13.4V to ±13.2V	5
• Deleted IMD (Intermodulation Distortion), ±12Vcc data, Dynamic Range (replaced with SNR, in 1V/V gain)	5
• Converted from % to dB	5
• Updated with latest data from newer QFN based EVM.	5

6 Pin Configuration and Functions

DWP (20)
PowerPAD™ Package
Top View



NC − No internal connection

RGY (14)
Thermal PAD
Top View

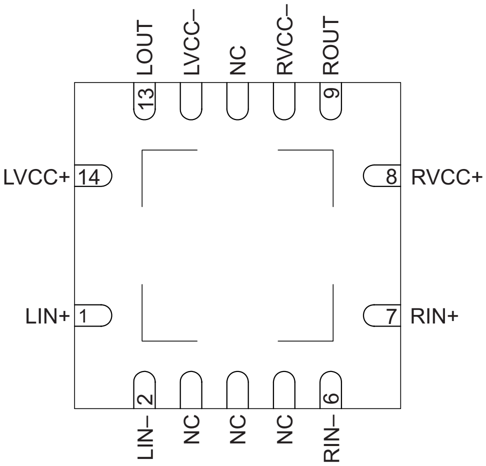


Table 2. Pin Functions

PIN			I/O	DESCRIPTIONS
NAME	DWP NO.	QFN NO.		
LVCC-	1	12	I	Left channel negative power supply – must be kept at the same potential as RVCC- if both amplifiers are to be used.
LOUT	2	13	O	Left channel output
LVCC+	3	14	I	Left channel positive power supply – must be kept at the same potential as RVCC+ if both amplifiers are to be used.
LIN+	4	1	I	Left channel positive input
LIN-	5	2	I	Left channel negative input
NC	6,7,8,9,10,11,12 ,13,14,15	3, 4, 5, 11	-	Not internally connected
RIN-	16	6	I	Right channel negative input
RIN+	17	7	I	Right channel positive input
RVCC+	18	8	I	Right channel positive power supply - must be kept at the same potential as LVCC+ if both amplifiers are to be used.
ROUT	19	9	O	Right channel output
RVCC-	20	10	I	Right channel negative power supply - must be kept at the same potential as LVCC- if both amplifiers are to be used.
Thermal Pad	-	-	-	Connect to ground. The thermal pad must be soldered down in all applications to properly secure device on the PCB.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage, xV_{CC+} to xV_{CC-} Where x=L or R channel	9	33	V
Input voltage, V_I (2)		± V_{CC}	
Differential input voltage, V_{ID}		6	V
Minimum load impedance		8	Ω
Continuous total power dissipation		See the Thermal Information table	
Operating free–air temperature range, T_A	–40	85	°C
Operating junction temperature range, T_J (3)	–40	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

(2) When the TPA6120A2 is powered down, the input source voltage must be kept below 600mV peak.

(3) The TPA6120A2 incorporates an exposed PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature that could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage Temperature		–40	125	°C
$V_{(ESD)}$	Electrostatic Discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, LVCC+, RVCC+, LVCC-, RVCC- pins (1)	–500	500	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all other pins	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	–1500	1500	V

(1) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

7.3 Thermal Information

THERMAL METRIC (1)		TPA6120A2	TPA6120A2	UNITS
		DWP	RGY	
		20 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.5	49.4	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	55.2	62.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.1	25.4	
ψ_{JT}	Junction-to-top characterization parameter	23.1	1.6	
ψ_{JB}	Junction-to-board characterization parameter	36.2	25.5	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	7.6	6.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} and V_{CC-}	Split Supply	±5		±15	V
	Single Supply	10		30	
Load impedance	V_{CC} = ±5V or ±15V	16			Ω
Operating free–air temperature, T_A		–40		85	°C

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{IO} \rvert$	Input offset voltage (measured differentially)	V_{CC} = ±5V or ±15V		2	5	mV
PSRR	Power supply rejection ratio	V_{CC} = ±5V to±15V		75		dB
V_{IC}	Common mode input voltage	V_{CC} = ±5V	±3.4	±3.7		V
		V_{CC} = ±15V	±13.2	±13.5		
I_{CC}	Supply current (each channel)	V_{CC} = ±5V		11.5	13	mA
		V_{CC}= ±15V			15	
I_O	Output current (per channel)	V_{CC}= ±5V to ±15V		700		mA
	Input offset voltage drift	V_{CC} = ±5V or ±15V		20		µV/°C
r_i	Input resistance			300		kΩ
r_o	Output resistance	Open Loop		13		Ω
V_O	Output voltage swing	V_{CC} = ±15V, R_L = 25Ω	11.8 to -11.5	12.5 to -12.2		V

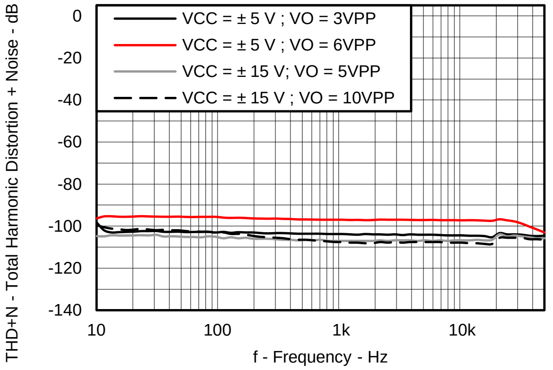
7.6 Operating Characteristics(1)

T_A = 25°C, R_L = 25Ω, Gain = 1V/V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD+N	Total harmonic distortion plus noise	R_L = 32Ω f = 1kHz	V_{CC} = ±5V P_O = 10mW		101		dB
			V_{CC} = ±15V P_O = 100mW		90		
		R_L = 64Ω f = 1kHz	V_{CC} = ±5V P_O = 10mW		104		
			V_{CC} = ±15V P_O = 100mW		94		
		V_{CC} = ±5V, Gain = 1V/V	V_O = 3V_{PP}, R_L = 10kΩ f = 1kHz		104		
		V_{CC} = ±15V, Gain = 1V/V	V_O = 10V_{PP}, R_L = 10kΩ f = 1kHz		108		
		V_{CC} = ±15V, Gain = 1V/V	V_O = 2V_{PP}, R_L = 10kΩ f = 1kHz		112.5		
k_{SVR}	Supply voltage rejection ratio	R_L = 32Ω f = 1kHz $V_{(RIPPLE)}$ = 1V_{PP}	V_{CC}= ±5V		–75		dB
			V_{CC}= ±15V		–78		
		R_L = 64Ω f = 1kHz $V_{(RIPPLE)}$ = 1V_{PP}	V_{CC}= ±5V		–75		
			V_{CC}= ±15V		–75		
CMRR	Common mode rejection ratio (differential)	V_{CC} = ±5V or ±15V			100		dB
SR	Slew rate	V_{CC} = ±15V, Gain = 5V/V, V_O = 20 V_{PP}			1300		V/µs
		V_{CC} = ±5V, Gain = 2V/V, V_O = 5V_{PP}			900		
V_n	Output noise voltage	V_{CC} = ±5V to ±15V R_L = 16Ω	Gain = 1V/V		0.9		µVrms
SNR	Signal-to-noise ratio	R_L = 32Ω to 64Ω f = 1kHz	V_{CC} = ±15V, Gain = 1V/V. A Weighted		128		dB
			V_{CC} = ±5V, Gain = 1V/V. A Weighted		116		
	Crosstalk	V_I = 1V_{RMS} R_F = 1kΩ R_L = 32Ω to 64Ω f = 1kHz	V_{CC} = ±15V		-112		dB
			V_{CC} = ±5V		-105		

(1) For THD+N, k_{SVR}, and crosstalk, the bandwidth of the measurement instruments was set to 80kHz.

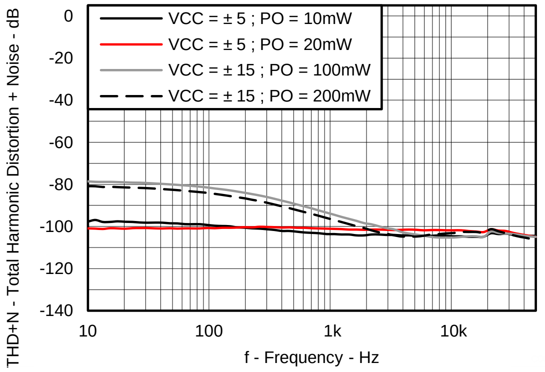
7.7 Typical Characteristics



R_L = 10kΩ Gain = 3V/V R_F = 2kΩ

R_I = 1kΩ BW = 80kHz

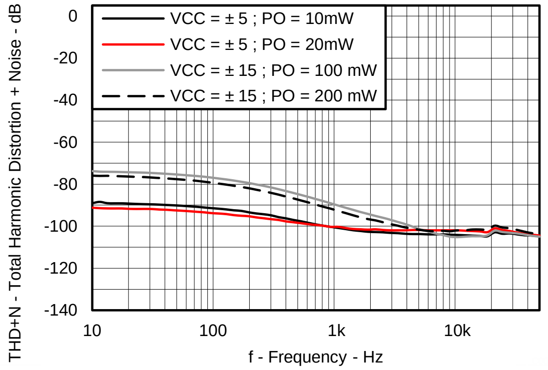
Figure 1. Total Harmonic Distortion + Noise versus Frequency



R_L = 64Ω Gain = 3V/V R_F = 2kΩ

R_I = 1kΩ BW = 80kHz

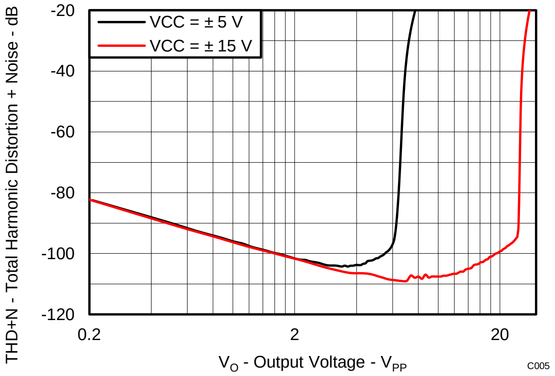
Figure 2. Total Harmonic Distortion + Noise versus Frequency



R_L = 32Ω Gain = 3V/V R_F = 2kΩ

R_I = 1kΩ BW = 80kHz

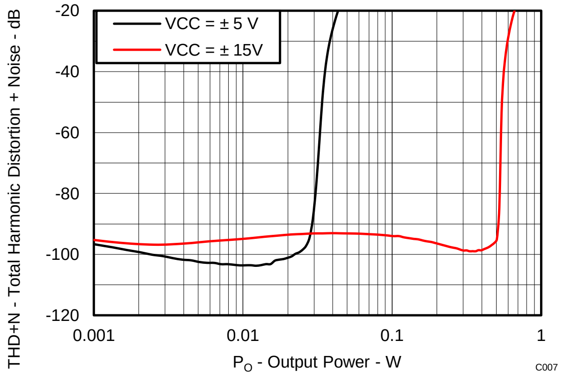
Figure 3. Total Harmonic Distortion + Noise versus Frequency



R_L = 10kΩ Gain = 3V/V R_F = 2kΩ

R_I = 1kΩ BW = 80kHz f = 1kHz

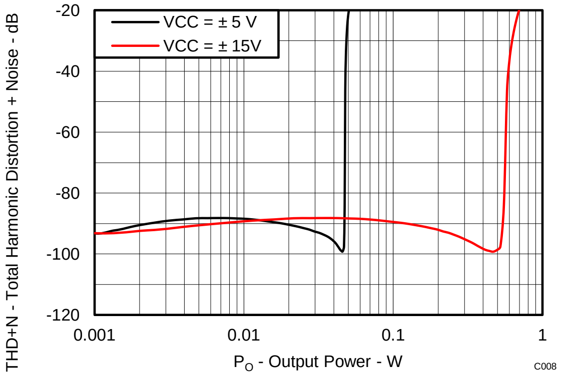
Figure 4. Total Harmonic Distortion + Noise versus Output Voltage



R_L = 64Ω Gain = 3V/V R_F = 2kΩ

R_I = 1kΩ BW = 80kHz f = 1kHz

Figure 5. Total Harmonic Distortion + Noise versus Output Power

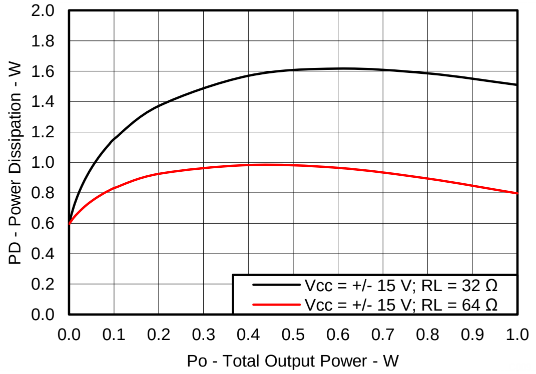


R_L = 32Ω Gain = 3V/V R_F = 2kΩ

R_I = 1kΩ BW = 80kHz f = 1kHz

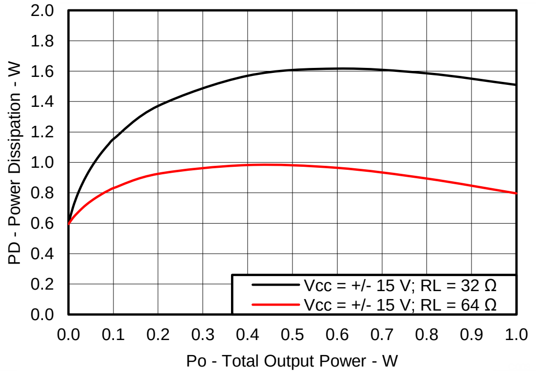
Figure 6. Total Harmonic distortion + Noise versus Output Power

Typical Characteristics (continued)



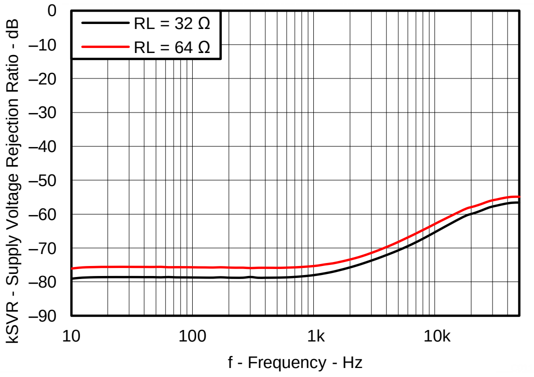
Mono V_{CC} = ±15V

Figure 7. Power Dissipation versus Output Power



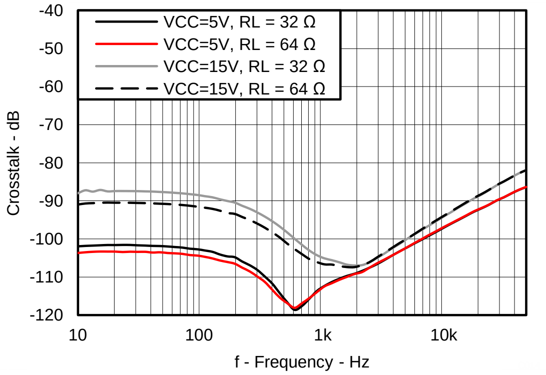
VCC = ±12V $V_{(ripple)}$ = $1V_{PP}$ Gain = 2V/V
BW = 80kHz
Representative of both positive and negative supplies

Figure 8. Power Dissipation versus Total Output Power



VCC = ±5V $V_{(ripple)}$ = $1V_{PP}$ Gain = 2V/V
BW = 80kHz

Figure 9. Supply Voltage rejection Ratio versus Frequency



R_F = 1kΩ Gain = 2V/V BW = 80kHz

Figure 10. Crosstalk versus Frequency

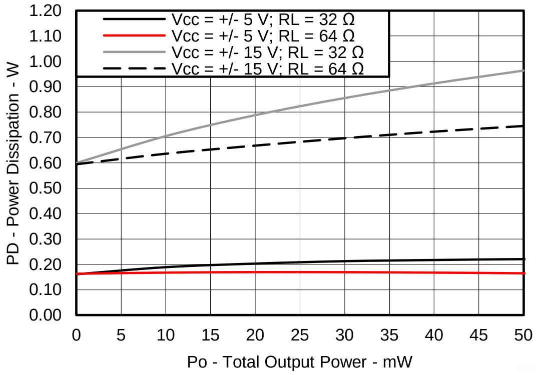
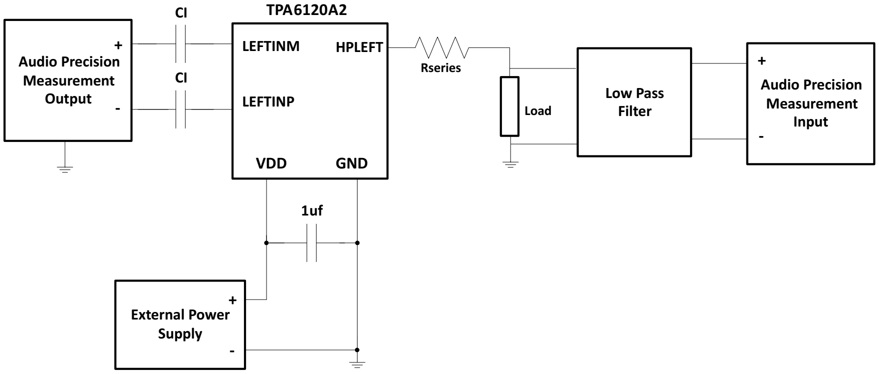


Figure 11. Power Dissipation versus Power Output - 50mW Scale

8 Parameter Measurement Information



A. Separate power supply decoupling capacitors are used on all Vcc pins.

B. The low-pass filter is used to remove harmonic content above the audible range.

Figure 12. Test Circuit

9 Detailed Description

9.1 Overview

The TPA6120A2 is a current-feedback amplifier with differential inputs and single-ended outputs.

9.2 Functional Block Diagram

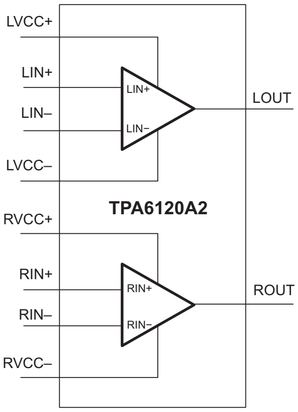


Figure 13. TPA6120A2 Block Diagram

9.3 Feature Description

9.3.1 Current-Feedback Amplifier

Current feedback results in low voltage noise, low distortion, high open-loop gain throughout a large frequency range, and can be used in a similar fashion as voltage-feedback amplifiers. The low distortion of the TPA6120A2 results in a signal-to-noise ratio of 128dB.

9.3.2 Independent Power Supplies

Because the power supplies for the two amplifiers are available separately, one amplifier can be turned off to conserve power.

See Power Supply Recommendations

9.4 Device Functional Modes

This device operates as a wide-bandwidth, current-feedback amplifier.

10 Applications and Implementation

10.1 High Voltage, High Fidelity DAC + Headphone Amplifier Solution

10.1.1 Application Circuit

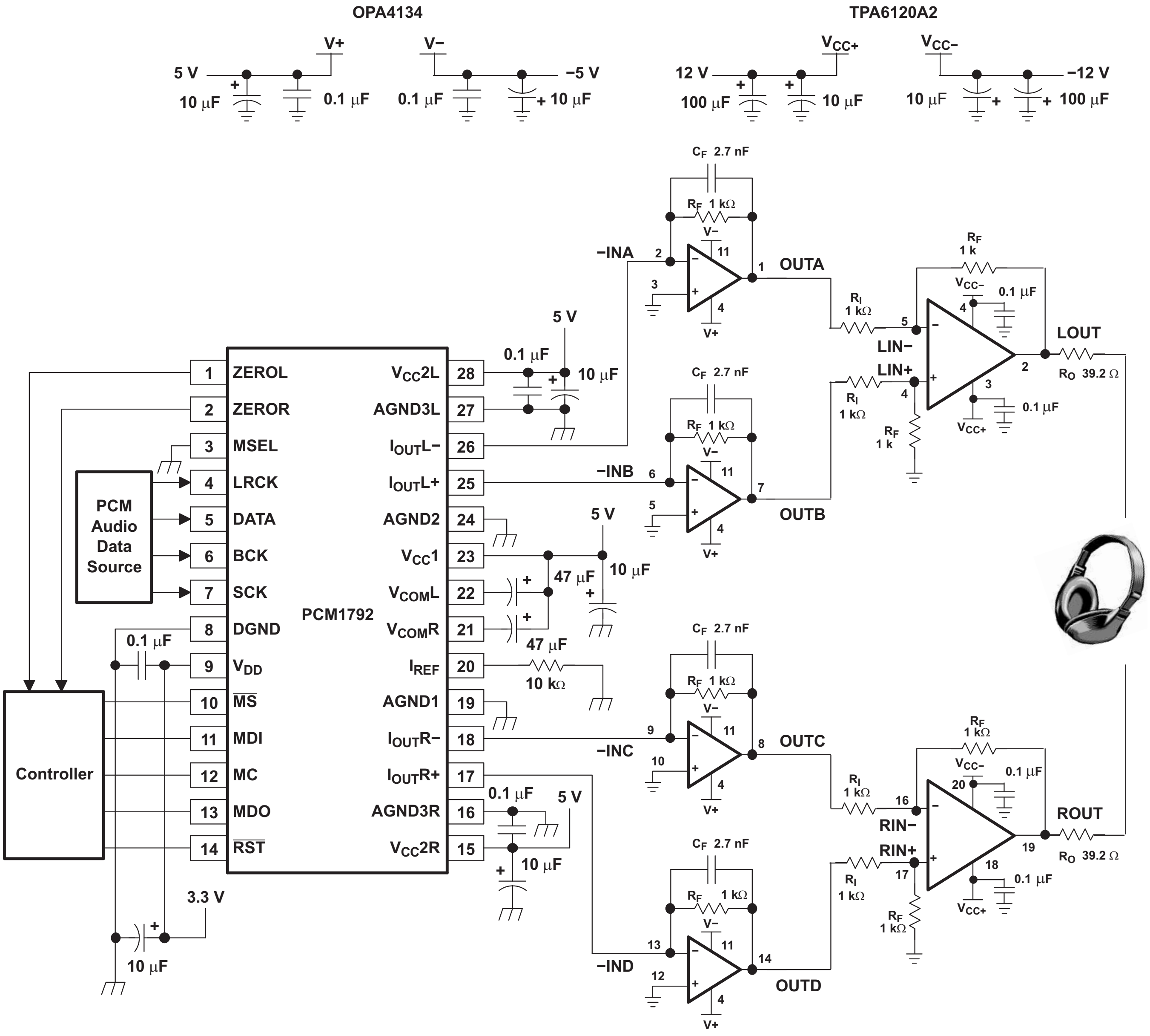


Figure 14. Typical Application Circuit

10.1.1.1 Design Requirements

In many applications, the audio source is digital, and must go through a digital-to-analog converter (DAC) so that traditional analog amplifiers can drive the speakers or headphones.

Figure 14 shows a complete circuit schematic for such a system. The digital audio is fed into a high performance DAC. The PCM1792, a Burr-Brown product from TI, is a 24-bit, stereo DAC.

High Voltage, High Fidelity DAC + Headphone Amplifier Solution (continued)

10.1.1.2 Detailed Design Procedure

The output of the PCM1792 is current, not voltage, so the OPA4134 is used to convert the current input to a voltage output. The OPA4134, a Burr-Brown product from TI, is a low-noise, high-speed, high-performance operational amplifier. C_F and R_F are used to set the cutoff frequency of the filter. The RC combination in Figure 14 has a cutoff frequency of 59 kHz. All four amplifiers of the OPA4134 are used so the TPA6120A2 can be driven differentially.

The output of the OPA4134 goes into the TPA6120A2. The TPA6120A2 is configured for use with differential inputs, stereo use, and a gain of 2V/V. Note that the 0.1µF capacitors are placed at every supply pin of the TPA6120A2, as well as the 39.2Ω series output resistor.

Each output goes to one channel of a pair of stereo headphones, where the listener enjoys crisp, clean, virtually noise free music with a dynamic range greater than the human ear is capable of detecting.

10.1.1.2.1 Resistor Values

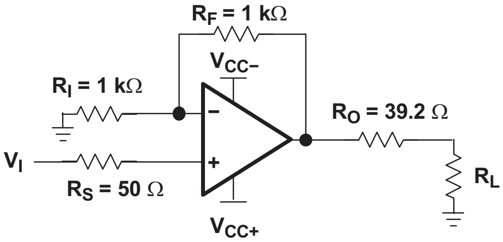


Figure 15. Single-Ended Input With A Noninverting Gain Of 2V/V

In the most basic configuration (see Figure 15), four resistors must be considered, not including the load impedance. The feedback and input resistors, R_F and R_I, respectively, determine the closed-loop gain of the amplifier. R_O is a series output resistor designed to protect the amplifier from any capacitance on the output path, including board and load capacitance. R_S is a series input resistor.

The series output resistor should be between 10Ω and 100Ω. The output series resistance eases the work of the output power stage by increasing the load when low impedance headphones are connected, as well as isolating any capacitance on the following traces and headphone cable.

Because the TPA6120A2 is a current-feedback amplifier, take care when choosing the feedback resistor. TI recommends a lower level of 800Ω for the feedback resistance. No capacitors should be used in the feedback path, as they will form a short circuit at high frequencies.

The value of the feedback resistor should be chosen by using Figure 18 as a guideline. The gain can then be set by adjusting the input resistor. The smaller the feedback resistor, the less noise is introduced into the system. However, smaller values move the dominant pole to higher and higher frequencies, making the device more susceptible to oscillations. Higher feedback resistor values add more noise to the system, but pull the dominant pole down to lower frequencies, making the device more stable. Higher impedance loads tend to make the device more unstable. One way to combat this problem is to increase the value of the feedback resistor. It is not recommended that the feedback resistor exceed a value of 10kΩ. The typical value for the feedback resistor for the TPA6120A2 is 1kΩ. In some cases, where a high-impedance load is used along with a relatively large gain and a capacitive load, it may be necessary to increase the value of the feedback resistor from 1kΩ to 2kΩ, thus adding more stability to the system. Another method to deal with oscillations is to increase the size of R_O.

CAUTION

Do not place a capacitor in the feedback path. Doing so can cause oscillations.

Capacitance at the outputs can cause oscillations. Capacitance from some sources, such as layout, can be minimized. Other sources, such as those from the load (for example, the inherent capacitance in a pair of headphones), cannot be easily minimized. In this case, adjustments to R_O and/or R_F may be necessary.

High Voltage, High Fidelity DAC + Headphone Amplifier Solution (continued)

The series output resistor should be kept at a minimum of 10Ω; small enough so that the effect on the load is minimal, but large enough to provide the protection necessary such that the output of the amplifier sees little capacitance. The value can be increased to provide further isolation, up to 100Ω. Care should be taken in selecting the thermal capacity of the output series resistor, as it will create a potential divider with the load and dissipate power.

The series resistor, R_S, should be used for two reasons:

1. It prevents the positive input pin from being exposed to capacitance from the line and source.
2. It prevents the source from seeing the input capacitance of the TPA6120A2.

The 50Ω resistor was chosen because it provides ample protection without interfering in any noticeable way with the signal. Not shown is another 50Ω resistor that can be placed on the source side of R_S to ground. In that capacity, it serves as an impedance match to any 50Ω source. See Figure 15

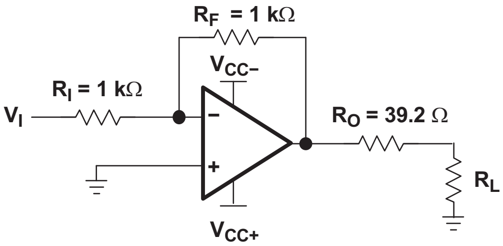


Figure 16. Single-Ended Input With A Noninverting Gain Of –1V/V

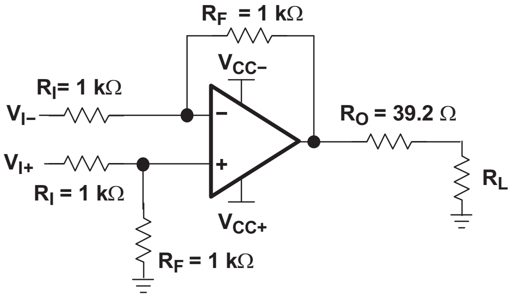


Figure 17. Differential Input With A Noninverting Gain Of 2V/V

Figure 17 shows the TPA6120A2 connected with differential inputs. Differential inputs are useful because they take the greatest advantage of the high CMRR of the device. The two feedback resistor values must be kept the same, as do the input resistor values.

High Voltage, High Fidelity DAC + Headphone Amplifier Solution (continued)

Special note regarding mono operation:

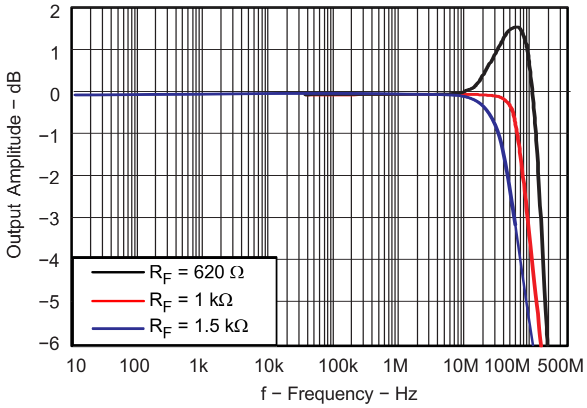
- If both amplifiers are powered on, but only one channel is to be used, the unused amplifier MUST have a feedback resistor from the output to the negative input. Additionally, the positive input should be grounded as close to the pin as possible. Terminate the output as close to the output pin as possible with a 25Ω load to ground.
- These measures should be followed to prevent the unused amplifier from oscillating. If it oscillates, and the power pins of both amplifiers are tied together, the performance of the amplifier could be seriously degraded.

10.1.1.2.2 Checking For Oscillations And Instability

Checking the stability of the amplifier setup is recommended. High frequency oscillations in the megahertz region can cause undesirable effects in the audio band.

Sometimes, the oscillations can be quite clear. An unexpectedly large draw from the power supply may be an indication of oscillations. These oscillations can be seen with an oscilloscope. However, if the oscillations are not obvious, or there is a chance that the system is stable but close to the edge, placing a scope probe with 10pF of capacitance can make the oscillations worse, or actually cause them to start.

A network analyzer can be used to determine the inherent stability of a system. An output versus frequency curve generated by a network analyzer can be a good indicator of stability. At high frequencies, the curve shows whether a system is oscillating, close to oscillation, or stable. In Figure 18 the system is stable because the high frequency rolloff is smooth and has no peaking. Increasing R_F decreases the frequency at which this rolloff occurs (see the Resistor Values section). Another scenario shows some peaking at high frequency. If the peaking is 2dB, the amplifier is stable as there is still 45 degrees of phase margin. As the peaking increases, the phase margin shrinks, causing the amplifier and the system to approach instability. The same system that normally has a 2dB peak has an increased peak when a capacitor is added to the output, indicating that the system is either on the verge of oscillation or is oscillating; corrective action is required.



V_{CC} = ±5V Gain = 1V/V R_L = 25Ω

V_{IN} = 200mV

Figure 18. High Frequency Peaking for Oscillation and Instability

High Voltage, High Fidelity DAC + Headphone Amplifier Solution (continued)

10.1.1.2.3 Thermal Considerations

There is no one to one relationship between output power and heat dissipation, so the following equations must be used:

$$\text{Efficiency of an amplifier} = \frac{P_L}{P_{SUP}} \tag{1}$$

Where

$$P_L = \frac{V_{LRMS}{}^2}{R_L},\ \text{and}\ V_{LRMS} = \frac{V_P}{\sqrt{2}},\ \text{therefore,}\ P_L = \frac{V_P{}^2}{2R_L}\ \text{per channel} \tag{2}$$

$$P_{SUP} = V_{CC} I_{CC}avg + V_{CC}\ I_{CC(q)} \tag{3}$$

$$I_{CCavg} = \frac{1}{\pi}\int_0^{\frac{\pi}{2}} \frac{V_P}{R_L} \sin(t)\,dt = -\frac{V_P}{\pi R_L}\left[\cos(t)\right]_0^{\frac{\pi}{2}} = \frac{V_P}{\pi\,R_L} \tag{4}$$

Where

$$V_P = \sqrt{2\,P_L\,R_L} \tag{5}$$

Therefore,

$$P_{SUP} = \frac{V_{CC}V_P}{\pi\,R_L} + V_{CC}\ I_{CC(q)} \tag{6}$$

P_L = Power delivered to load (per channel)
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on the load
R_L = Load resistance
V_P = Peak voltage on the load
I_{CC}avg = Average current drawn from the power supply
I_{CC}(q) = Quiescent current (per channel)
V_{CC} = Power supply voltage (total supply voltage = 30 V if running on a ±15-V power supply
η = Efficiency of a SE amplifier

For stereo operation, the efficiency does not change because both P_L and P_{SUP} are doubled, affecting the amount of power dissipated by the package in the form of heat.

A simple formula for calculating the power dissipated, P_{DISS}, is shown in Equation 7:

$$P_{DISS} = (1 - \eta)\,P_{SUP} \tag{7}$$

In stereo operation, P_{SUP} is twice the quantity that is present in mono operation.

The maximum ambient temperature, T_A, depends on the heat-sinking ability of the system. $R_{\theta JA}$ for a 20-pin DWP, whose thermal pad is properly soldered down, is shown in Thermal Information. Also see Figure 19.

$$T_A\ \text{Max} = T_J\ \text{Max} - \Theta_{JA}\ P_{Diss} \tag{8}$$

10.1.2 Application Performance Plots

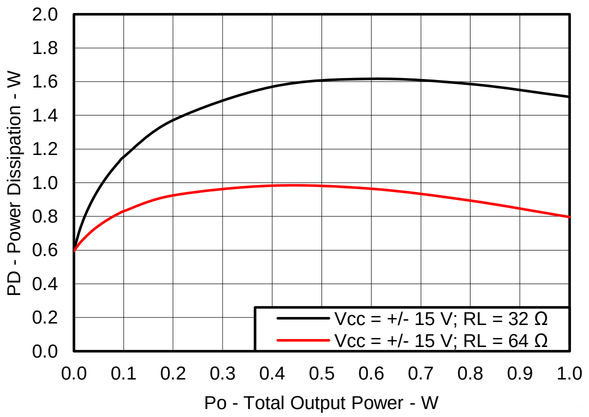


Figure 19. Power Dissipation versus Output Power

10.2 High Fidelity Smartphone Application

10.2.1 Application Circuit

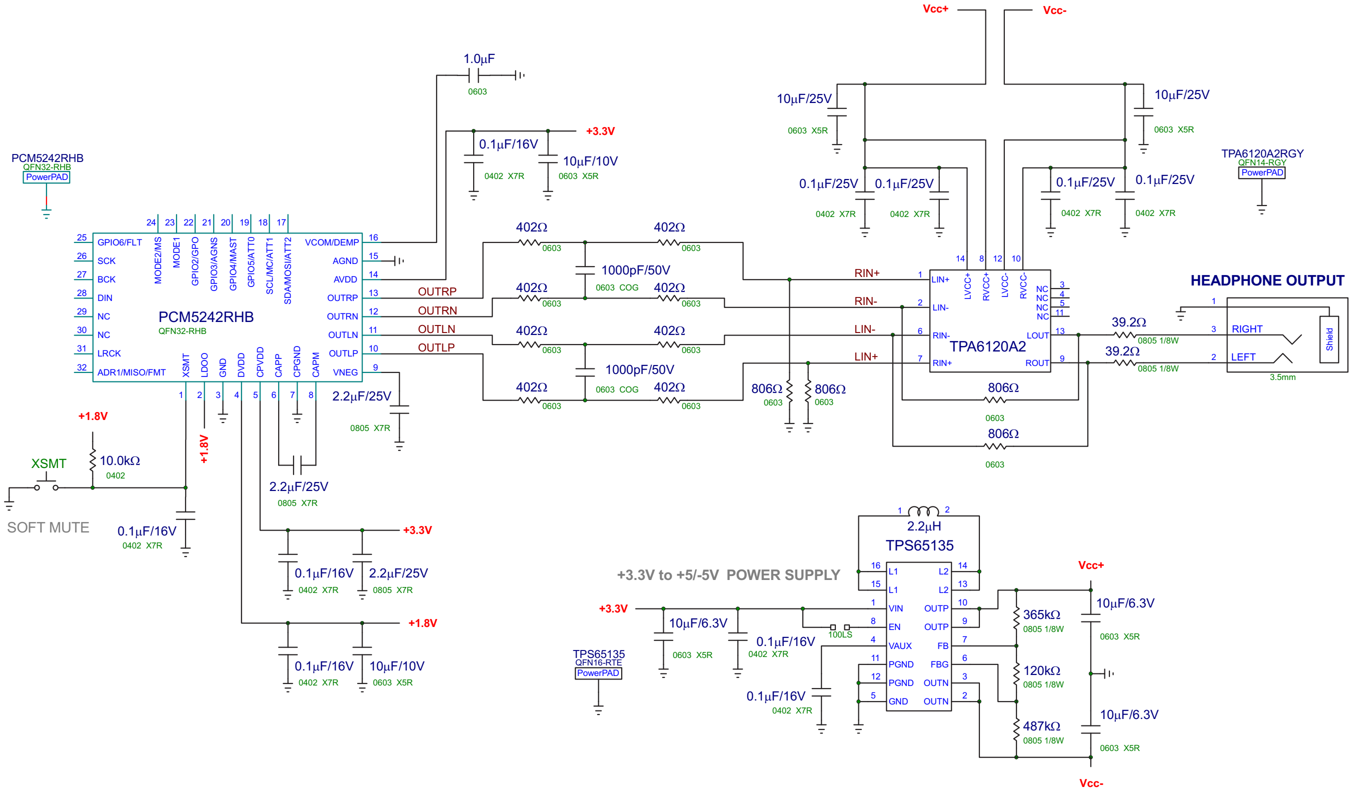


Figure 20. Typical Application Circuit

A new trend in portable applications are termed "Hifi Smartphones". In these systems, a standard portable audio codec continues to be used for telephony, while a separate, higher performance DAC and Headphone Amplifier is used for music playback.

Figure 20 shows a complete circuit schematic for such a system. The digital audio is fed into a high performance DAC. The PCM5242, a Burr-Brown product from TI, is a 32-bit, stereo DAC.

10.2.2 Design Requirements

- ±5V Operation from an over system power supply of 3.3V

High Fidelity Smartphone Application (continued)

- Stereo differential inputs (DAC is differential)
- Be transparent to the user. (DAC SNR and THD+N performance all the way to the headphone)

10.2.3 Design Procedure

For optimal performance, the TPA6120A2 is configured for use with differential inputs, stereo use, and a gain of 1V/V.

The TPA6120A2 requires a bipolar power supply to drive a ground centered output. The application employs a TPS65135 DC-DC converter that generates ±5V from a single 3.3V supply.

The PCM5242 DAC is configured for a 1VRMS output so that clipping is avoided should the 3.3V power supply sag. The PCM5242 offers a ground centered output, so that no DC blocking capacitors are required between it and the TPA6120A2.

Resistor values around the TPA6120A2 of 806Ω and a 39.2Ω were found to offer the optimal conditions of SNR and THD. Starting with 1KΩ resistors for input and feedback, and 10Ω output resistance, the feedback resistance was lowered to increase the amount of current in the feedback network. The output resistance was increased to ease the load on the headphone amplifier when low impedance headphones are connected. Both of these additions contribute to the excellent SNR and THD of the TPA6120A2 in such a low voltage application.

Note that the 0.1-uF X7R capacitors are placed at every supply pin of the TPA6120A2.

Using such a solution makes the TPA6120A2 transparent in the circuit, even into a low impedance 32Ohm load.

The remaining steps are the same as those described in Resistor Values.

10.2.4 Application Performance Plots

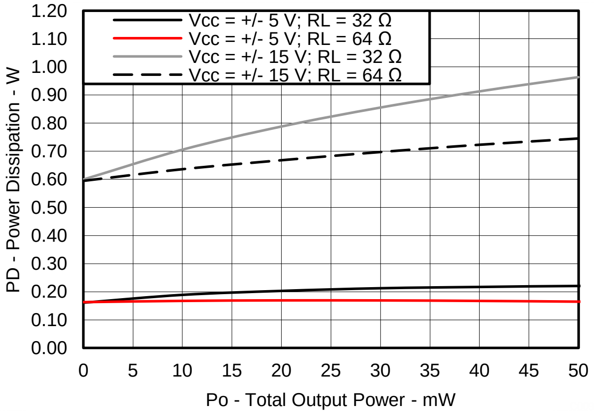


Figure 21. Power Dissipation versus Power Output - 50mW Scale

In this particular application, the TPA6120A2's performance is transparent and the performance of the system is dictated by the PCM5242 DAC.

11 Power Supply Recommendations

11.1 Independent Power Supplies

The TPA6120A2 consists of two independent high-fidelity amplifiers. Each amplifier has its own voltage supply, allowing the user to leave one of the amplifiers off, saving power, reducing the generated heat, and reducing crosstalk.

Although the power supplies are independent, there are some limitations. When both amplifiers are used, the same voltage must be applied to each amplifier. For example, if the left channel amplifier is connected to a ±12-V supply, the right channel amplifier must also be connected to a ±12-V supply. If the device is connected to a different supply voltage, it may not operate properly and consistently.

When the use of only one amplifier is preferred, it must be the left amplifier. The voltage supply to the left amplifier is also responsible for internal start-up and bias circuitry of the device. Regardless of whether one or both amplifiers are used, the V_{CC-} pins of both amplifiers must always be at the same potential.

To power down the right channel amplifier, disconnect the V_{CC+} pin from the power source.

The two independent power supplies can be tied together on the board to receive their power from the same source.

11.2 Power Supply Decoupling

As with any design, proper power supply decoupling is essential. Decoupling prevents noise from entering the device via the power traces and provides the extra power the device can sometimes require in a rapid fashion, preventing the device from being momentarily current-starved. Both of these functions serve to reduce distortion, leaving a clean, uninterrupted signal at the output.

Bulk decoupling capacitors should be used where the main power is brought to the board. Smaller capacitors should be placed as close as possible to the actual power pins of the device. Because the TPA6120A2 has four power pins, use four surface mount capacitors. Both types of capacitors should be low ESR.

12 Layout

12.1 Layout Guidelines

Proper board layout is crucial to getting the maximum performance out of the TPA6120A2.

A ground plane should be used on the board to provide a low inductive ground connection. Having a ground plane underneath traces adds capacitance, so care must be taken when laying out the ground plane on the underside of the board (assuming a 2-layer board). The ground plane is necessary on the bottom for thermal reasons.

Stray capacitance can still make its way onto the sensitive outputs and inputs. Place components as close as possible to the pins and reduce trace lengths. See Figure 22 and Figure 23. Place the feedback resistor and the series output resistor extremely close to the pins. The input resistor should also be placed close to the pin. If the amplifier is to be driven in a noninverting configuration, ground the input close to the device so the current has a short, straight path to the PowerPAD (gnd).

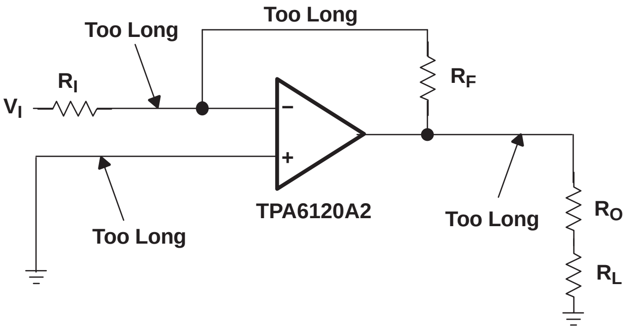


Figure 22. Layout That Can Cause Oscillation

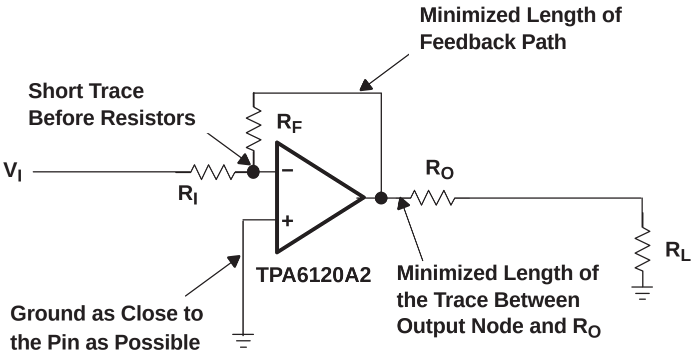


Figure 23. Layout Designed To Reduce Capacitance On Critical Nodes

12.2 Layout Example

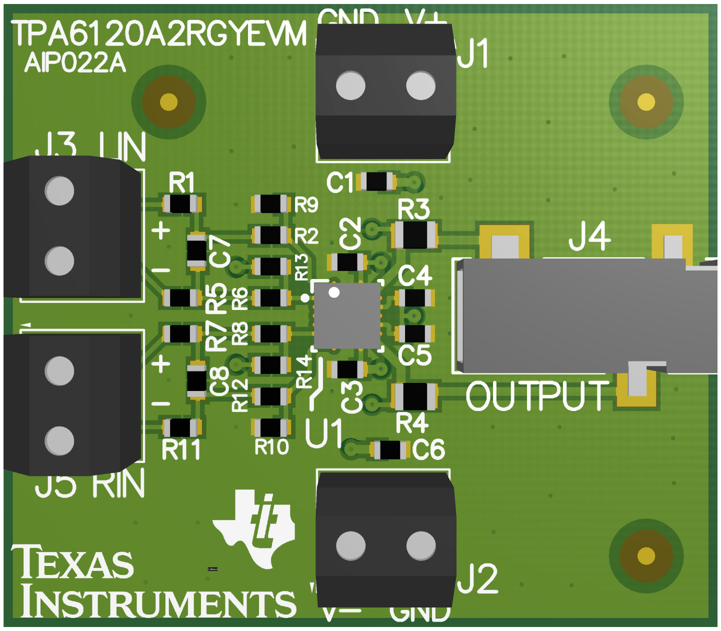


Figure 24. PCB Layout Example

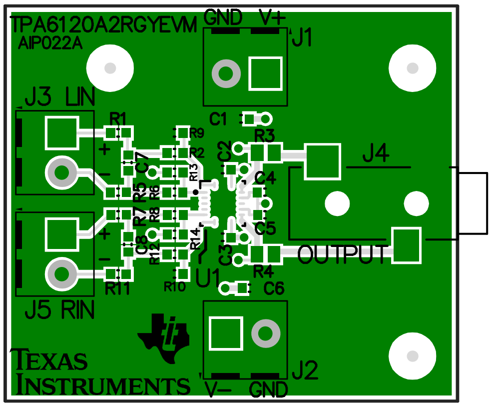


Figure 25. Example PCB Layout, Top Layer and Silkscreen, Top View

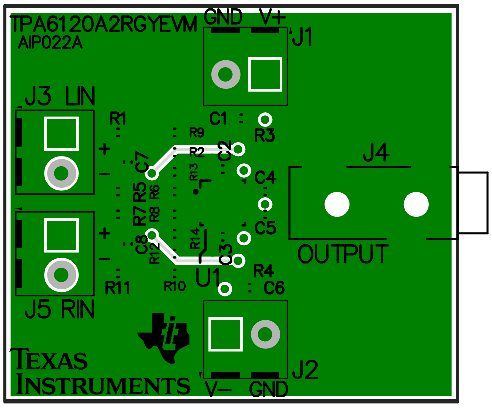


Figure 26. Example PCB Layout, Middle-1 Layer and Silkscreen, Top View

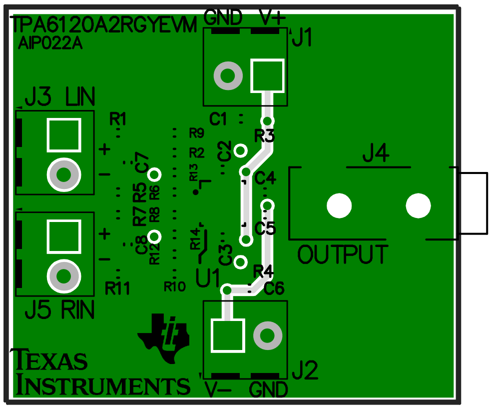


Figure 27. Example PCB Layout, Middle-2 Layer and Silkscreen, Top View

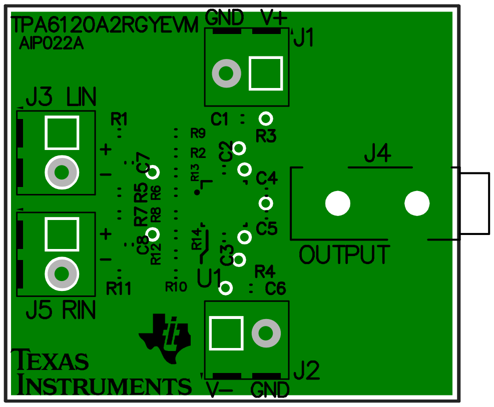


Figure 28. Example PCB Layout, Bottom Layer and Silkscreen, Top View

Layout Example (continued)

This is part of a 4-layer board, where ground, V+, V- are on the bottom and two middle traces, respectively. Key items to note in this layout:

1. R4 and R3 are the output resistors in the schematic. They are sized as 0603 surface mount resistors instead of 0402 for their thermal capacity, as they will be dissipating heat, depending on the output power.
2. Traces are kept as short as possible to avoid any capacitance or oscillation issues.
3. In systems that may be using the DWP package with through hole resistors, it's strongly suggested that the input and output pins and components do not have a ground plane directly beneath them, to avoid stray capacitance.

13 Device and Documentation Support

13.1 Documentation Support (if applicable)

13.1.1 Related Documentation

Headphone Amplifier Parametric Table

13.2 Trademarks

PowerPAD is a trademark of Texas Instruments.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6120A2DWP	ACTIVE	SO PowerPAD	DWP	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6120A2	Samples
TPA6120A2DWPG4	ACTIVE	SO PowerPAD	DWP	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6120A2	Samples
TPA6120A2DWPR	ACTIVE	SO PowerPAD	DWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6120A2	Samples
TPA6120A2DWPRG4	ACTIVE	SO PowerPAD	DWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6120A2	Samples
TPA6120A2RGYR	ACTIVE	VQFN	RGY	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6120A2	Samples
TPA6120A2RGYT	ACTIVE	VQFN	RGY	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6120A2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

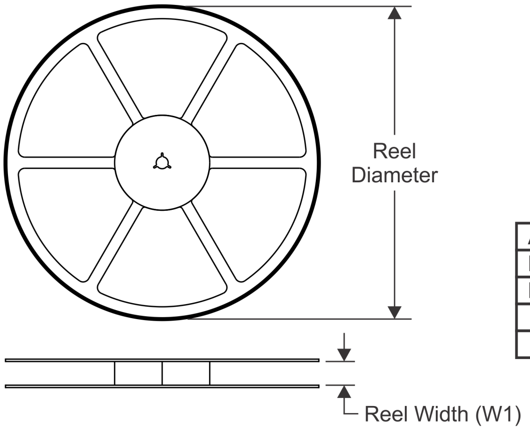
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

---

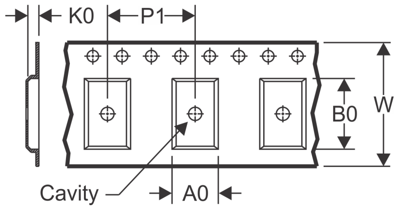
[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

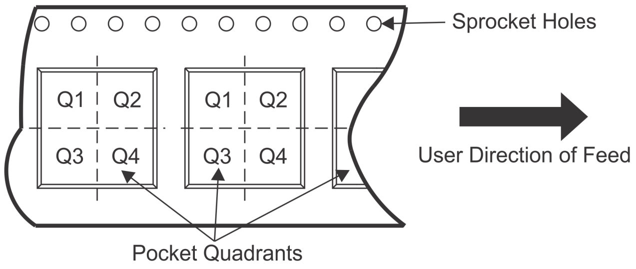


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

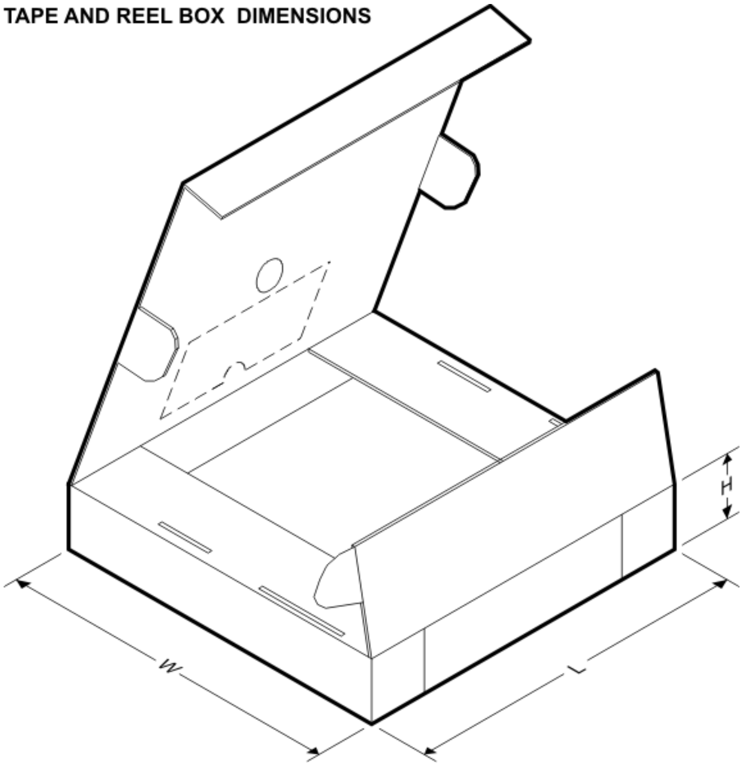


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6120A2DWPR	SO Power PAD	DWP	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TPA6120A2RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TPA6120A2RGYT	VQFN	RGY	14	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

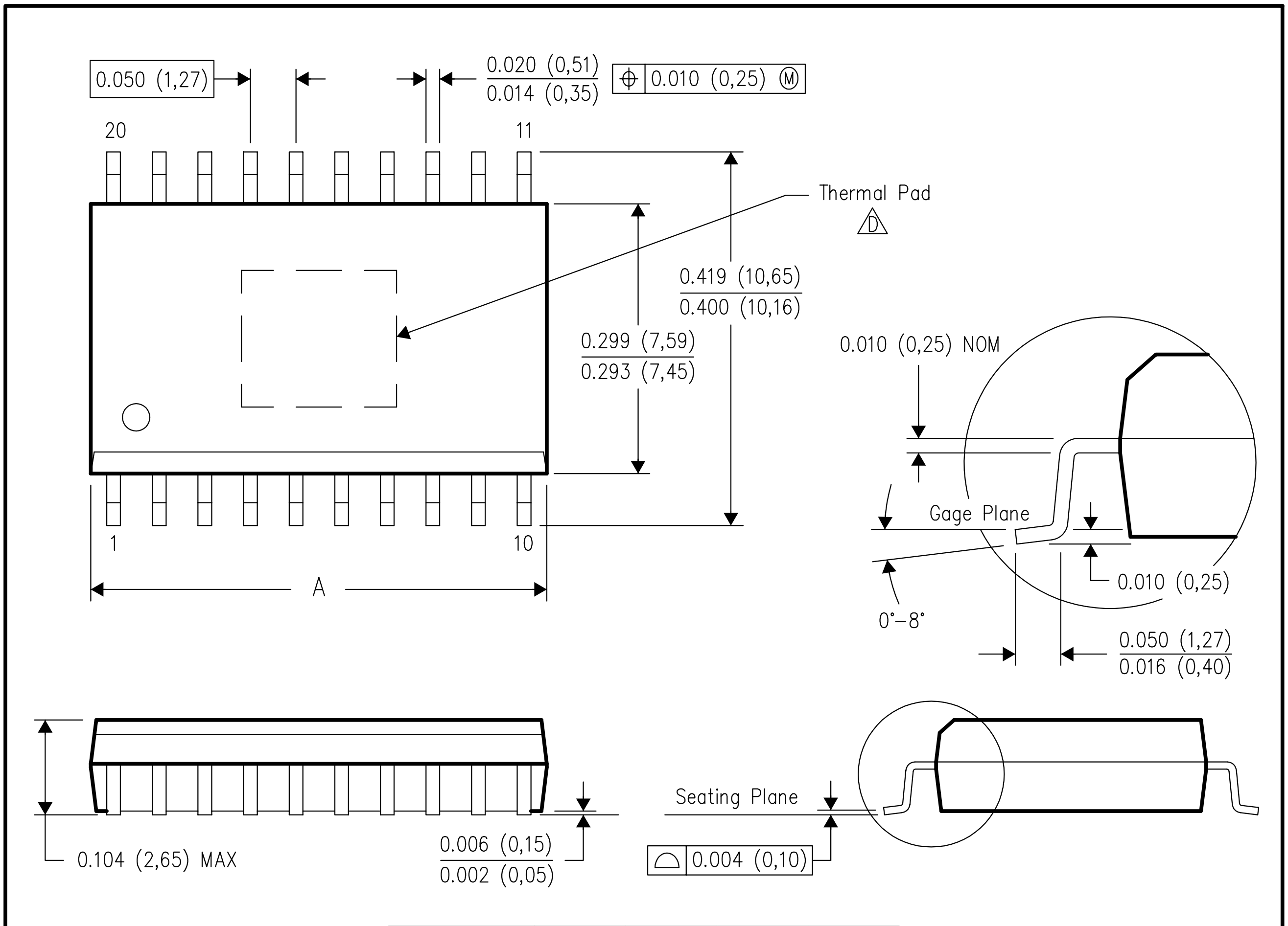


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6120A2DWPR	SO PowerPAD	DWP	20	2000	367.0	367.0	45.0
TPA6120A2RGYR	VQFN	RGY	14	3000	367.0	367.0	35.0
TPA6120A2RGYT	VQFN	RGY	14	250	210.0	185.0	35.0

DWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PINS SHOWN



PINS ** DIM	16	20	24	28
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)	0.710 (18,03)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)	0.700 (17,78)

4147575/C 02/05

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.

PowerPAD is a trademark of Texas Instruments.

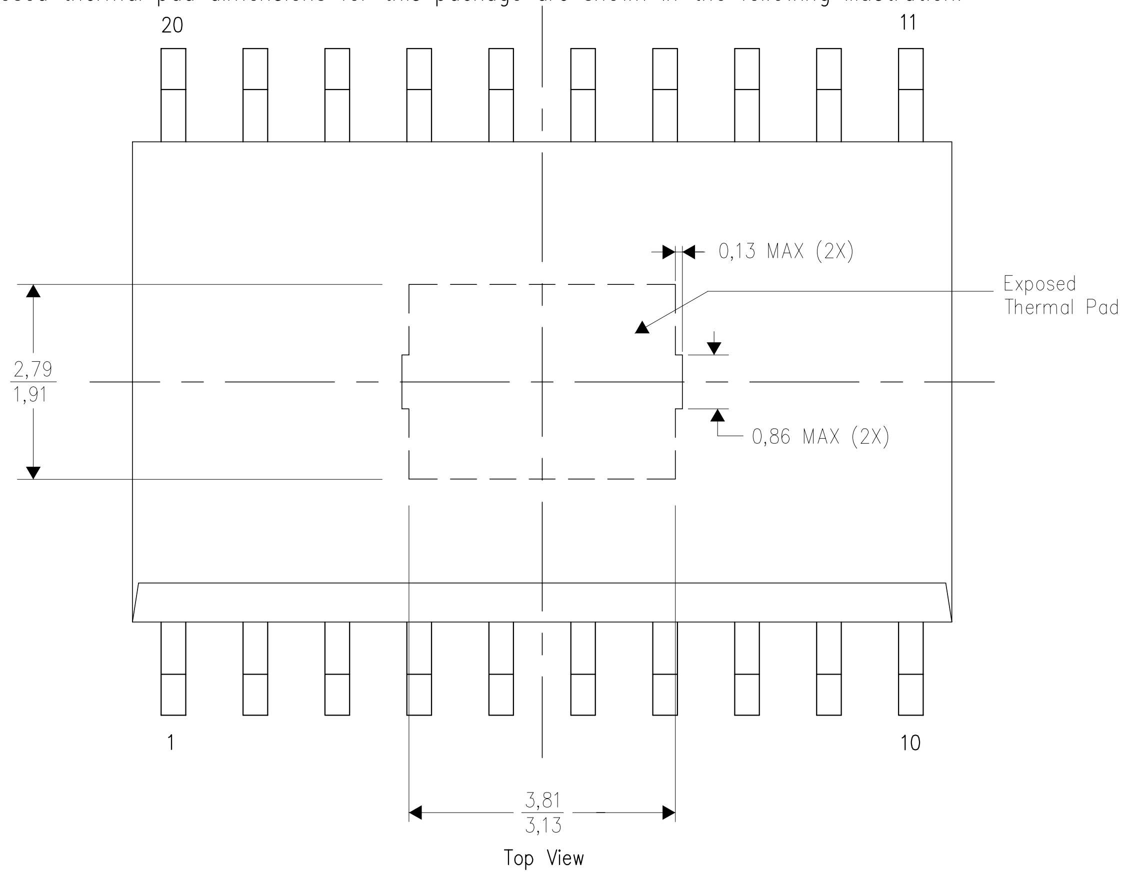
DWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

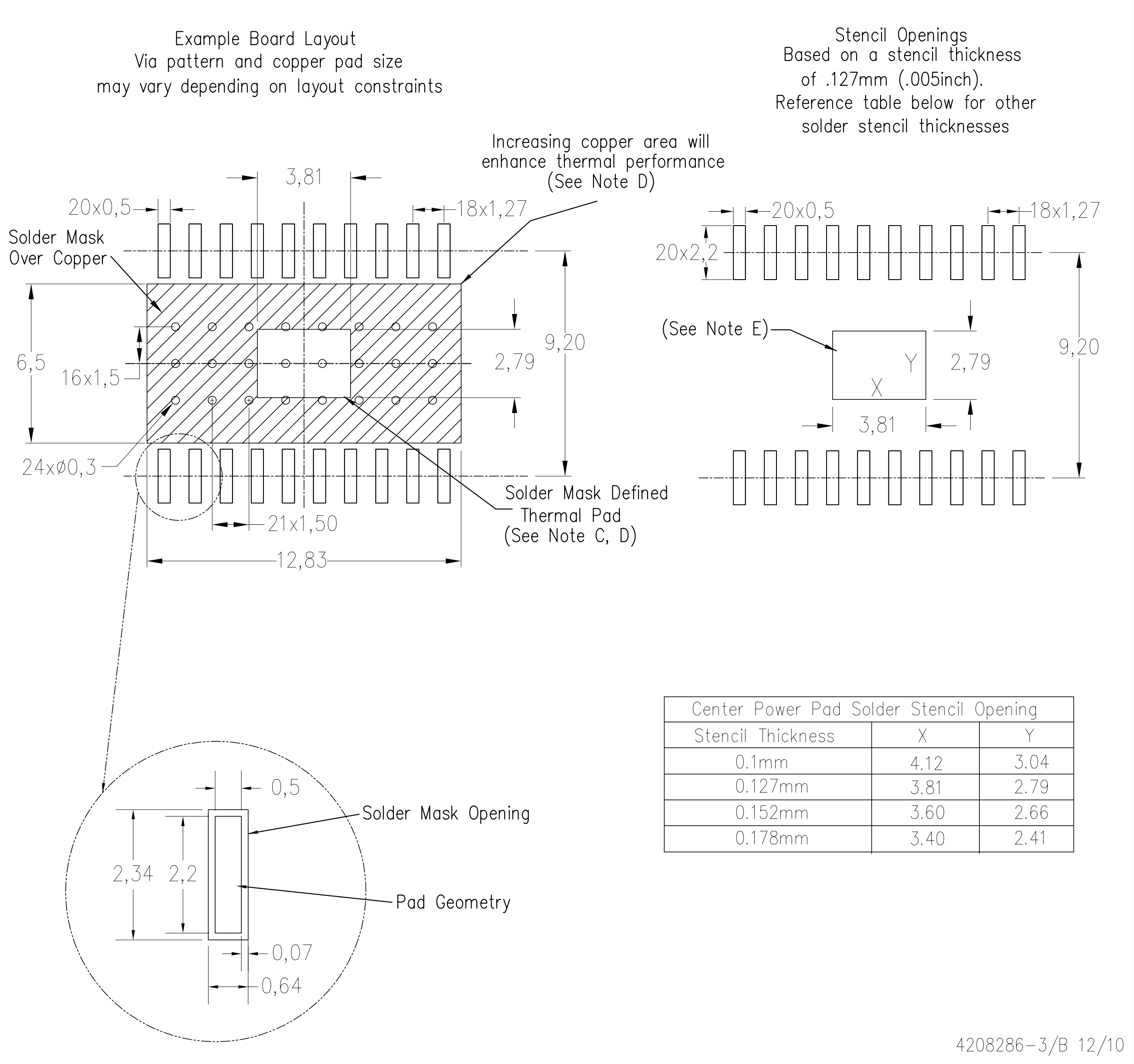


Exposed Thermal Pad Dimensions

4206325–4/E 12/10

NOTE: A. All linear dimensions are in millimeters

DWP (R-PDSO-G20) PowerPAD™ PLASTIC SMALL OUTLINE

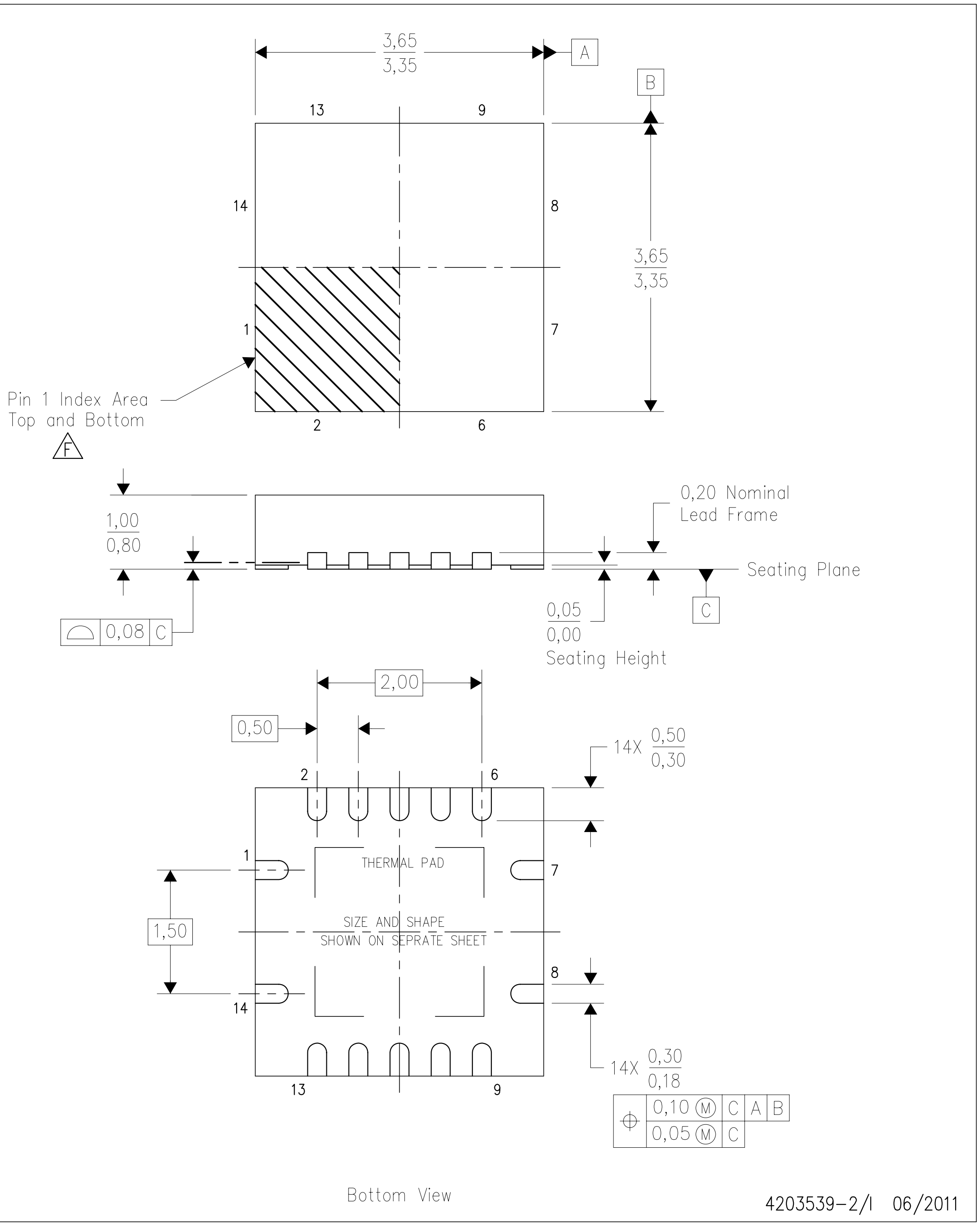


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.12	3.04
0.127mm	3.81	2.79
0.152mm	3.60	2.66
0.178mm	3.40	2.41

4208286-3/B 12/10

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste.

RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/I 06/2011

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.

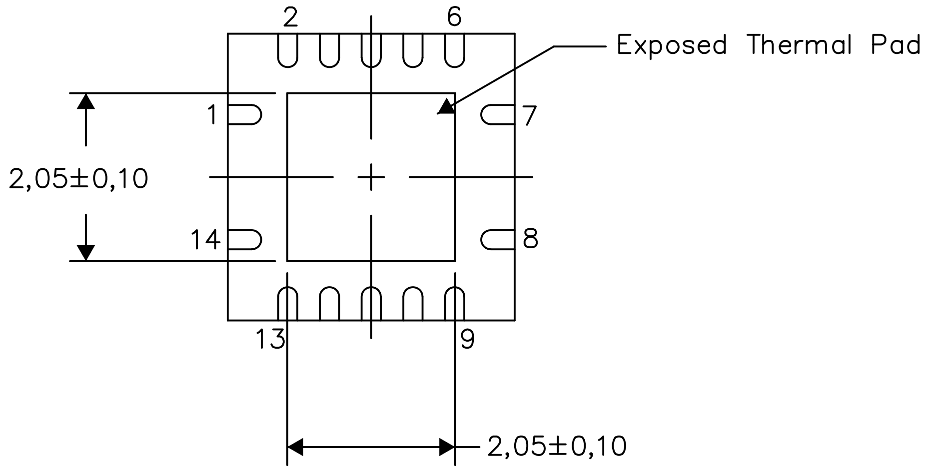
RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



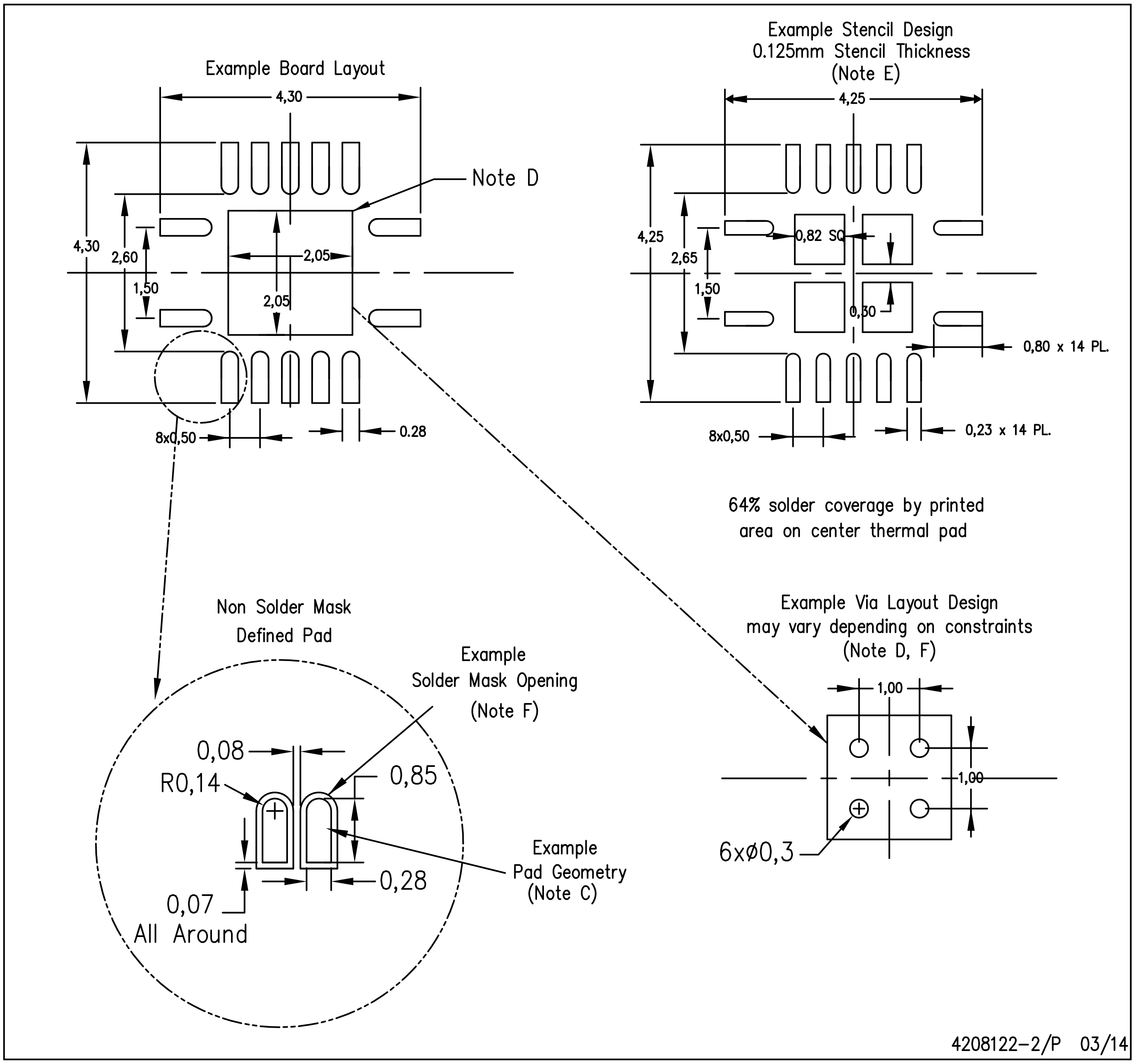
Bottom View

Exposed Thermal Pad Dimensions

4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (S–PVQFN–N14) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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