PICMG 2.0 D3.0

CompactPCI Specification

September 24, 1999

DRAFT SPECIFICATION

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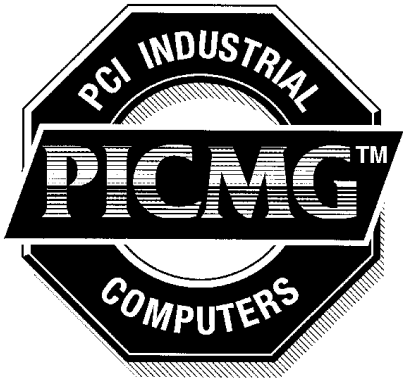

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1 Overview

1.1 CompactPCI Objectives

CompactPCI is an adaptation of the *Peripheral Component Interconnect (PCI) Specification* 2.1 or later for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI. CompactPCI uses industry standard mechanical components and high performance connector technologies to provide an optimized system intended for rugged applications. CompactPCI provides a system that is electrically compatible with the PCI Specification, allowing low cost PCI components to be utilized in a mechanical form factor suited for rugged environments.

CompactPCI is an open specification supported by the PICMG (PCI Industrial Computer Manufacturers Group), which is a consortium of companies involved in utilizing PCI for embedded applications. PICMG controls this specification.

1.2 Background and Terminology

Eurocard - A series of mechanical board form factor sizes for rack-based systems as used in VME, Multibus II, and other applications defined by the Institute of Electrical and Electronics Engineers (IEEE) and International Electrotechnical Committee (IEC).

ISA - Industry Standard Architecture. A specification by which Personal Computers (PCs) add boards.

PCI - Peripheral Component Interconnect. A specification for defining a common interconnect between logic components. Typically used for interconnecting high-speed, PC-compatible chipset components. The PCI specification is issued through the PCI Special Interest Group (PCI SIG).

This specification utilizes several key words, which are defined below:

may: A key word indicating flexibility of choice with no implied preference.

shall: A key word indicating a mandatory requirement. Designers **shall** implement such mandatory requirements to ensure interchangeability and to claim conformance with the specification.

should: A key word indicating flexibility of choice with a strongly preferred implementation.

1.3 Desired Audience

CompactPCI exists to provide a standard form factor for those applications requiring the high performance of PCI as well as the small size and ruggedness of a rack mount system. CompactPCI provides a mechanism for OEM and end users to di-

rectly apply PCI components and technology to a new mechanical form factor while maintaining compatibility with existing operating systems and application software available for desktop PCI.

1.4 CompactPCI Features

CompactPCI has the following feature set:

- 33 and 66 MHz PCI performance
- 32- and 64-bit data transfers
- 8 CompactPCI slots per bus segment at 33 MHz
- 5 CompactPCI slots per bus segment at 66 MHz
- Industry standard software support
- 3U small form factor (100 mm by 160 mm)
- 6U form factor (233.35 mm by 160 mm)
- IEEE (1101.1, 1101.10 and 1101.11) Eurocard packaging
- Wide variety of available I/O
- System Management Bus

1.5 Applicable Documents

This *CompactPCI Specification* builds on several industry standards. You should reference the following list of publications while reading this specification.

- *PCI Local Bus Specification*, PCI Special Interest Group, 5200 N. E. Elam Young Parkway, Hillsboro, Oregon, USA, 97124-6497, (503) 696-2000, http://www.pcisig.org
- PICMG 2.1, *CompactPCI Hot Swap Specification*, PCI Industrial Manufacturers Group (PICMG), 301 Edgewater Place, Suite 220, Wakefield, MA 01880 USA, Tel: 781.224.1100, Fax: 781.224.1239, www.picmg.org
- PICMG 2.10, *CompactPCI Keying Specification*, PCI Industrial Manufacturers Group (PICMG), 301 Edgewater Place, Suite 220, Wakefield, MA 01880 USA, Tel: 781.224.1100, Fax: 781.224.1239, www.picmg.org
- PICMG 2.9, *CompactPCI System Management Specification,* PCI Industrial Manufacturers Group (PICMG), 301 Edgewater Place, Suite 220, Wakefield, MA 01880 USA, Tel: 781.224.1100, Fax: 781.224.1239, www.picmg.org
- PICMG 2.11, *CompactPCI Power Interface Specification,* PCI Industrial Manufacturers Group (PICMG), 301 Edgewater Place, Suite 220, Wakefield, MA 01880 USA, Tel: 781.224.1100, Fax: 781.224.1239, www.picmg.org
- IEC 60297-3 and -4, *Eurocard Specification*, International Electrotechnical Commission, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY, USA 10036, http://www.iec.ch

- IEC-61076-4-101, *Specification for 2 mm Connector Systems*, International Electrotechnical Commission, American National Standards Institute, 11 West 42nd Street, 13th Floor, New York, NY, USA 10036, http://www.iec.ch
- IEEE 1101.1-1991, *IEEE Standard for Mechanical Core Specifications for Microcomputers Using IEC 603-2 Connectors*, Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, P.O. Box 1331, Piscatoway, NJ, USA, 08855-1331, http://www.ieee.org
- IEEE 1101.10, *IEEE Standard for Additional Mechanical Specifications for Microcomputers using IEEE 1101.1 Equipment Practice,* Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, P.O. Box 1331, Piscatoway, NJ, USA, 08855-1331, http://www.ieee.org
- IEEE 1101.11, *IEEE Standard for Additional Mechanical Specifications for Microcomputers using IEEE 1101.1 Equipment Practice,* Institute of Electrical and Electronics Engineers, Inc., 445 Hoes Lane, P.O. Box 1331, Piscatoway, NJ, USA, 08855-1331, http://www.ieee.org
- VITA 30 –199X , *VSO Standard for 2mm Connector Practice for Euroboard Systems,* VITA Standards Organization, 7825 E. Gelding Drive, suite 104, Scottsdale, AZ 85260, http://www.vita.com

1.6 Administration

CompactPCI is an open specification supported by the PCI Industrial Manufacturers Group (PICMG). PICMG maintains this specification and is chartered to:

- Extend the PCI standard into industrial systems
- Manage and maintain relevant PCI specifications
- Contribute to the establishment of relevant PCI specifications as an industry wide specification

For information on how to become a PICMG member, please contact:

PICMG
301 Edgewater Place
Suite 220
Wakefield, MA 01880 USA
Tel: 781.224.1100
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Web: http://www.picmg.org

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- Since the *PICMG* and *CompactPCI* logos, and the *PICMG* and *CompactPCI* names are registered trademarks of the PICMG, the following statement **shall** be included in all published literature and advertising material in which the logo appears:

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2 Feature Set

2.1 Form Factor

The form factor defined for CompactPCI boards is based on the Eurocard form factor as defined in IEC 60297-3 and IEC 60297-4 and extended by IEEE 1101.10. Both 3U (100 mm by 160 mm) and 6U (233.35 mm by 160 mm) board sizes are defined. **Figure 1** shows a 3U style board.

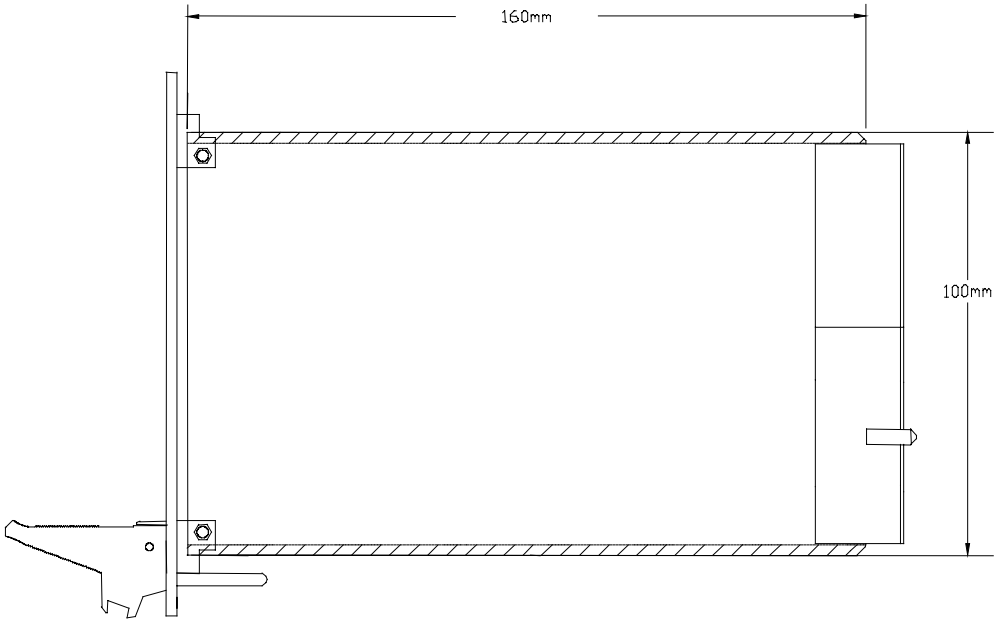


Figure 1. 3U 64-Bit CompactPCI Form Factor.

A CompactPCI system is composed of one or more CompactPCI bus segments. Each segment is composed of up to eight CompactPCI slots (at 33 MHz) with 20.32 mm (0.8 inch) board center-to-center spacing. Each CompactPCI bus segment consists of one System Slot, and up to seven Peripheral Slots.

The System Slot provides arbitration, clock distribution, and reset functions for all boards on the segment. The System Slot is responsible for performing system initialization by managing each local board's IDSEL signal. Physically, the System Slot **may** be located at any position in the backplane. For simplicity, this specification assumes one CompactPCI bus segment in which the System Slot is located on the left of the bus segment when the backplane is viewed from the front side.

The Peripheral Slots may contain simple boards, intelligent slaves, or PCI bus masters. **Figure 2** illustrates the front view of a typical 3U CompactPCI segment.

Other topologies besides the linear arrangement illustrated in **Figure 2** are allowed by CompactPCI. However, this specification and all backplane simulations have assumed a linear topology using 20.32 mm (0.8 inch) board center-to-center spacing with the System Slot located on either end of the bus segment. Any other topology **shall** be simulated or otherwise verified to ensure compliance to the PCI specification.

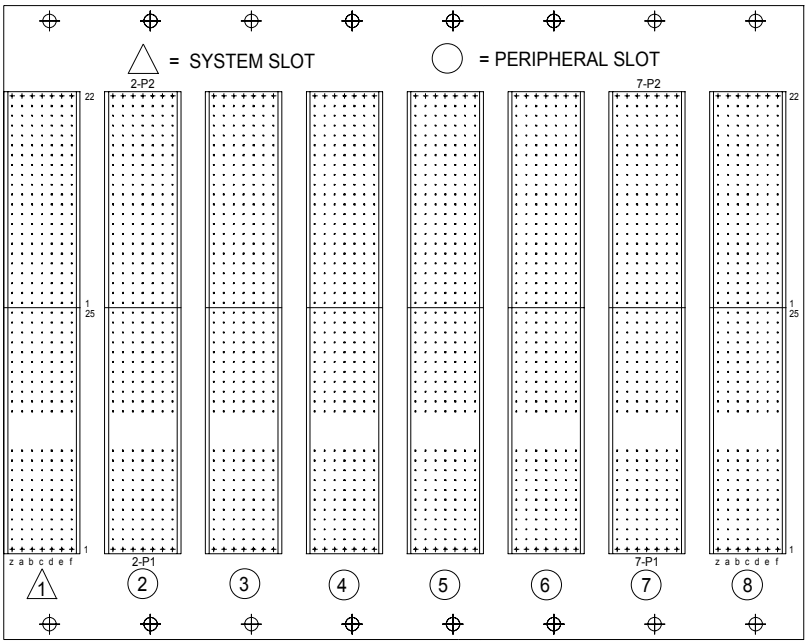


Figure 2. 3U CompactPCI Backplane Example.

CompactPCI defines slot numbering based on the concept of physical and logical slots. Physical slot numbers **shall** start at 1 in the top-left corner of the card cage. All CompactPCI systems **should** label all physical slots within the compatibility glyphs. **Figure 2** illustrates an example of physical slot numbering within the compatibility glyphs (e.g., △1).

Logical slot numbers **shall** be defined by the IDSEL signal and associated address used to select the slot. Logical numbers are used in the nomenclature to define the physical outline of a connector on a bus segment. Logical numbers are illustrated in **Figure 2** just below the connector outline (e.g., 2-P1). Logical and physical slot numbers **may** not always coincide. In either case, Chapter 3 defines signal routing requirements.

Capability glyphs provide visual indication of backplane connector and board capability. Capability glyphs are:

- △ (triangle) for System Slot
- ○ (circle) for Peripheral Slots

2.2 Connector

The CompactPCI connector is a shielded, 2 mm-pitch, 5-row connector as defined by IEC 60917 and IEC 61076-4-101. Features of this connector include:

- Pin and socket interconnect mechanism
- Multi-vendor support
- Coding Mechanism providing positive keying
- Staggered make-break pin populations for hot swap capability
- Rear panel option for through-the-backplane I/O applications
- High density PCI capability
- Shield for EMI/RFI protection
- Expandability for end user applications

CompactPCI bus interconnection is defined as a 5 row by 47 position array of pins divided logically into two groups corresponding to the physical connector implementation. 32-bit PCI and connector keying are implemented on one connector (J1). An additional connector (J2) is defined for 64-bit transfers, for rear-panel I/O or for geographic addressing. See Section 1 for connector pin assignments and signal grouping.

The CompactPCI connector utilizes guiding features located on both the board and backplane connector to ensure correct polarized mating. Proper mating is further enhanced by the use of coding keys for 3.3 V or 5 V operation, with or without hot swap capability, to prevent incorrect installation of boards.

Coding keys prevent inadvertent installation of a 5 V board in a 3.3 V system. **Table 1** illustrates the color coding that relates to different physical keys for the backplane connector and board connectors. Universal boards **shall** operate in either environment and are not keyed. Backplane connectors **shall** always be keyed according to the signaling level on the backplane segment.

Table 1. Coding Key Color Assignments.

Signaling Voltage V(I/O)	Color Reference
3.3 V	Cadmium Yellow
5 V	Brilliant Blue
3.3 V or 5 V (Universal Board)	None

The keying illustration of Table 1 is only a sufficient level of keying if J1 is populated and J1 is the only connector populated. Any CompactPCI board implementation that populates any connector other than J1 **shall** additionally conform to the PICMG 2.10 Keying of CompactPCI Boards and Backplanes

specification. The color coded keying mechanism provided in the J1 connector is sufficient keying only for 3U and 6U non-rear I/O 32 bit signaling boards, any other implementations **shall** conform to the keying mechanism specified in PICMG 2.10.

2.3 Modularity

A key feature of CompactPCI is system modularity. Modularity is achieved by utilizing various Eurocard form factors along with a versatile IEC-61076-4-101 connector. Either the 3U or 6U form factor, or a combination of the two, **may** be used directly to create a system. The IEC-61076-4-101 connector is available in a variety of mechanical form factors for different applications.

2.4 Hot Swap Capability

The *PICMG 2.1, Hot Swap Specification* **shall** be used as a reference for details on the design issues regarding hot swap boards or systems.

3 Electrical Requirements

This section documents the electrical requirements for CompactPCI boards and backplanes.

3.1 Board Design Rules

CompactPCI board design **shall** adhere to the design requirements for standard desktop PCI boards as specified in the PCI Specification. This section documents additional requirements or restrictions as needed. The design rules in sections 3.1 through 3.4 apply to PCI bus operation up to 33 MHz. Refer to section 3.5 for rules applicable to 66 MHz designs.

3.1.1 Decoupling Requirements

Each CompactPCI board **shall** have adequate decoupling for its intended application**.** Table 2 illustrates the minimum requirements that **should** be used. For CompactPCI Hot Swap boards, these requirements are modified. Refer to the Hot Swap Specification, PICMG 2.1 for details.

Table 2. Board Decoupling Requirements.

Connector	Mnemonic	Description	Decoupling Capacitance		Voltage
			.1 µF ±20%(1)	10 µF ±20%(2)	
P1	5V	+5 VDC			15 V min.
P1	3.3V	+3.3 VDC			10 V min.
P1	V(I/O)	+5/3.3 VDC			15 V min.
P1	+12V	+12 VDC		(3)	35 V min.
P1	-12V	-12 VDC		(3)	35 V min.
P2(4)	V(I/O)	+5/3.3 VDC			15 V min.

Notes:

(1) For all voltages, one .1 µF ceramic capacitor suitable for high speed decoupling **should** be provided close to the connector to decouple every 10 power pins. Note this rule applies to all power pins even if unused on board.

(2) One 10 µf low ESR capacitor per voltage **should** be located close to the connector (see note 3).

(3) Only required if ±12 V is used on board. Note, one .1 µF capacitor **should** be provided on +12 V and –12 V even if unused on board.

(4) Requirements for P2 in a 64-bit system. If P2 is used for user defined I/O, additional decoupling capacitance may be required.

3.1.2 CompactPCI Signal Additions

CompactPCI defines some additional signals beyond the PCI specification that may be applicable to board designs. Please refer to Section 3.2.7 for further descriptions.

3.1.3 CompactPCI Stub Termination

Many bussed PCI signals **shall** include a 10 Ω series stub termination resistor located on the board at the CompactPCI connector interface. The signals that **shall** be terminated are: AD0-AD31, C/BE0#-C/BE3#, PAR, FRAME#, IRDY#, TRDY#, STOP#, LOCK#, IDSEL, DEVSEL#, PERR#, SERR#, and RST#.

Table 3. Stub Termination Resistor.

Parameter	Min.	Nominal	Max.	Units	Comment
R_{term}	-5%	10	+5%	Ohms	Stub terminating resistor located at connector on board

If used by a board, the following signals **shall** also be terminated: INTA#, INTB#, INTC#, INTD#, AD32-AD63, C/BE4#-C/BE7#, REQ64#, ACK64#, and PAR64.

The following signals do not require a stub termination resistor: CLK, REQ#, and GNT#.

The stub termination minimizes the effect of the stub on each board to the PCI backplane. The resistor **shall** be placed within 15.2 mm (0.6 inches) of the signal's connector pin. This length **shall** be included in the overall length of trace that is allowed for the signal as described in Sections 3.1.4 and 3.1.6.

Peripheral boards that drive REQ# **should** provide a series terminating resistor (sized according to the output characteristics of the buffer) at the driver pin (not a stub termination resistor at the connector). On System Slot boards, a series resistor (sized according to the output characteristics of the clock buffer) **shall** be located at the driver for the CLK signal provided to each slot. Each System Slot board's GNT# signal **shall** also be series terminated at the driver with a resistor as required by the driving buffer output characteristics.

3.1.4 Peripheral Board Signal Stub Length

Signal length for 32-bit or 64-bit signals (J1, J2) **shall** be less than or equal to 63.5 mm (2.5 inches). This length is measured from the connector pin through

the stub or series termination resistor (described in Section 3.1.3) to the PCI device pin. These lengths are more generous than the PCI Specification requirements but also include the resistor in the total trace length.

A maximum of one PCI load **shall** be allowed on any PCI signal on any peripheral board. Peripheral boards with more than one load are not compliant with the CompactPCI Specification and **shall** not be declared CompactPCI compatible.

3.1.5 Characteristic Impedance

Boards **shall** be fabricated to provide CompactPCI signal traces within the characteristic impedance range given in Table 4.

Table 4. Board Characteristics.

Parameter	Min.	Nominal	Max.	Units	Comment
Z_0	-10%	65	+10%	Ohms	PCB traces only, but including plated through-holes.

3.1.6 System Slot Board Signal Stub Length

The System Slot **shall** have signal lengths less than or equal to 63.5 mm (2.5 inches) for 32-bit or 64-bit boards.

The System Slot **may** have two PCI loads on each signal on a PCI backplane segment to accommodate practical implementations of PCI-based CPU designs. If an additional load is added on the System Slot board, only one stub termination resistor per PCI signal **shall** be required as defined in Section 3.1.3.

On the system slot, when two PCI loads are used, the signal **shall** be routed linearly from the connector, to the first load and then to the second load. The stub connecting to the first load **shall** be less than 0.5inch.

3.1.7 Peripheral Board PCI Clock Signal Length

On Peripheral boards, the PCI clock signal length **shall** be 63.5 mm ± 2.54 mm (2.5 inches ±0.1 inches), and **shall** drive only one load on the board.

3.1.8 Pull-Up Location

Pull-up resistors required by the PCI specification **shall** be located on the System Slot board. Table 5 provides values for both 5 V and 3.3 V signaling environments. All values assume nine loads (two on the System Slot board plus one each on seven other boards) and ± 5% resistor values. The pull-up resistor, for those signals requiring a pull-up, **shall** be placed on the in-board side of the

stub termination resistor. The stub length for the pull-up resistor **shall** be less than 0.5inch, with the stub length being considered as a part of the total trace length.

A System Slot board that supports both signaling modes **shall** be designed to support the appropriate pull-up value for the signaling environment that it is operating in. A board that may function as either a System Slot board or Peripheral board **shall not** have the pull-up resistors connected when in Peripheral board function.

Table 5. Pull-up Resistor Values.

Signaling Voltage	Min.	Nominal	Max.	Units
5 V	-5%	1.0	+5%	KΩ
3.3 V	-5%	2.7	+5%	KΩ

In addition to the pull-ups required on control signals, ALL System Slot boards **shall** provide pull-up resistors for the 64-bit data path expansion signals, AD[63::32], C/BE[7::4]#, and PAR64.

The System Slot board **shall** provide a pull-up resistor for the REQ64# and ACK64# signals even if the System Slot board does not use these signals, as in the case of a 32-bit System Slot board. The above requirements accommodate 64-bit peripheral boards used in platforms with 32-bit or 64-bit System Slot Boards. The pull-up resistor also prevents floating REQ64# or ACK64# signals on 64-bit boards. Refer to section 3.4 for additional details on 64-bit signaling.

Each peripheral board using GNT# **shall** have a 100 KΩ pull-up resistor to prevent a floating input if GNT# is not being driven by the System Slot board designed prior to the 3.0 revision of this specification.

See also Sections 3.2.7.4 and 3.2.7.5 for details of pull-up for Legacy IDE Interrupt and System Enumeration related signals.

3.1.9 Board Connector Shield Requirements

The J1 and J2 connectors **shall** load a shield at row F on the board. This shield provides a low impedance return path for logic ground between the board and the CompactPCI backplane. Boards that do not use this shield are not compliant and are not guaranteed to work in all CompactPCI system topologies.

The Z row shield option that is provided for in the IEC-61076 connector is not required for CompactPCI boards and **shall** not be loaded if it protrudes into the interboard separation plane.

3.2 Backplane Design Rules

CompactPCI defines a backplane environment that **may** have up to eight slots at 33MHz. 66Mhz backplanes **may** have up to five slots. See Section 3.5.3 for 66Mhz design rules.

One slot, the System Slot, provides the clocking, arbitration, configuration, and interrupt processing for the other seven slots. Fewer slots may be provided in a CompactPCI backplane, but the following sections assume that a maximum configuration is employed in a linear topology using 20.32 mm (0.8 inch) board center-to-center spacing with the System Slot located on either end of the bus segment. Any other topology **shall** be simulated or otherwise verified to ensure compliance to the PCI specification.

It is possible to design a backplane capable of both 33Mhz and 66Mhz operation. See Section 3.5.3 for 66Mhz design rules. M66EN **shall** be grounded on all slots for backplanes with more than five slots.

Backplanes **shall** provide separate power planes for 3.3 V, 5 V, and ground. If V(I/O) is configurable as 3.3 V or 5 V, then a separate power plane **shall** be dedicated for V(I/O).

3.2.1 Characteristic Impedance

Backplanes **shall** be fabricated to provide CompactPCI signal traces within the characteristic impedance range given in Table 6.

Table 6. Backplane Characteristics.

Parameter	Min.	Nominal	Max.	Units	Comment
Z_0	-10%	65	+10%	ohms	PCB without connectors or boards installed, but including plated through-holes

3.2.2 Eight-Slot Backplane Termination

System simulation has shown that when using the strongest PCI buffer allowed (refer to the PCI specification V-I curves) and with a lightly loaded eight-slot backplane configuration with the System Slot and its adjacent Peripheral Slot loaded (only two boards), that the 10 ns maximum propagation delay for PCI signals is violated.

For this specific system configuration, fast Schottky diode signal termination (For example: see Texas Instruments 74S1053 diode array) **shall** be added to the end of the backplane furthest from the System Slot on all bused PCI signals, as illustrated in Figure 3. The diodes **may** be added directly to the backplane or via

a diode termination board in the slot furthest away from the System Slot. If used, the diodes **shall** be as near as practical to the end of the net for each PCI signal.

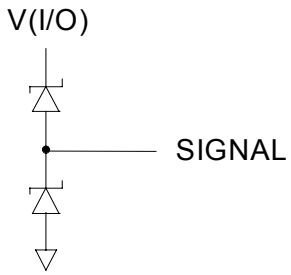


Figure 3. PCI Signal Termination.

3.2.3 Signaling Environment

Each CompactPCI backplane provides for either a 5 V or 3.3 V signaling environment. PCI allows for two types of buffer interfaces for interboard connection. 5 V signaling will generally be used for early systems. A gradual shift to 3.3 V will occur as the semiconductor industry shifts to the lower power interface for speed and power dissipation reasons. The V(I/O) power pins on the connector are used to power the buffers on the peripheral boards, allowing a card to be designed to work in either interface.

CompactPCI allows for this dual interface scheme by providing a unique backplane connector coding plug for either system. The CompactPCI backplane may be either a fixed signaling environment backplane (e.g., 5 V only) or may be configurable. In any case, when configured for 5 V operation, the 5 V coding plug (Brilliant Blue) **shall** be used, and when configured for 3.3 V operation, the 3.3 V coding plug (Cadmium Yellow) **shall** be installed in the backplane connector.

With the above mechanism, boards that have the coding plug matching the backplane can be inserted. The opposite technology board is likewise inhibited from being inserted. Boards that are either 3.3 V or 5 V **shall** not have a coding plug and therefore can be inserted in either system. Refer to Sections 5.6 and 5.7 for details.

3.2.4 IDSEL Assignment

The PCI signal IDSEL is used to provide unique access to each logical slot for configuration purposes. By connecting one of the address lines AD31 through AD25 to each board's IDSEL pin (J1:B9), a unique address for each board is provided during configuration cycles. **Table 7** illustrates the assignment of address lines to each board's IDSEL pin. The backplane **shall** make the connection to IDSEL at each logical slot's connector with minimum trace length.

One additional PCI device on the CompactPCI bus segment is allowed on the System Slot board. This device **may** be selected using lower ADxx lines in the range of AD11 to AD24.

3.2.5 REQ#/GNT# Assignment

The System Slot interfaces to seven pairs of REQx#/GNTx# pins called REQ0#-REQ6# and GNT0#-GNT6#. Each Peripheral Board interfaces to one pair of REQx#/GNTx# signals using pins called REQ# (J1:A6) and GNT# (J1:E5). **Table 7** lists the assignment of request/grant signals to each board's REQ# and GNT# pins.

The System Slot on any given CompactPCI backplane segment **shall** support the full complement of REQ#/GNT# signals.

The System Slot board **shall** support seven pairs of REQx#/GNTx# signals.

Table 7. System to Logical Slot Signal Assignments.

Signal	Connector:Pin	Signal	Connector:Pin
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 2**	
AD31	P1:E6	IDSEL(1)	P1:B9
REQ0#	P1:A6	REQ#	P1:A6
GNT0#	P1:E5	GNT#	P1:E5
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 3**	
AD30	P1:A7	IDSEL(1)	P1:B9
REQ1#	P2:C1	REQ#	P1:A6
GNT1#	P2:D1	GNT#	P1:E5
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 4**	
AD29	P1:B7	IDSEL(1)	P1:B9
REQ2#	P2:E1	REQ#	P1:A6
GNT2#	P2:D2	GNT#	P1:E5
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 5**	
AD28	P1:C7	IDSEL(1)	P1:B9
REQ3#	P2:E2	REQ#	P1:A6
GNT3#	P2:C3	GNT#	P1:E5
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 6**	
AD27	P1:E7	IDSEL(1)	P1:B9
REQ4#	P2:D3	REQ#	P1:A6
GNT4#	P2:E3	GNT#	P1:E5
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 7**	
AD26	P1:A8	IDSEL(1)	P1:B9
REQ5#	P2:D15	REQ#	P1:A6
GNT5#	P2:E15	GNT#	P1:E5
System Slot (△), Logical Slot 1		**Peripheral Slot (◯), Logical Slot 8**	
AD25	P1:D8	IDSEL(1)	P1:B9
REQ6#	P2:D17	REQ#	P1:A6
GNT6#	P2:E17	GNT#	P1:E5

Notes:

(2) (1) The IDSEL signal at each slot **shall** be connected with minimal trace length at the slot that is intended. For example, at logical slot 6, IDSEL **shall** be connected to AD27 with minimal trace length.

3.2.6 PCI Interrupt Binding

Interrupt binding of the BIOS setup program **shall** require backplane assignments from the System Slot interrupt pins INTA#-INTD# to the logical board slot interrupts as defined in Table 8.

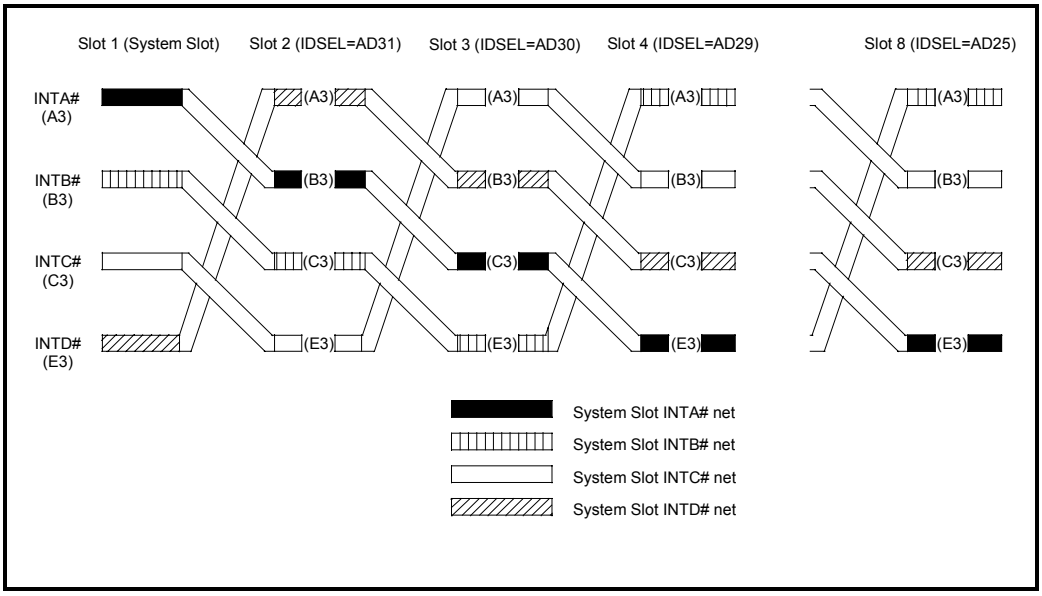
Backplane assignments rotate through logical board slots to provide a unique PCI interrupt to each board for the first four PCI connectors (assuming that each board drives just its INTA# signal). Rotating interrupt assignments allows multiple PCI peripherals that drive only INTA# in order to utilize a different interrupt on the System Slot board without the need to share an interrupt with another PCI interface. Since multi-function PCI devices are allowed to drive more than one interrupt, shared interrupts may be required even within the first four board slots. In addition, the rotating pattern repeats itself after logical slot four, which also requires the sharing of an interrupt for slots that are four connectors apart (logical slots 2 and 6 for example).

The Interrupt assignments are consistent with the PCI-PCI Bridge Specification as defined by the PCI SIG. This is to allow PCI-PCI bridge technology on CPU boards between Bus 0 and CompactPCI.

Although PCI software device drivers are designed to allow sharing of interrupt signals, sharing an interrupt with another device can affect interrupt latency and is generally avoided where possible.

Please see Section 3.2.7.4 for interrupt support for legacy IDE devices.

Table 8. System to Logical Slot Interrupt Assignments.



3.2.7 CompactPCI Signal Additions

CompactPCI utilizes PCI signals as defined by the *PCI Local Bus Specification* with some additional signals. These additional signals do not affect the PCI signals but **may** enhance system operation by providing push button reset, power supply status, System Slot identification, geographic addressing, system management, and legacy IDE interrupt support features.

3.2.7.1 Push Button Reset (PRST#)

PRST# **may** be used in a CompactPCI system to reset the System Slot board, which in turn would reset the rest of the system using the PCI RST# signal. PRST# is an active low true TTL signal generated by a switch closure or an open-collector driver. It is the responsibility of the System Slot board receiving PRST# to debounce it as required. The System Slot board **shall** terminate PRST# with a minimum 1KΩ pullup resistor to V(I/O).

3.2.7.2 Power Supply Status (DEG#, FAL#)

Power sub-system status **may** be determined from two low true TTL power supply status signals available on backplanes utilizing modular power supplies implementing the optional DEG# and FAL# signals. The System Slot board **shall** terminate both signals with a minimum 1KΩ pullup resistor to V(I/O), even if the system board does not use these signals. Please see Section 3.2.8.2 for more information.

3.2.7.3 System Slot Identification (SYSEN#)

This pin is grounded on the CompactPCI backplane segment at the System Slot so the board **may** identify installation into the System Slot. This pin is not connected on the backplane for the remaining slots. Boards that sense this signal **shall** provide their own pull-up to V(I/O) and disable all System Slot functions, such as clock generation and bus arbitration when it is not installed in a System Slot.

3.2.7.4 Legacy IDE Interrupt Support

Two additional non-PCI interrupts, INTP and INTS, are defined for boards using legacy interrupts. Support of these interrupts is optional. INTP (pin D4) is used as a steerable interrupt which **may** be routed to any legacy ISA interrupt on the system master. The system master **shall** provide a way for the user to control the usage and routing of this interrupt, e.g. via the BIOS setup menu. After PCI Reset, this steerable interrupt **shall** be disabled on the system master and any peripheral board supporting this interrupt.

On legacy system masters, INTP **may** be hardwired to a single legacy ISA interrupt. This especially includes the option to use INTP as legacy IDE interrupt as proposed by former revisions of this specification.

INTP is an active high TTL signal and does not have the requirement of meeting the PCI electrical buffer characteristics. The System Slot board

shall provide a 1KΩ pullup to V(I/O), even if the System Slot board does not support this signal.

INTS (pin E4) **may** be used as serialized interrupt in compliance with the ”Serialized IRQ Support for PCI Systems” specification, Rev. 6.0, September 1995.

The system master **shall** provide a way for the user to control the usage and routing of this interrupt, e.g. via the BIOS setup menu. After PCI Reset, this serialized interrupt **shall** be disabled on the system master and any peripheral boards supporting the serialized IRQ protocol.

INTS is synchronous to the PCI clock and has the requirement of meeting the PCI electrical buffer characteristics. This line **shall** have a pull up resistor on the system slot board in accordance with Section 3.1.8 and a termination resistor in accordance with Section 3.1.3 on any board supporting this signal. The electrical characteristics and routing of the PCB trace **shall** comply with sections 3.1.4 through 3.1.7.

The support for INTP and INTS **shall** be clearly documented by the system slot and peripheral board vendors.

3.2.7.5 System Enumeration (ENUM#)

This low true TTL open-collector signal **shall** be driven by hot swap compatible boards after insertion and prior to removal. The System Master uses this interrupt signal to force software to interrogate all boards within the system for resource allocation regarding I/O, memory, and interrupt usage. The System Slot board **shall** terminate ENUM# with a pullup resistor as defined in Section 3.1.8. Different levels of hot swap capability are defined in the CompactPCI Hot Swap Specification regarding the ENUM# Signal. Consult the CompactPCI Hot Swap Specification for further details.

3.2.7.6 Geographic Addressing (GA[4..0])

For backplanes, if P2 is populated on a particular slot, then it **shall** support the GA[4..0] geographic addressing signals for unique slot identification. Boards that use geographical address signals GA[4..0] **shall** be pulled up with a 10.0 KΩ ±10% resistor.

For backplanes the physical slot address (GA[4..0]) **shall** be encoded on the backplane by grounding and leaving unconnected different combinations of pins at each connector. Physical slot addresses are defined by the physical slot number in Section 2.1. **Table 9** illustrates the physical slot number and its physical slot address defined by GA[4..0]. Physical slot “0” is reserved for future use. Geographical address “31” is the default address that results when a geographical address capable board is installed in a backplane slot that does not support geographical addressing.

Boards that support system management **may** use these signals to provide a unique address within the system. Refer to the pending CompactPCI System Management Specification for further information

Table 9. Physical Slot Addresses.

Physical Slot Number	GA[4] (J2-A22)	GA[3] (J2-B22)	GA[2] (J2-C22)	GA[1] (J2-D22)	GA[0] (J2-E22)
0(1)	GND	GND	GND	GND	GND
1	GND	GND	GND	GND	Open
2	GND	GND	GND	Open	GND
3	GND	GND	GND	Open	Open
4	GND	GND	Open	GND	GND
5	GND	GND	Open	GND	Open
6	GND	GND	Open	Open	GND
7	GND	GND	Open	Open	Open
8	GND	Open	GND	GND	GND
9	GND	Open	GND	GND	Open
10	GND	Open	GND	Open	GND
11	GND	Open	GND	Open	Open
12	GND	Open	Open	GND	GND
13	GND	Open	Open	GND	Open
14	GND	Open	Open	Open	GND
15	GND	Open	Open	Open	Open
16	Open	GND	GND	GND	GND
17	Open	GND	GND	GND	Open
18	Open	GND	GND	Open	GND
19	Open	GND	GND	Open	Open
20	Open	GND	Open	GND	GND
21	Open	GND	Open	GND	Open
22	Open	GND	Open	Open	GND
23	Open	GND	Open	Open	Open
24	Open	Open	GND	GND	GND
25	Open	Open	GND	GND	Open
26	Open	Open	GND	Open	GND
27	Open	Open	GND	Open	Open
28	Open	Open	Open	GND	GND
29	Open	Open	Open	GND	Open
30	Open	Open	Open	Open	GND
31	Open	Open	Open	Open	Open

Note:

(1) Physical slot number "0" is reserved for future use.

3.2.7.7 System management bus

Three pins, (IPMB_SCL, IPMB_SDA, IPMB_PWR), are defined on J1/P1 for incorporating system management features including board identification, environmental and voltage monitoring, etc.

Three pins, (ICMB_SCL, ICMB_SDA, ICMB_PWR), are reserved on J2/P2 for possible use by non-backplane bussed system management functions.

Refer to the PICMG 2.9*, CompactPCI System Management Specification* for further information.

The IPMB_PWR backplane traces **shall** have a current carrying capacity of at least 100 mA per slot.

3.2.8 Power Distribution

Power is distributed in a CompactPCI system by utilizing a backplane. Each backplane **shall** make provisions for the standard regulated direct current (DC) supply voltages in **Table 10** below.

Table 10. Power Specifications.

Mnemonic	Description	Nominal Value	Tolerance(2)	Max. Ripple (p-p)(3)
5 V	+5 VDC	5.0 V	+5%/-3%	50 mV(1)(4)
3.3 V	+3.3 VDC	3.3 V	+5%/-3%	50 mV(1)(4)
+12 V	+12 VDC	12.0 V	±5%	240 mV(1)(5)
-12 V	-12 VDC	-12.0 V	±5%	240 mV(1)(5)
V(I/O)	PCI I/O Buffer Voltage	5.0V or 3.3V	+5%/-3%	50mV(1)(4)
GND	Ground			

Note:

(1) Maximum ripple is very difficult to accurately measure and therefore requires good measurement techniques. Measurement should be made at 20 MHz bandwidth with a minimum length ground strap. Each CompactPCI slot must meet this specification.

(2) This specification is for power delivered to each slot and it includes both the power supply and the backplane tolerance.

(3) For ripple directly related to the line frequency, the maximum ripple shall be a maximum 10mV(p-p) for +12V and -12V and 5mV(p-p) for +5V and +3.3V

(4) Distribution between board and backplane: 20 mV for backplane; 30mV for board.

(5) Distribution between board and backplane: 96 mV for backplane; 144 mV for board.

3.2.8.1 External Power Connections

Power terminals **may** be located on the front or rear side of the backplane for external power sources. Several styles of high current printed circuit board terminals are available. At least one per supply voltage **shall** be provided.

3.2.8.2 In-Rack Power Connections

The *PICMG 2.11 Power Interface Specification* defines several methods for implementing In-rack modular power supplies. Previous versions of the core specification (PICMG 2.0) have referenced an IEC 603-2 (DIN 41612) style connector for modular power supplies, which is one of the referenced configurations in PICMG 2.11. For further details refer to *PICMG 2.11 Power Interface Specification*.

3.2.8.3 V(I/O) Current Carrying Capability

Backplanes **shall** be designed to provide an aggregate 4A minimum to each CompactPCI slot through that slot's V(I/O) pins. Boards **may** assume that up to 4A of current (at either 5V or 3.3V) is available through the V(I/O) pins at the connector. This requirement merely grants permission for boards to draw power from V(I/O) in addition to 5V and 3.3V power pins. Overall system power allocation is a system integration concern.

3.2.9 Power Decoupling

CompactPCI boards may utilize any of the voltages in **Table 10**. Without adequate power decoupling on the backplane for the 5 V and 3.3 V power, intermittent operation may result. The backplane has dedicated 5 V and 3.3 V power pins along with V(I/O) power pins. The V(I/O) power pins are connected to either 5 V or 3.3 V depending on if 5 V or 3.3 V backplane signals are being used. See Section 5.6.

All power voltages **shall** be decoupled to ground in such a manner as to provide for reasonable management of switching currents (di/dt). Low impedance power planes and connections to low equivalent series resistance (ESR) capacitors **should** be used. Even if a system does not use 3.3 or 5 V, the unused power pins **shall** be connected and decoupled to provide an additional AC return path. **Table 11** illustrates the bypass guidelines that **shall**, at a minimum, be used for each connector.

Table 11. Backplane Decoupling Recommendations.

Mnemonic	Description	Decoupling Capacitance	Voltage
5V	+5 VDC	44 µF ± 20% (1)	15 V min.
3.3V	+3.3 VDC	44 µF ± 20% (1)	10 V min.
V(I/O)	+5/3.3 VDC	44 µF ± 20% (1)	15 V min.
+12V	+12 VDC	15 µF ± 20%	35 V min.
-12V	-12 VDC	15 µF ± 20%	35 V min.

Note:

(1) Recommended decoupling capacitance per connector best distributed across the length of each connector.

3.2.10 Healthy *(Healthy#)*

This pin is reserved for use in hot swap systems. The backplane **SHALL** leave HEALTHY# open (not connected). This pin **SHALL** be bypassed on the backplane at each slot with a 0.01uF capacitor to maintain the AC shielding capability of the line. Additional requirements may apply to some Hot Swap platforms, refer to PICMG 2.1 for details.

3.3 33 MHz PCI Clock Distribution

The System Slot board **shall** provide clock signals for all PCI peripherals in the system, including devices on the System Slot board. Peripheral boards are provided clock signals via the CompactPCI backplane. A maximum skew of 2 ns **shall** be maintained across the system operating at 33 MHz between any two PCI devices at the clock input of the integrated circuits.

Clock skew is the difference between the maximum and minimum propagation delay of any PCI clock signal. There are two components that contribute to clock skew in a CompactPCI system:

1. Backplane Clock Skew. The CompactPCI backplane provides the distribution of clock signals for all of the board slots in the system. The differences in the trace routing and net topologies contribute to skew and also define the longest clock delay that **shall** be considered in the design of the system and still meet overall system clock skew requirements.
2. System Slot Board Clock Skew. This is the clock skew that **may** be attributed to the onboard routing differences (if any) of all of the PCI clocks as well as the skew specification for the type of integrated circuit driver used for clock distribu-

tion. The onboard clock routing **shall** be designed to complement the propagation delays of distributing the clock to a backplane and still meet overall system skew requirements.

3.3.1 Backplane Clock Routing Design Rules

CompactPCI backplanes **shall** be designed to provide a consistent environment for System Slot boards with regard to backplane clock routing. Design rules assume a linear backplane with the System Slot at one end of the bus segment and 20.32 mm (0.8 inch) connector spacing.

The System Slot provides 7 clock signals, which dedicates a unique clock to each slot. Correspondence between individual clock signals and physical slots is arbitrary.

Backplanes **shall** use these clock lines to provide a single clock line per slot. Clock lines **shall** not be shared. These clock lines **shall** be routed between 135 mm (5.3 inches) and 185 mm (7.3 inches) in length.

System Slot boards **shall** drive each of the 7 clock lines.

3.3.2 System Slot Board Clock Routing Design Rules

The System Slot clock distribution circuitry **shall** be designed to accommodate up to 1.2 ns of backplane skew (minimum vs. maximum number of slots and various loading configurations). The following design rules apply to clock distribution to backplane peripherals and local (onboard) PCI peripherals. See Section 3.1.3 for details of termination on System Slot Boards.

3.3.2.1 Clock Routing to Connector Clock Pins

The clock distribution circuitry on the System Slot **shall** provide a discrete clock signal to each of the CompactPCI connector pins defined as a PCI clock (CLK0, CLK1, CLK2, CLK3, CLK4, CLK5, CLK6). The routing of these signals **shall** be matched in length.

3.3.2.2 Clock Routing to Local PCI Peripherals

Any onboard PCI peripherals connected to the CompactPCI bus, including PCI to PCI bridges, **shall** be provided a clock that is delayed to accommodate the maximum propagation delay of the backplane clocks and still meet the 2 ns overall skew requirement of the PCI Specification. Up to 800 ps of skew is allowed for onboard clock distribution (including the clock buffer internal skew). The onboard clock signals **shall** be delayed beyond the clocks routed to the backplane (Section 3.3.2.1) to accommodate best and worst case backplane delays and the 63.5mm wire delay on the peripheral board.

3.4 64-Bit Design Rules

64-bit Peripheral boards must be configured correctly for the type of backplane environment that they are plugged into. This includes 64-bit Peripheral boards plugged into a system controlled by a 32-bit System Master as well as a 64-bit Peripheral board being plugged into a hot swap capable system. This revision of the CompactPCI specification differs from the PCI specification in the method that a Peripheral board determines the proper mode of operation.

The PCI Specification requires the following: On a 64-bit Peripheral board (32-bit Peripheral boards ignore REQ64#) REQ64# is sampled by the peripheral PCI device at the rising (trailing) edge of RST# to configure the upper 32-bit signal buffers for the type of system that the peripheral is installed into. If REQ64# is high, the 64-bit device is allowed to drive the upper 32-bits signals active to prevent these signals from floating. If REQ64# is sampled low, the device must configure the upper 32-bit signals for proper 64-bit operation.

CASE A: In CompactPCI, it is possible to have a 64-bit System Slot board plugged into a 32-bit only backplane, in which case it is required that any 64-bit Peripheral boards terminate the upper 32-bit signals for non 64-bit operation.

CASE B: It is also desirable to allow 64-bit Peripheral boards to communicate with each other at 64-bits when in a 64-bit backplane controlled by a 32-bit System Slot board. It is also desirable to allow the backplane to contain a mix of 32-bit and 64-bit slots.

CASE C: In a hot swap system, a board must configure itself because the time for a system reset has long passed and the board is being installed in an operating backplane environment with PCI transactions occurring.

To allow boards to self configure for 64-bit operation, pin B5 of P2 is defined as 64EN# and is GROUND in 64-bit backplanes and is left unconnected in 32-bit backplanes. This signal is then used by onboard circuitry to self-configure during RST#.

64EN# may be used in different ways to configure the local device. These include, but are not limited to, the following implementations:

a) Using 64EN# to drive the devices REQ64# signal during local reset by decoupling the backplane REQ64# from the device during reset. After reset, the backplane REQ64# is then connected to the device for normal 64-bit handshake operation. In all cases, normal electrical operation of REQ64# **shall** be maintained after reset. See Figure 4 below for an example of a possible circuit topology.

b) A 64-bit device may directly sample 64EN# during local reset to configure for 32- or 64-bit operation.

c) 64EN# may be used as part of an EEPROM serial pre-load mechanism to configure a 64-bit device for proper operation.

64-bit Peripheral boards **shall** use 64EN# to self-configure. Using the state of REQ64# at the trailing edge of RST# is no longer allowed. With the requirements given in this revision of the CompactPCI Specification, 64-bit capability is no longer an overall platform attribute. 64-bit capability can be determined on a slot by slot basis.

The following circuit topology shows a FET in series with the backplane REQ64# and the devices REQ64# pin. During reset, the FET is OFF, and the resistance to the 64EN# pin configures the device at the rising edge of reset. When RST# is de-asserted, the FET is enabled and REQ64# is allowed to function in it's normal mode (As defined in PCI Specification 2.1).

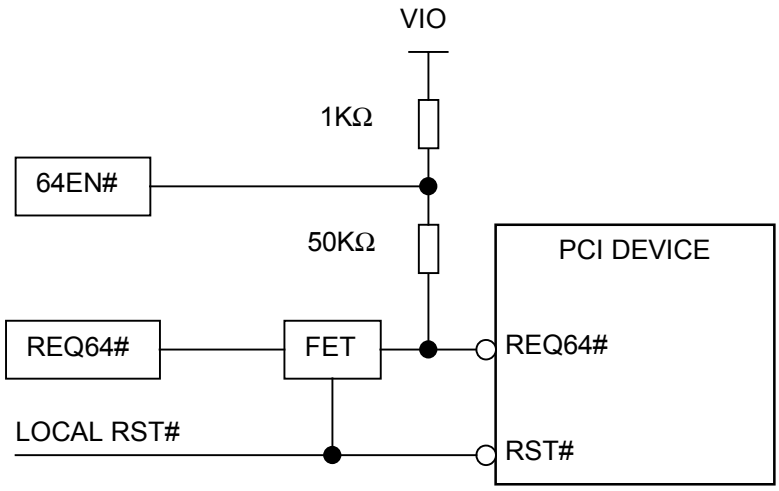


Figure 4. Local 64 Bit Initialization

To allow for the addition of the REQ64# series FET, the FET must not exceed the following parameters:

ON resistance: 5-10Ω typical

The capacitance of the FET circuit must be isolated from ground. One method of accomplishing isolation of the FET capacitance is to use a discrete 3-Terminal FET, with the device's gate driven through a high valued resistor.

The FET **may** replace the 10Ω *CompactPCI* ® stub isolation resistor, but the circuit topology must provide the equivalent stub isolation of a non-FET implementation. Refer to the CompactPCI Hot Swap Specification (PCIMG 2.1 R1.0) for details of the hot swap circuit analysis.

3.5 66 MHz Electrical Requirements

This section documents the additional requirements for 66 MHz operation. 33 MHz design rules apply for features not specifically called out in this section.

3.5.1 66 MHz Board Design Rules

On 66 MHz Peripheral boards, the PCI clock signal length **shall** be 63.5 mm ±1 mm (2.5 inches ±0.04 inches), and **shall** drive only one load on the board. Inner layer stripline construction **shall** be used for all clock lines in order to equalize delays.

3.5.2 66 MHz System Board Design Rules

On 66MHz System Slot Boards only one PCI load **shall** be allowed.

3.5.3 66MHz Backplane Design Rules

66 MHz CompactPCI defines a backplane environment that **may** have up to five slots.

One slot, the System Slot, provides the clocking, arbitration, configuration, and interrupt processing for the other four slots. Fewer slots may be provided in a CompactPCI backplane, but the following sections assume that a maximum configuration is employed in a linear topology using 20.32 mm (0.8 inch) board center-to-center spacing with the System Slot located on either end of the bus segment. Any other topology **shall** be simulated or otherwise verified to ensure compliance to the PCI specification.

M66EN, the 66Mhz Enabling Line, **shall** be bussed to all slots in 66Mhz backplanes.

Backplanes **shall** provide separate power planes for 3.3 V, 5 V, and ground. V(I/O) **shall** always be configured as 3.3V.

3.5.4 66MHz PCI Clock Distribution

The System Slot board **shall** provide clock signals for all PCI peripherals in the system, including the device on the System Slot board. Peripheral boards are provided clock signals via the CompactPCI backplane. A maximum skew of 1 ns **shall** be maintained across the system operating at 66 MHz between any two PCI devices at the clock input of the integrated circuits.

Clock skew is the difference between the maximum and minimum propagation delay of any PCI clock signal. There are two components that contribute to clock skew in a CompactPCI system:

1. Backplane Clock Skew. The CompactPCI backplane provides the distribution of clock signals for all of the board slots in the system. The slight differences in the

trace routing and net topologies contribute to skew and also define the longest clock delay that **shall** be considered in the design of the system and still meet overall system clock skew requirements.

2. System Slot Board Clock Skew. This is the clock skew that **may** be attributed to the onboard routing differences (if any) of all of the PCI clocks as well as the skew specification for the type of integrated circuit driver used for clock distribution. The onboard clock routing **shall** be designed to complement the propagation delays of distributing the clock to a backplane and still meet overall system skew requirements. A System Slot board designed for both 33 MHz and 66 MHz operation **shall** be designed with consideration for the different clock environments that it may operate in.

3.5.4.1 66 MHz backplane clock routing design rules

66 MHz systems require only 4 Peripheral Slot clocks to be connected. Correspondence between individual clock signals and physical slots is arbitrary.

Backplanes **shall** use these clock lines to provide a single clock line per slot. Clock lines **shall** not be shared. These clock lines **shall** be routed to 160mm ±1mm (6.300 inches ± 0.04) in length.

Inner layer stripline construction **shall** be used for all clock lines in order to equalize delays. Vias **shall** not be used to route any backplane clock lines.

3.5.5 66 MHz System Slot Board Clock Routing Design Rules

The System Slot clock distribution circuitry **shall** be designed to accommodate up to 200 ps of backplane and peripheral board skew. The following design rules apply to clock distribution to backplane peripherals and local (onboard) PCI peripherals.

3.5.5.1 Clock Routing to Connector Clock Pins

The clock distribution circuitry on the System Slot **shall** provide a discrete clock signal to each of the CompactPCI connector pins defined as a PCI clock (CLK0, CLK1, CLK2, CLK3, CLK4, CLK5, and CLK6). The routing of these signals **shall** be matched in length.

3.5.5.2 Clock Routing to Local PCI Peripherals

Any onboard PCI peripherals connected to the CompactPCI bus, including PCI to PCI bridges, **shall** be provided a clock that is delayed to accommodate the maximum propagation delay of the backplane clocks and still meet the 1 ns overall skew requirement. Up to 800 ps of skew is allowed for onboard clock distribution (including the clock buffer internal skew). The onboard clock signals **shall** be delayed beyond the clocks routed

to the backplane (Section 3.5.5.1) to accommodate best and worst case backplane delays and the 63.5mm wire delay on the peripheral board.

3.5.6 66 MHz Hot Swap

66MHz host silicon is not typically designed to dynamically switch between 33MHz and 66MHz operation. Because of this, hot swapping 33MHz peripherals into an operating 66MHz backplane is not allowed, unless the host silicon supports dynamic frequency change.

Removing a 33MHz peripheral from, what would otherwise be, a 66MHz platform is also not allowed, unless the host silicon continues to operate at 33MHz, or the host silicon supports dynamic frequency change.

3.6 System and Board Grounding

3.6.1 Board Front Panel Grounding Requirements

CompactPCI boards **should** utilize metalized shell front panel connectors for EMI/RFI protection. The shell **should** be electrically connected to the front panel through a low impedance path.

The following practice is prescribed for CompactPCI:

a) The front panel **shall** be connected to frame ground and isolated from logic ground.

b) CompactPCI boards **should** provide a mechanism to connect frame ground (on front panel) through a low impedance path to logic ground used on board. This will allow for flexibility in system integration for applications with differing grounding practices.

3.6.2 Backplane Grounding Requirements

Backplanes **shall** provide isolation between frame ground and logic ground. CompactPCI Backplanes **should** provide a configurable method of connecting frame ground to logic ground on the backplane. The intent of this is to allow the systems integrator the option to configure the grounding scheme as needed.

3.7 CompactPCI Buffer Models

The CompactPCI simulation V-I curve assumptions are provided in Appendix A for reference. Both 5V and 3.3V buffer models are provided. Note that all 66 MHz simulation assumes 3.3V buffers only. 33 MHz environments have been simulated with 5V, 3.3V and Universal buffer models.

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4 Mechanical Requirements

4.1 Board Requirements

CompactPCI defines two board sizes, 3U and 6U.

4.1.1 3U Boards

3U boards are 100 mm by 160 mm. The PCB is 1.6 ±0.2 mm thick. A 2 mm (IEC-61076-4-101) connector is used for interfacing to the CompactPCI bus segment. **Figure 6** illustrates the 3U board dimensions and connector location. 32-bit PCI is implemented on J1. J2 **may** be used for 64-bit PCI signaling, rear-panel I/O, or System Slot functions.

Note that row Z is not present on connectors J1 and J2 used on system or peripheral boards. Refer to IEC-61076-4-101 documentation for details.

4.1.2 6U Boards

6U boards are 233.35 mm by 160 mm. Figure 7 illustrates the 6U board dimensions and connector locations J1, J2, J3, J4 and J5. 32-bit PCI is implemented on J1. J2 is used for 64-bit PCI signaling, rear-panel I/O, or System Slot functions. J3, J4 and J5 **may** be used for rear-panel I/O.

Rear-panel I/O **may** be defined by the user and/or utilize PICMG specifications. Contact PICMG for copies of these specifications.

Note that row Z is not present on connectors J1 and J2 used on system or peripheral boards. Refer to IEC-61076-4-101 documentation for details.

4.1.3 Rear-panel I/O Boards

Rear-panel I/O boards may be either 3U (100 mm) or 6U (233.35 mm) in height and **shall** be 80 mm in depth for standard applications.

Figure 9 and Figure 10 illustrate 3U and 6U respectively, 80 mm representative rear-panel I/O board defined by IEEE 1101.11. Other depths as defined by IEEE 1101.11 are allowed depending on the application requirements. Refer to IEEE 1101.11 for further details. Since rear panel I/O is not available on J1, and therefore rear panel I/O necessitates additional connectors, these implementations **shall** be keyed to conform to the PICMG 2.10, Keying of CompactPCI Boards and Backplanes specification. The keying combination used on the rear panel I/O module **shall** match that used on the corresponding front panel.

4.1.4 ESD Discharge Strip

All boards **shall** implement features for ESD protection defined by IEEE 1101.10 and IEEE1101.11. The minimum ESD requirement for a board shall be a discharge strip located along both sides of the bottom edge of the board.

Figure 8 and Figure 11 shows the implementation for a front plug-in board and a rear panel I/O board respectively.

When a board is inserted into an enclosure, the ESD strip connects with an ESD clip on the cardguide which is connected to chassis ground, see 4.1.5. The ESD strip is separated into three segments to achieve a "controlled discharge". The first segment is connected to the front panel through a 10M**Ω** resistance to discharge any built up static from the board or user. The resistor is used to limit the amount of discharge current. The second segment discharges the board's ground planes as it is inserted further into the cardguide; again through a 10 M**Ω** resistance. The final third segment has a direct connection to the front panel. This provides a discharge path as the backplane connectors engage and when the board comes to rest after being completely installed. The third segment also provides a discharge path from the front panel to chassis ground when the entire system is assembled making it safe for handling and operation.

The level of ESD protection required depends upon the environment. For example, humans in dry ambient conditions can generate ESD potentials of over 20 kV. Use of an ESD wrist strap connected to chassis ground will limit the maximum potential to well below 2.5 kV. Other standard ESD reduction techniques such as natural-fiber wool apparel for service uniforms, minimum 35% RH operating environments, conductive mats or flooring, etc, are also helpful. For the discharge circuitry to be effective, no arc-over must occur across the resistor nor to surrounding components or circuitry. This implies (1) the breakover potential of the 10 M**Ω** discharge resistance must exceed the expected ESD potential buildup, and (2) the clearance area between the discharge circuitry and surrounding components or circuitry must be adequate to prevent arc-over. Discharge resistors that can tolerate high voltage levels are physically large. Fortunately, the breakdown voltage of resistors in series is additive and stray capacitance is sufficient to equalize the potential across each resistor. So if ***N*** resistors is used in series, of 10M**Ω**/***N*****Ω** resistance, the total breakdown voltage to ***N*** times the single resistor value.

4.1.5 ESD Clip

The ESD cardguide clip contacts the board edge as the board is inserted in the system and provides a path for ESD energy on the board to be discharged into the chassis. An ESD clip **shall** be provided in the lower card guide. The location of this clip **shall** be 35mm ± 5mm (1.38 inches ± 0.2 inches)

from the front attachment plane as shown in Figure 5. Note, this dimension is tighter than the location defined in IEEE 1101.10. These dimensions **shall** apply to both front and rear card guides.

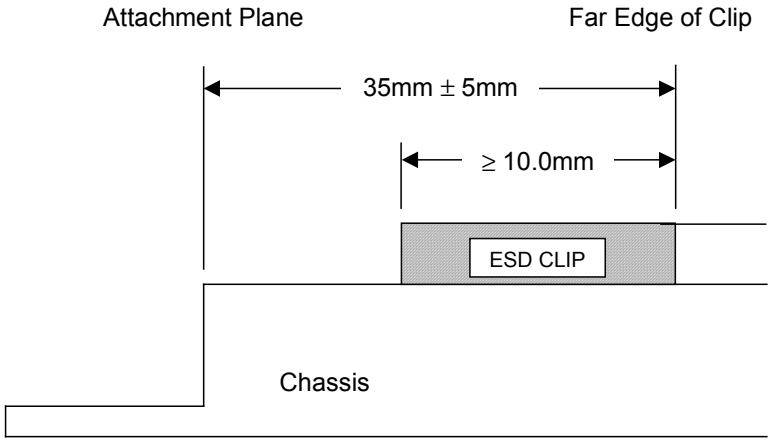


Figure 5. ESD Clip Location

4.1.6 Cross Sectional View

Figure 12 provides a cross sectional view illustrating the relationship between the front panel, board, connectors, and backplane. Refer to IEEE 1101.1 and IEEE 1101.10 (EMC) for additional details. Note that the top connector shield (component side) **shall** be installed to meet the electrical requirements. The bottom connector shield (back side) **may** be installed if it does not protrude into the interboard separation plane.

4.1.7 Component Outline and Warpage

Component outline and warpage is shown Figure 13. The sum of the component height/lead lengths and warpage (bow and twist) **shall** remain within the boundaries specified by the interboard separation planes. See IEEE1101.1 and IEEE 1101.10 for additional details.

4.1.8 Solder Side Cover

A protective solder side cover may be required to prevent damage of backside components when boards are installed/extracted from the subrack. All boards having backside components or through-hole pins **should** provide a means for mounting a protective cover. All such boards **should** be equipped with a solder side cover. The mounting holes for an IEEE 1101.10 compliant protective cover **should** be used, see Figure 6, Figure 7,

Figure **9** and Figure 10.

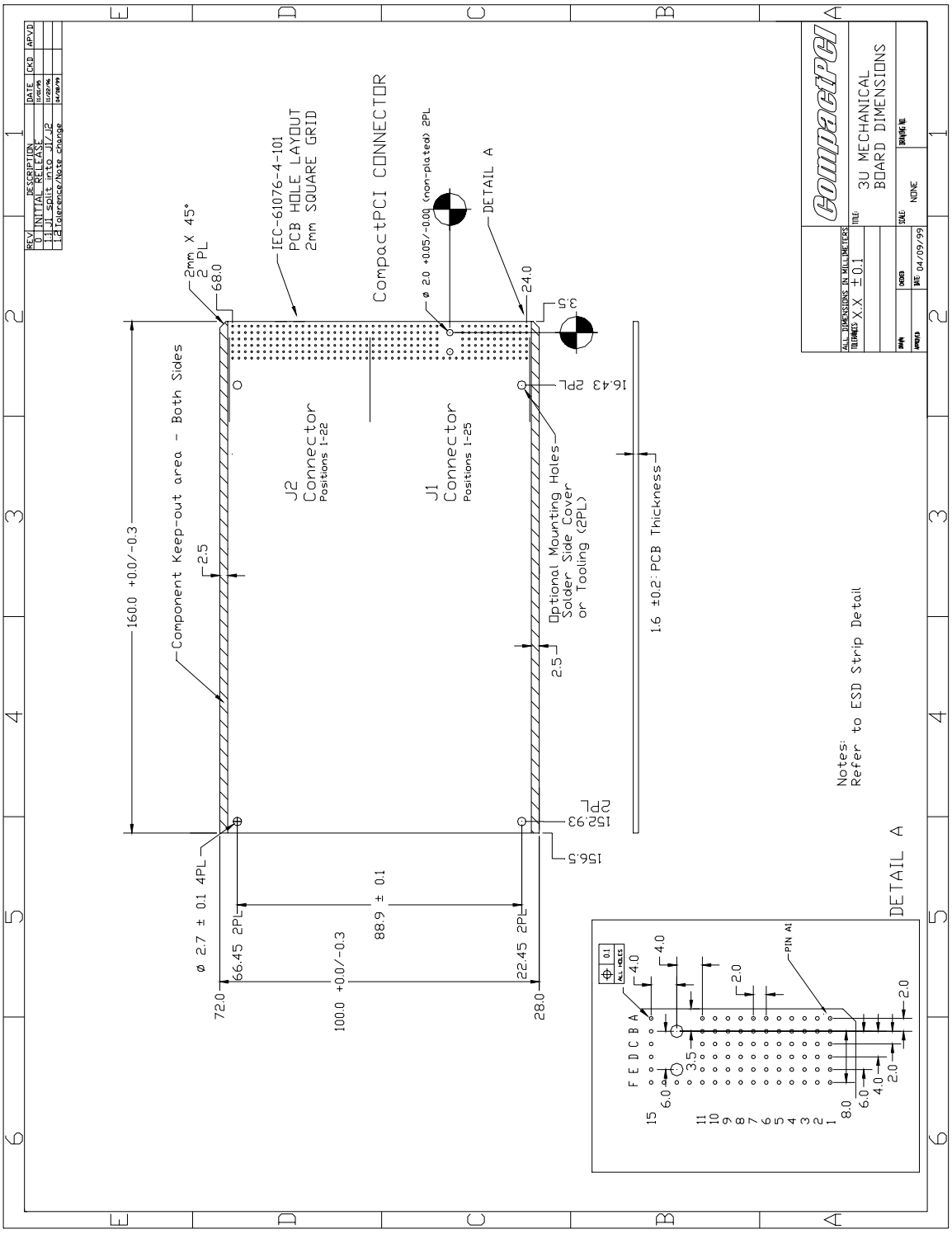


Figure 6. 3U Board.

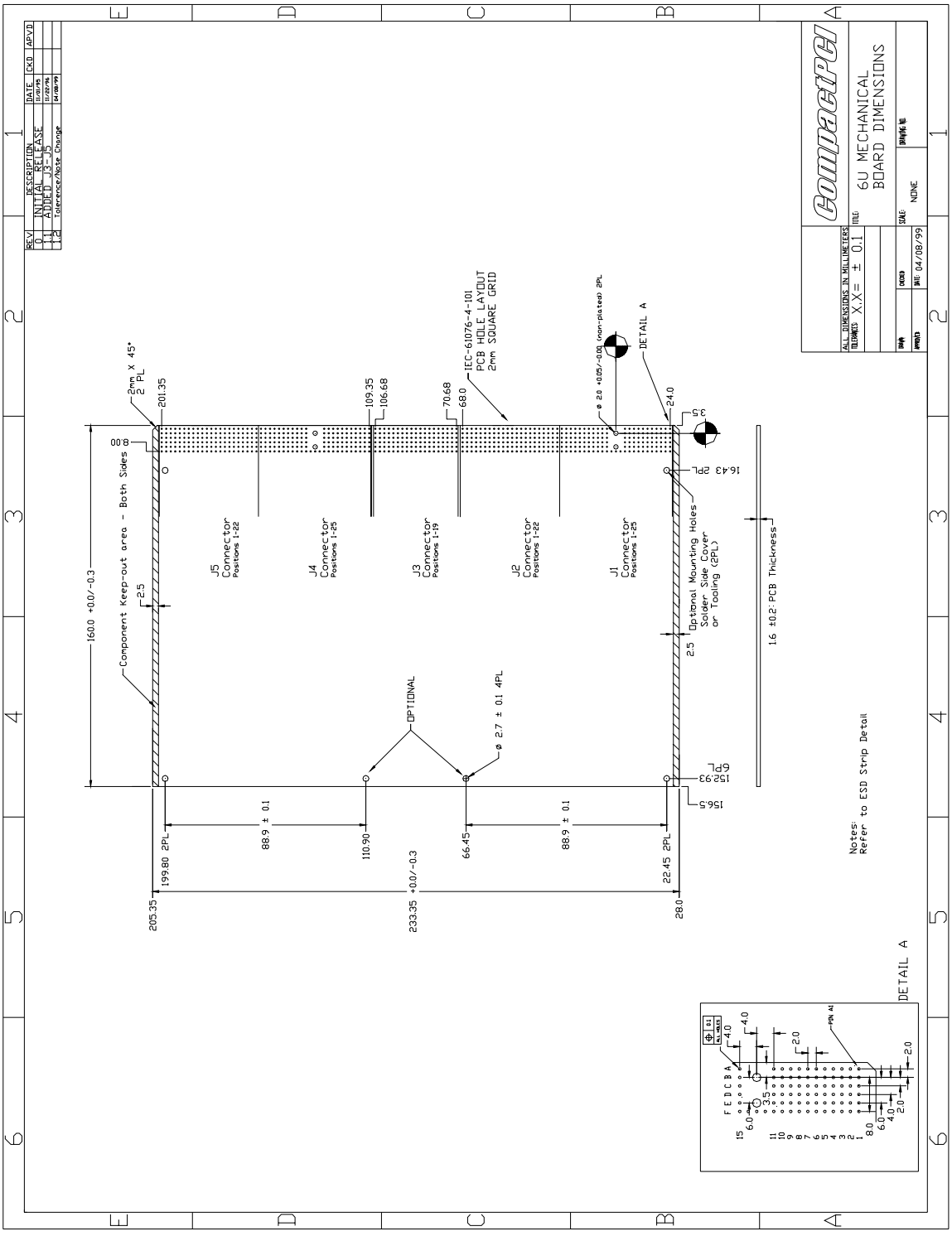


Figure 7. 6U Board.

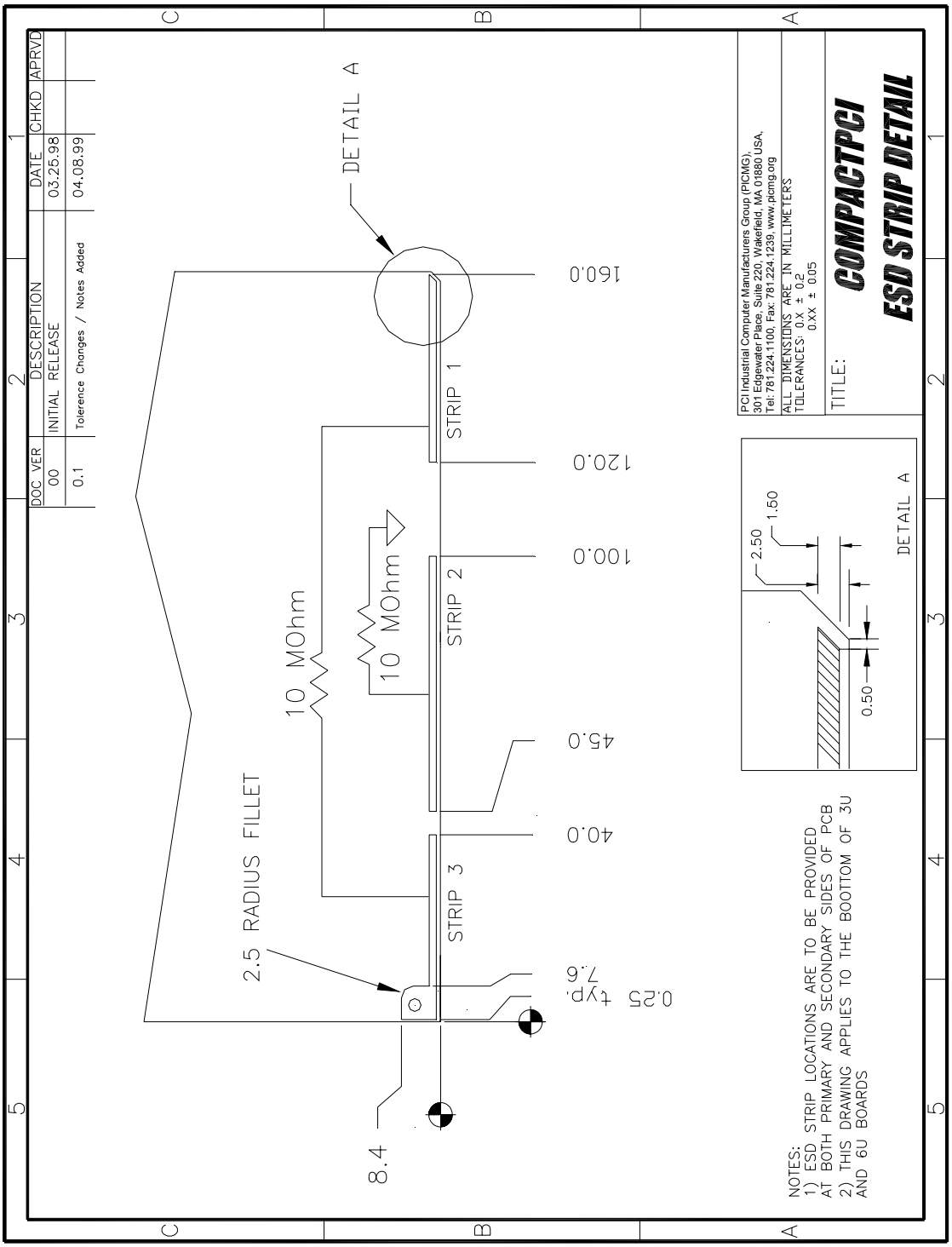


Figure 8. Front Side Board ESD Dimensions

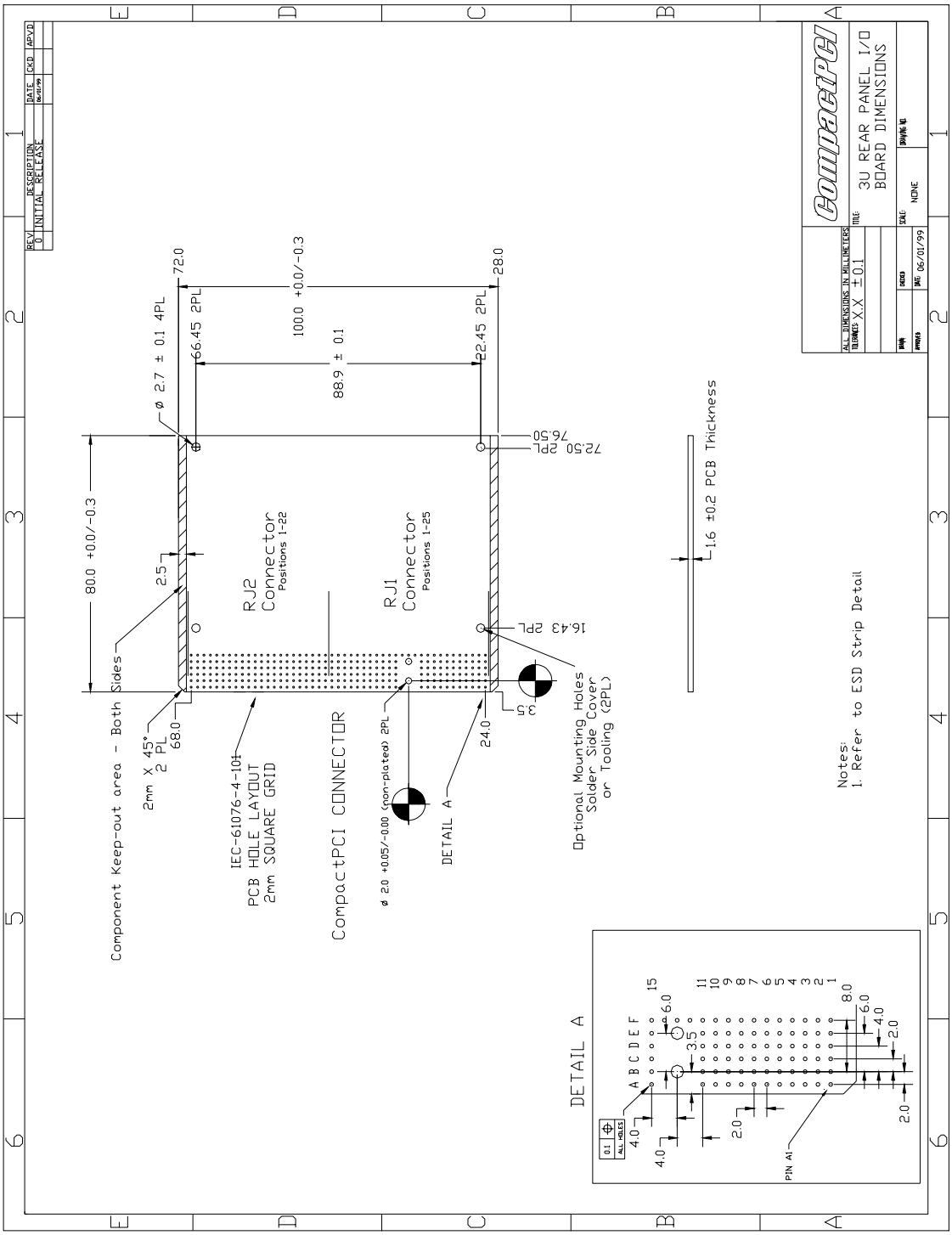


Figure 9. 3U Rear-Panel I/O Board Dimensions

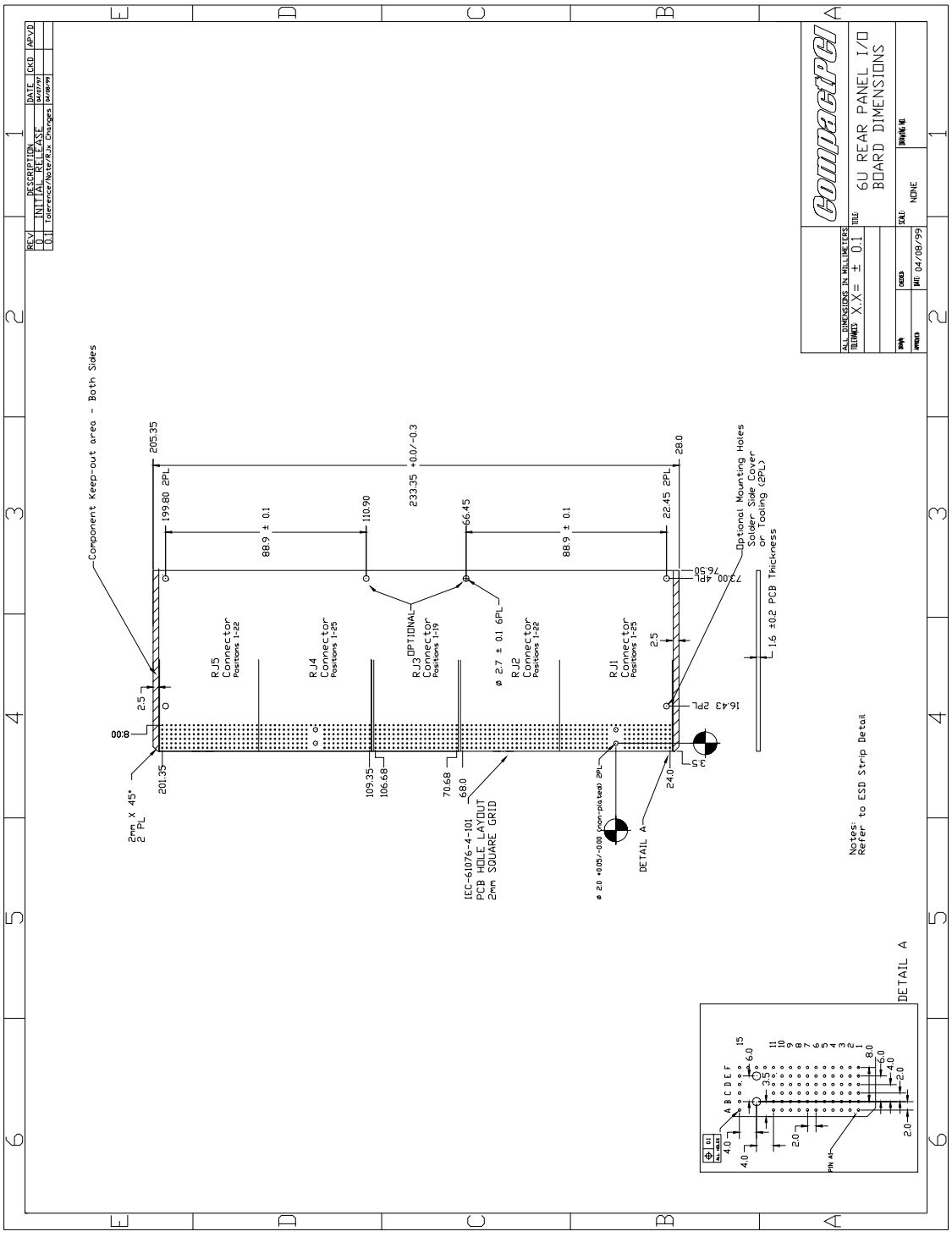


Figure 10. 6U Rear Panel I/O Board Dimensions

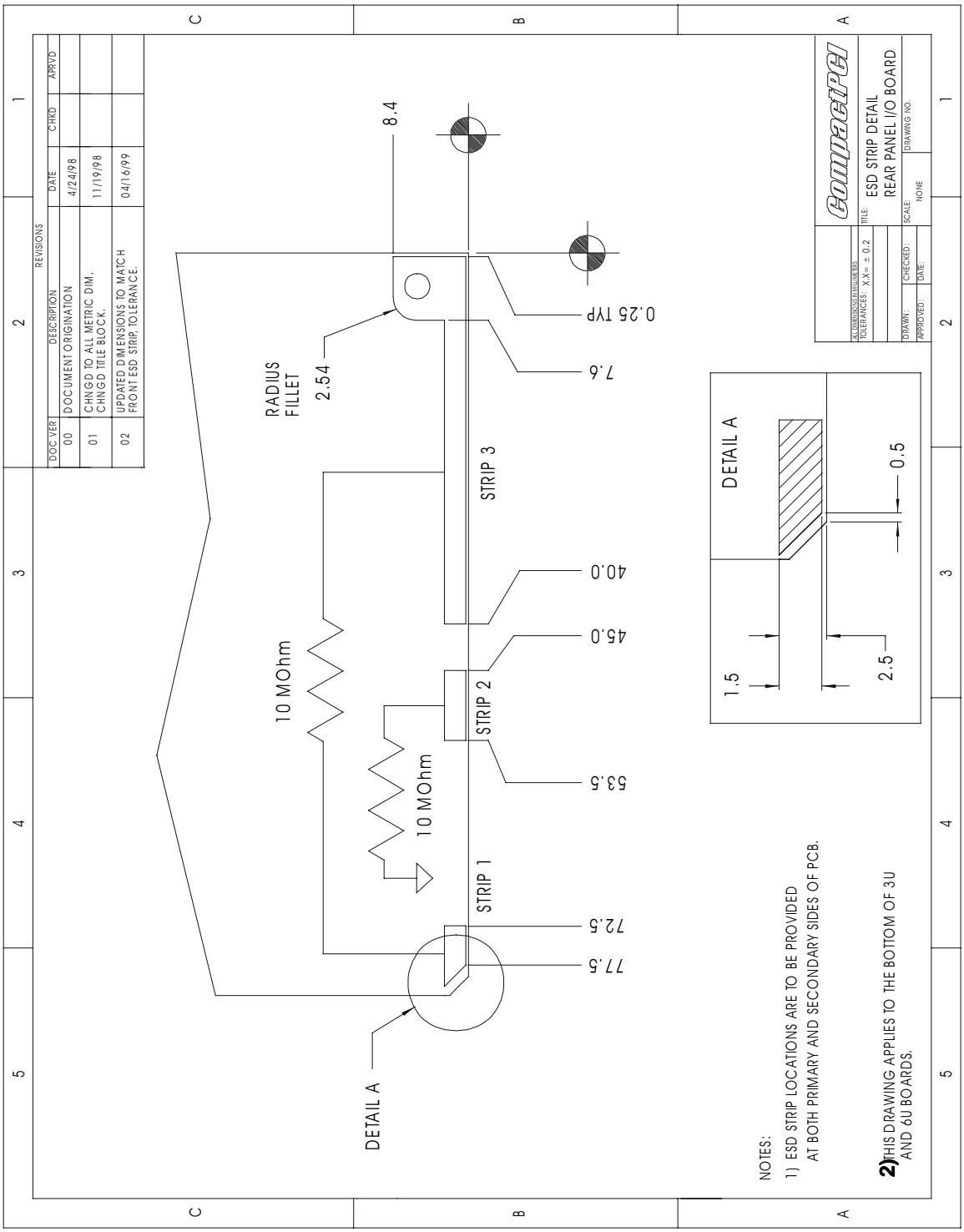


Figure 11. Rear Panel I/O ESD Dimensions

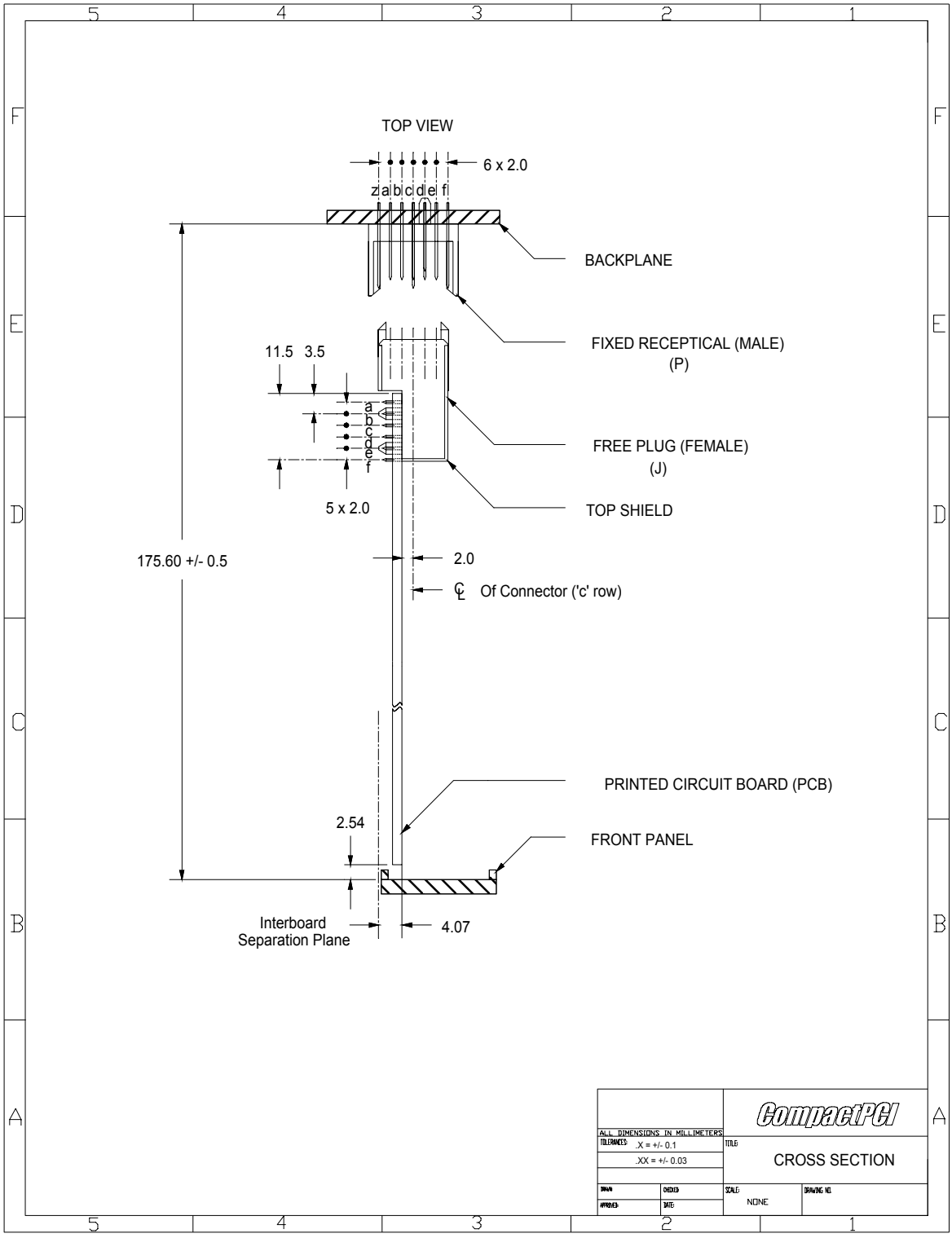


Figure 12. Cross Sectional Board, Connector, Backplane and Front Panel View.

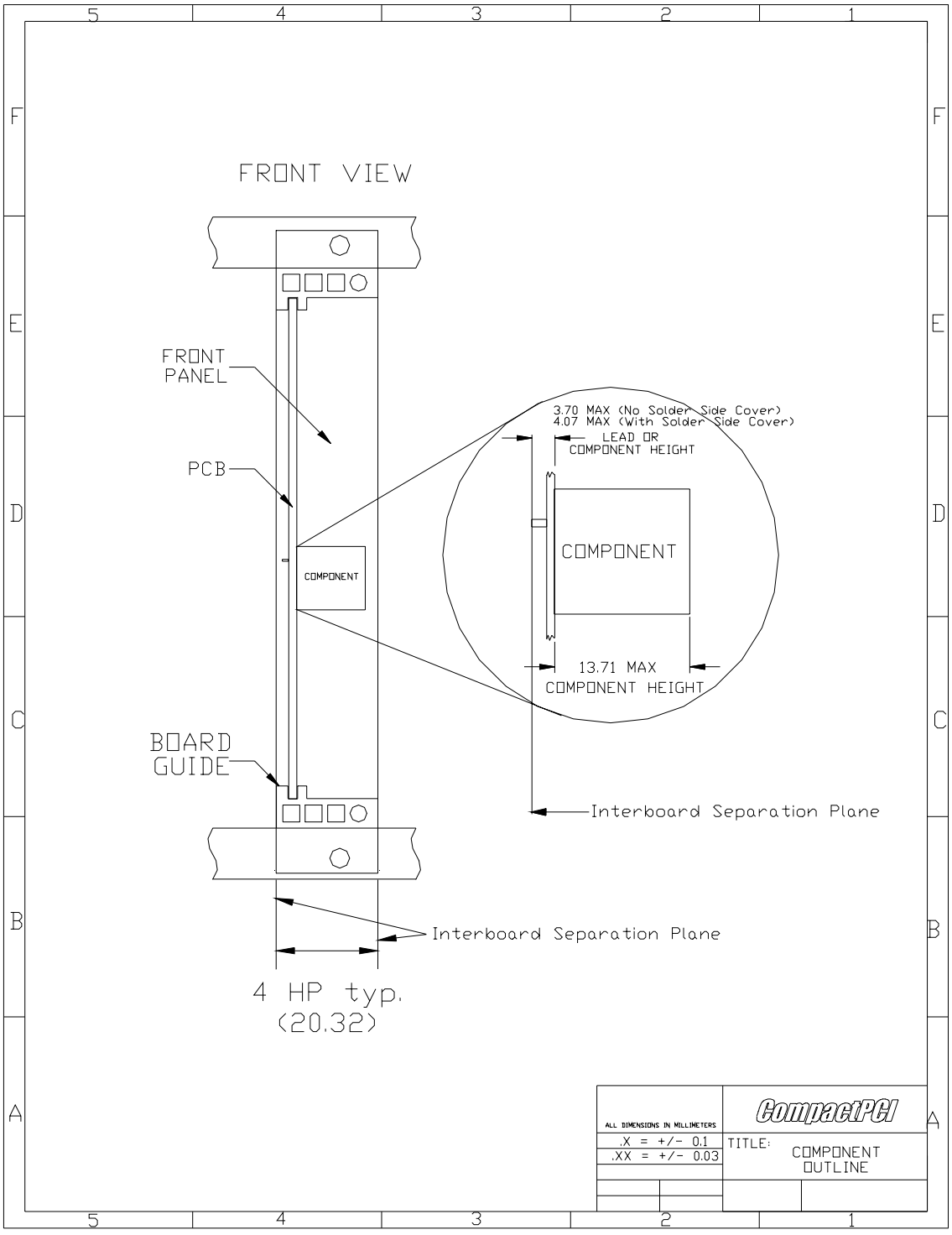


Figure 13. Component Outline.

4.1.9 Front Panels

CompactPCI boards provide a front plate interface that is consistent with Eurocard packaging. CompactPCI boards **shall** use front panels that are compliant with IEEE 1101.1 (for flat panels) or IEEE 1101.10 (EMC panels). IEEE 1101.10 for EMC panels is preferred and **should** be used on all boards and filler panels.

Ejector/injector handles that are compliant with IEEE 1101.10 **shall** also be used. One ejector handle **shall** be used for 3U boards. 6U boards **shall** use two handles. Filler panels do not require handles. Sub-racks **shall** also comply with IEEE 1101.10.

Front entry of CompactPCI boards into the subrack is defined by IEEE 1101.1 and IEEE 1101.10. Rear entry of boards (real panel I/O) into the subrack is defined by IEEE 1101.11.

Physical Slot locations within the subrack **should** be indicated by a numbering scheme visible from the front (and rear if rear panel I/O is utilized) of the subrack. Physical numbers **should** be placed within the compatibility glyphs.

Connector cutouts, labeling, and handle appearance may vary as required. The CompactPCI logo **shall** be clearly visible on the front panel.

Board compatibility glyphs **shall** be displayed on the front panel. Capability glyphs are:

- △ (triangle) for System Slot
- ○ (circle) for Peripheral Slots

Figure 14 illustrates the CompactPCI compatibility glyphs. Boards that can be used in either a System Slot or Peripheral Slot **shall** combine both compatibility glyphs on top of one another.

Figure 14. CompactPCI Compatibility Glyphs.

Figure 15 illustrates the CompactPCI logo that shall be used on the front panels. The font style is Italic Impact.

CompactPCI®

Figure 15. CompactPCI Logo.

4.1.9.1 3U Front Panels

3U boards **shall** use one IEEE 1101.10 handle located on the bottom as illustrated in Figure 16.

4.1.9.2 6U Front Panels

6U boards **shall** use two IEEE 1101.10 handles as illustrated in Figure 17.

4.1.10 System Slot Identification

System Slot capability **shall** be indicated within a CompactPCI subrack by red guide rails. This allows users to easily locate the System Slot. Peripheral slots **shall not** use red guide rails.

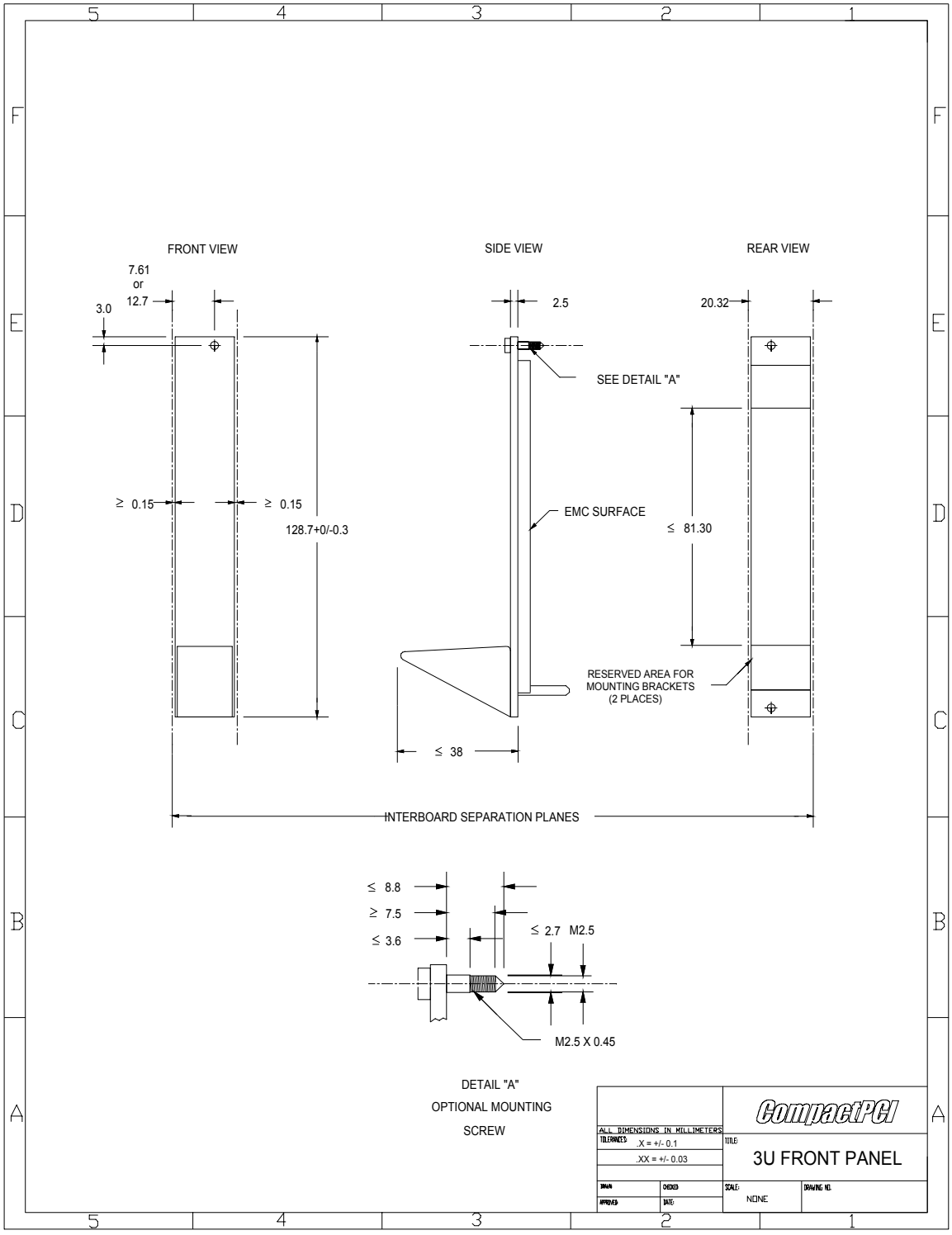


Figure 16. 3U EMC Front Panel.

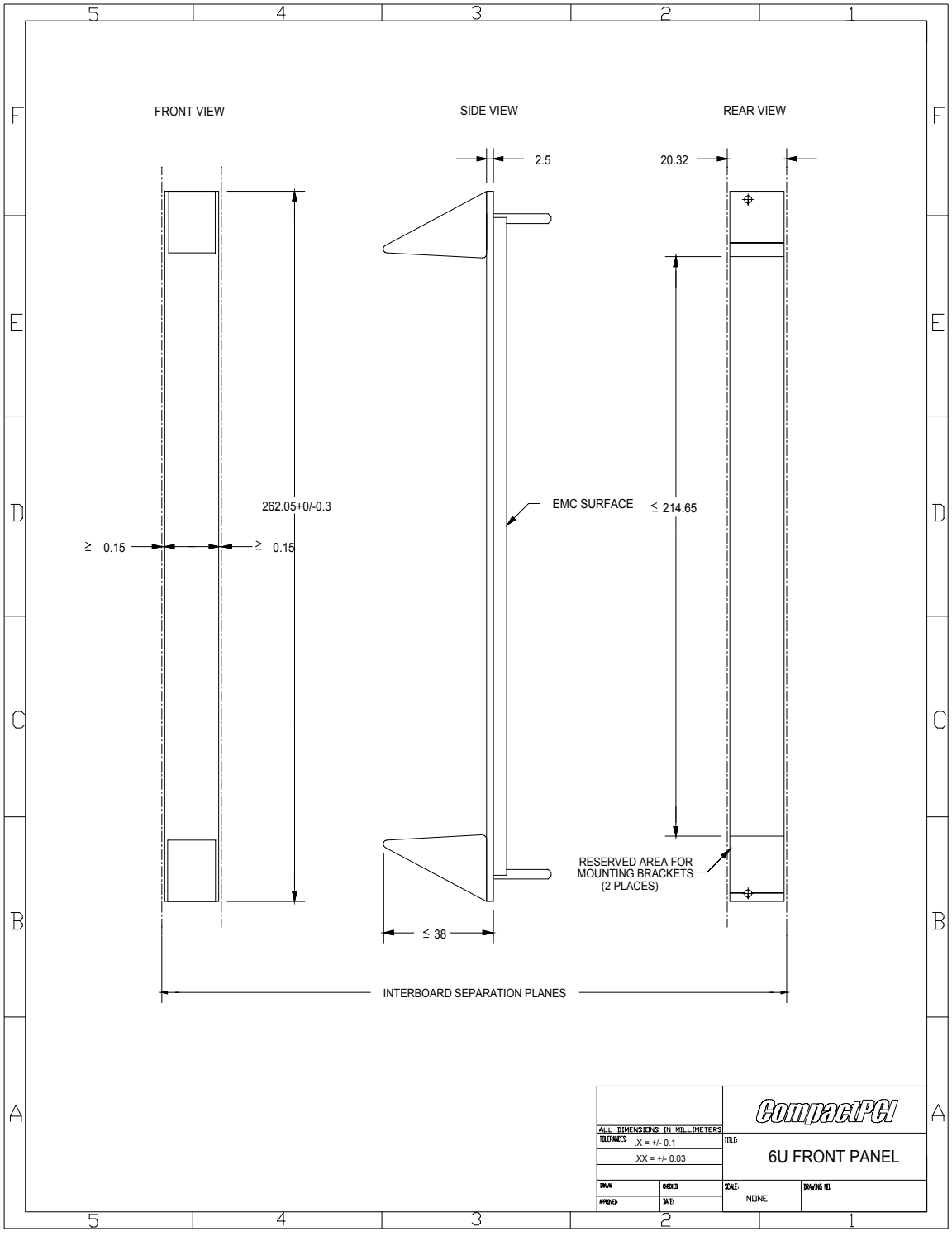


Figure 17. 6U EMC Front Panel.

4.2 Rear-Panel I/O Board Requirements

The front plug-in boards may route I/O through the backplane via the J2/P2, J3/P3, J4/P4 and J5/P5 connector pairs, using any combination of connectors. In many applications, the only practical way to route this I/O off the backplane is to utilize a rear I/O transition board that has standard I/O connectors for each particular type of I/O.

4.2.1 Mechanicals

IEEE 1101.11 defines the generic mechanics for rear-panel I/O transition boards. The mechanical implementation of rear-panel I/O transition boards and subracks **should** be in accordance to IEEE 1101.11 for 80 mm deep boards and subracks (also see Section 4.1.3).

The same front panel, the same handles, the same keying, the same alignment pin, the same EMC and the same ESD mechanics **should** be used as on the front CompactPCI boards.

The same subrack rails, card guides, EMC support, ESD support, keying, alignment pin hole, and injector/extractor comb **should** be used as on the subrack front side, except for the card guide's depth.

Note that rear-panel I/O transition boards are "in-line" with the front CompactPCI boards. This means that the front panels of rear-panel I/O transition boards are reversed (mirrored) from the front boards. The top handles are on the bottom and the bottom handles are on the top. The slot keying holes and hole labels in both the card guides and front panels will be upside down as compared to the front boards and card guides.

The same connector pin labeling sequence **should** be used on the rear I/O transition boards as the on front boards, with the position numbers going from bottom to top. Effectively this is a mirror image of the front board’s layout orientation. By using the same 1 for 1 pin mapping labeling sequence eliminates confusion and I/O signal pin mapping problems. Example, pin J5:A3 of the front board connects to P5:A3 of the backplane, the signal is available as rP5:A3 from the rear of the backplane, and connects to rJ5:A3 of the rear I/O module.

Note that

Figure **9** and Figure 10, illustrating 3U and 6U rear-panel I/O boards, show rJ1 for mechanical reference only.

4.2.2 Power

In some applications, the rear-panel transition board will have active components. Power can be applied either through the I/O pins from the front board, or from the normal power and ground pins defined as part of the J1/P1 and J2/P2 connector pin assignments.

4.2.3 Rear Panel Keying

Rear panel I/O boards **shall** be keyed in accordance with the PICMG 2.10 Keying of CompactPCI Boards and Backplanes specification.

4.3 Backplane Requirements

4.3.1 Connector Orientation

The bus segment connector orientation is illustrated in Figure 18 when viewed from the front of the system chassis. The System Slot **may** be located in any position on a backplane but **shall** be located on either end of the bus segment unless otherwise simulated to ensure compliance to the PCI specification.

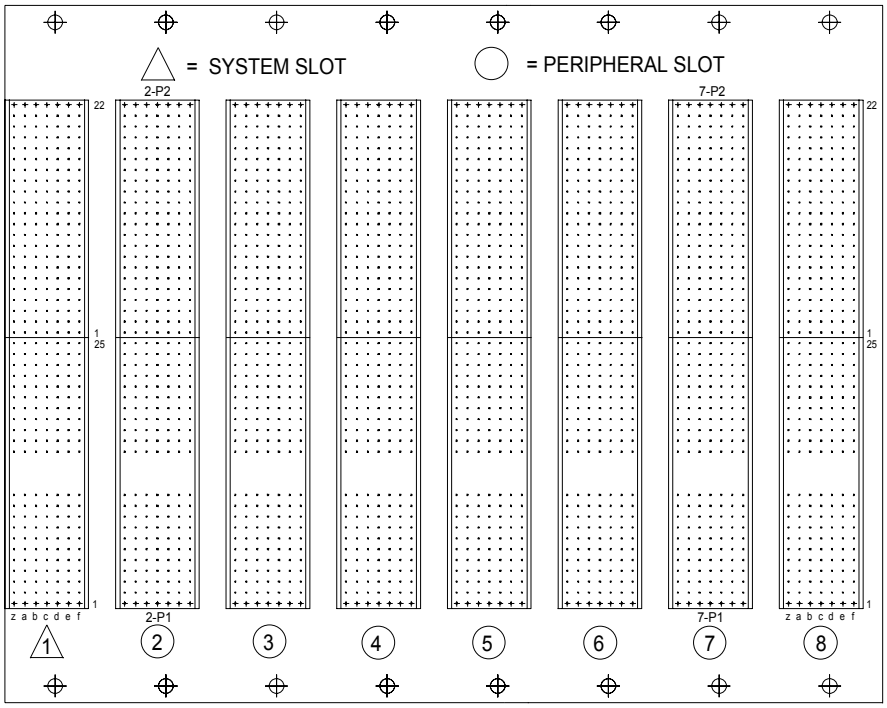


Figure 18. 3U Backplane Example - Front View.

4.3.2 Slot Spacing

This specification and all backplane simulations have assumed a linear topology using 20.32 mm (0.8 inch) board center-to-center spacing. Any other topology **shall** be simulated or otherwise verified to ensure compliance to the PCI specification.

Bus segments **shall** not have more than eight slots without one or more PCI bridges.

4.3.3 Slot Designation

Physical backplane slots **shall** be designated 1, 2, 3, through N, where N is the number of slots. For example, an eight slot backplane would designate the backplane slots as 1 through 8 with the compatibility glyphs. Slot numbering **shall** start at the top left corner as viewed from the front.

Logical slot numbers **shall** be defined by the IDSEL and associated address used to select the slot as defined in Table 7. Logical slot numbers are used in the nomenclature to define the physical outline of a connector on a bus segment. Please see Chapter 3 for signal routing requirements.

Each slot **may** be implemented with one or more connectors. Backplane connectors **shall** be designated as P1 through P5, corresponding in location to the board's connectors illustrated in Figure 6 and Figure 7.

Any given connector **shall** be referenced by first specifying the logical slot number (1...8) followed by a hyphen and then the individual connector (P1...P5). For example, in a 32-bit 3U system 5-P2 would designate the rear-panel I/O connector in logical slot 5. In a 64-bit 6U system 1-P3 would designate the rear-panel I/O connector in logical slot 1.

4.3.4 Bus Segments

Bus segments **may** accommodate 64-bit operation or **shall** provide individual pull-up resistors at each board slot for the REQ64# and ACK64# signals. Refer to the PCI specification for details. The System Slot **shall** use both J1 and J2 to allow the arbitration and clock signals to be connected to the backplane from a System Slot board. Connectors require pin staging (see Section 5.8) to accommodate hot swap operation.

CompactPCI bus segments **shall** bus all signals in all slots within the segment except the slot specific signals: CLK, REQ# and GNT#. Each logical slot also has a unique IDSEL signal connected to one of the upper ADxx signals for configuration (plug and play) decoding.

Backplanes **shall** provide connection for the DEG#(P2:C16) and FAL# (P2:C15) signals at the System Slot that may be provided by the power supply or other system management functions.

4.3.5 Backplane Dimensions

Depending on system design requirements, termination networks, etc., the left and right ends of a backplane can be made longer. Whenever extended, the end dimensions **shall** be in increments of 5.08 mm. This will allow for modular construction of backplanes and subracks.

4.3.5.1 3U Backplanes

A 3U backplane without a power connector is illustrated in Figure 19. This figure illustrates physical slot locations designated 1 through 8.

4.3.5.2 6U Backplanes

A 6U backplane without a power connector is illustrated in Figure 20. Physical slot locations are designated 1 through 8.

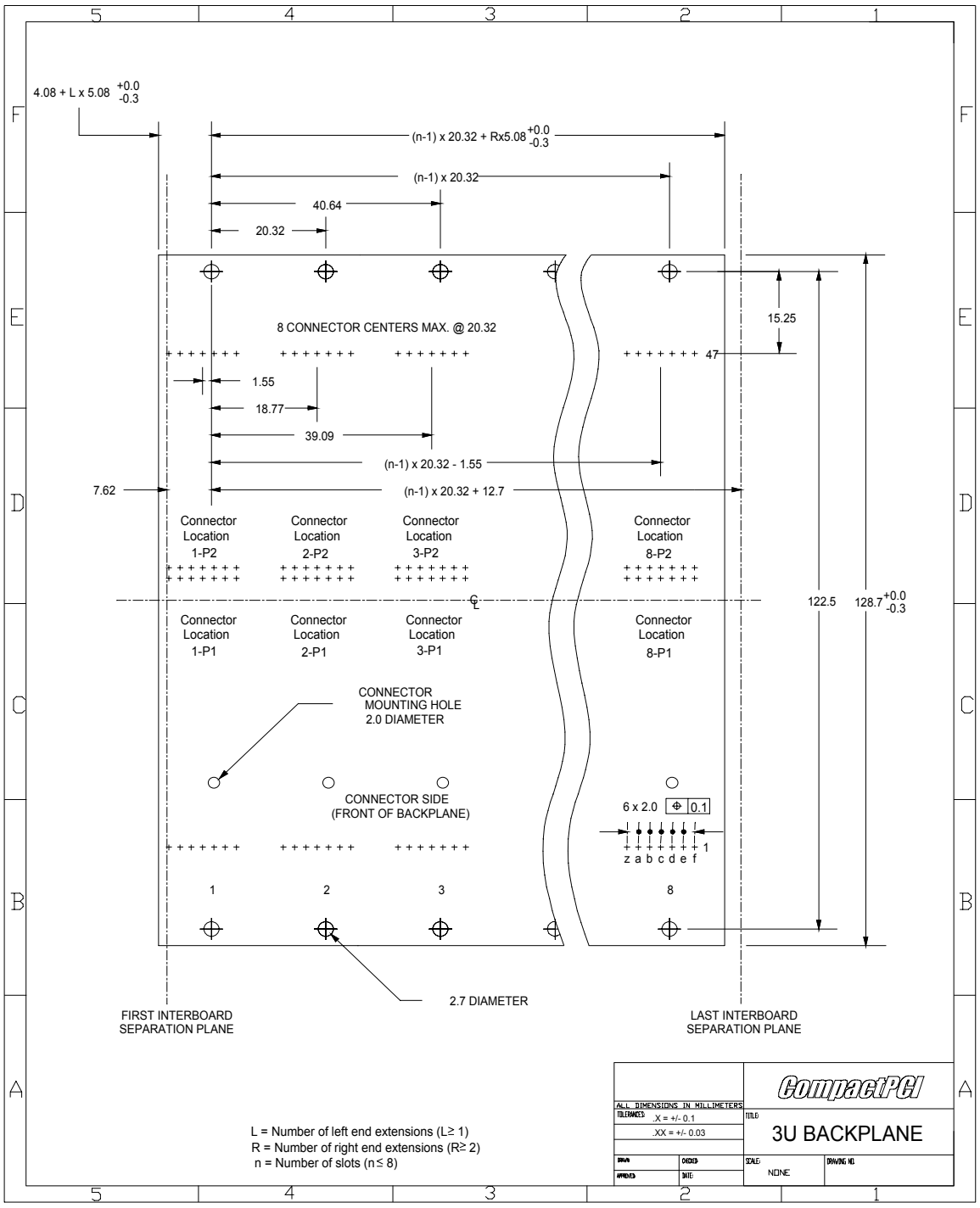


Figure 19. 3U Backplane Dimensions.

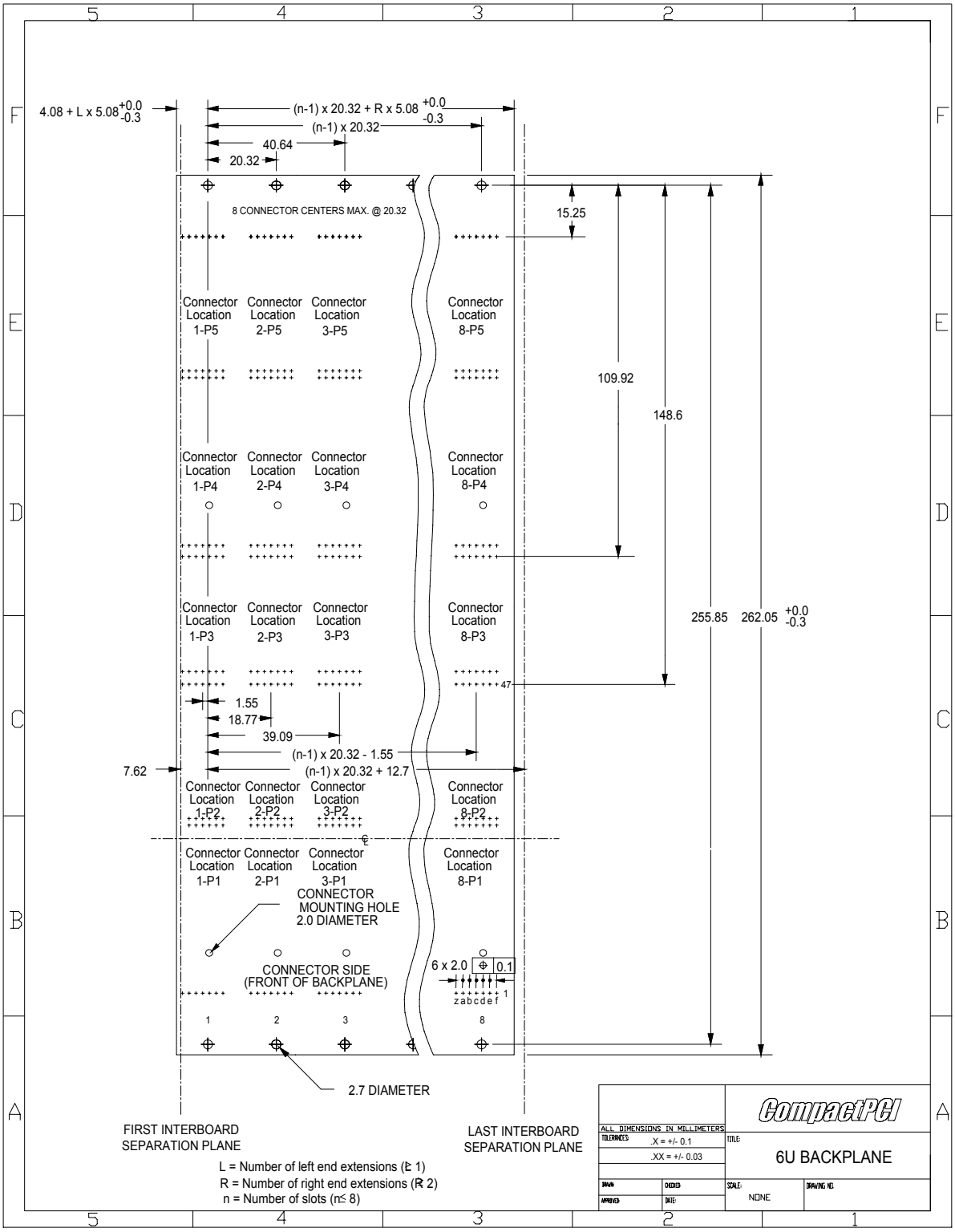


Figure 20. 6U Backplane Dimensions.

5 Connector Implementation

All 3U/6U CompactPCI boards and backplanes **shall** follow the connector implementation shown in Figure 21 and Figure 22. The connectors belong to the 2 mm hard metric family as defined by IEC 61076-4-101. Appendix B summarizes the connector implementation, and the connector pin numbering regime.

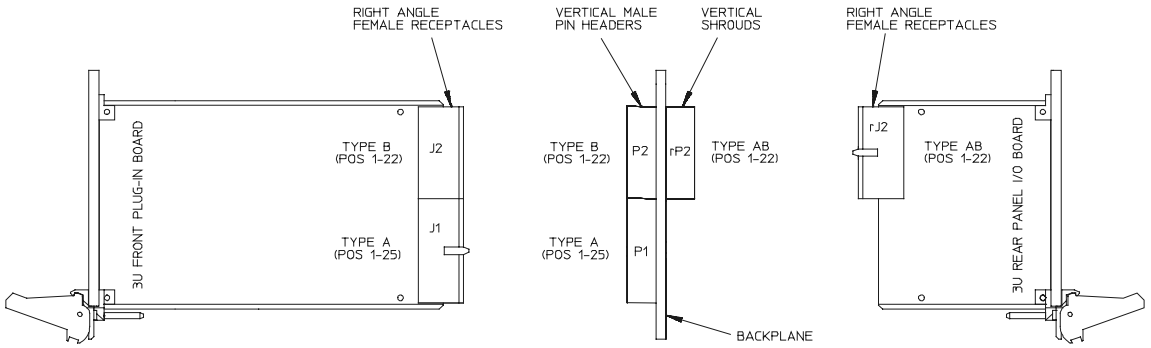


Figure 21. 3U Connector Implementation

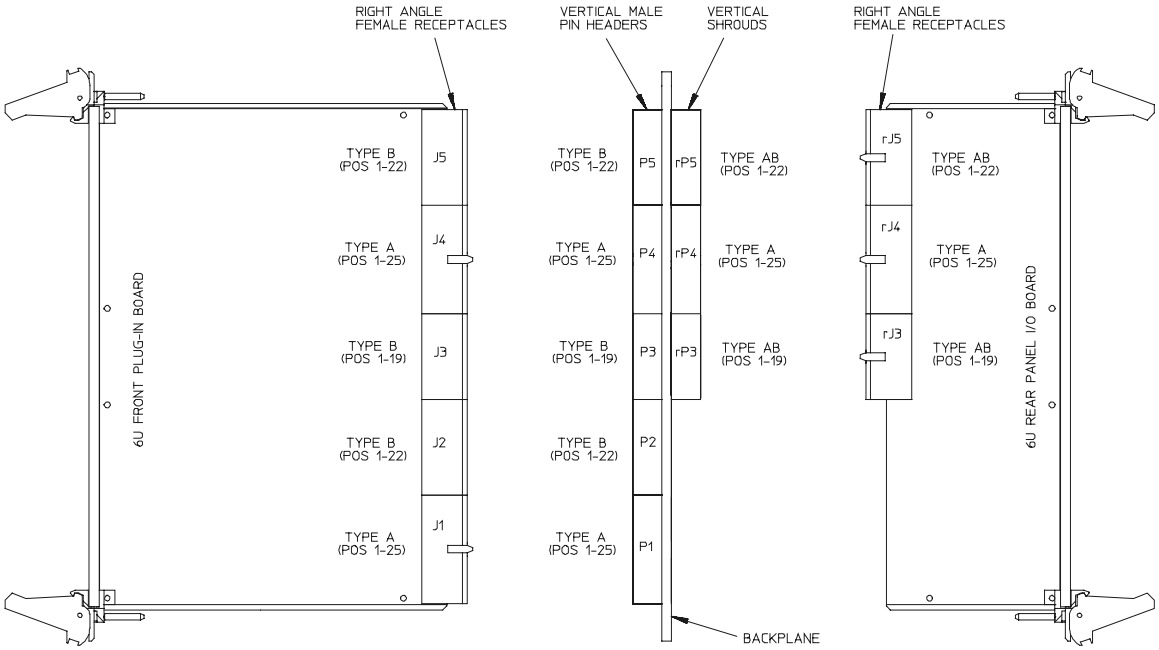


Figure 22. 6U Connector Implementation

5.1 Overview

5.1.1 Location

Connector locations are designated from bottom to top by numbers 1 to 5. The prefix "J" is assigned to connectors on front plug-in boards. The prefix "P" is assigned to connectors on the front side of backplane. The prefix "rP" is assigned to connectors on the rear side of backplane. The prefix "rJ" is assigned to connectors on rear-panel I/O boards.

5.1.2 Housing Types

Connector housing types are designated by Type A, Type B, and Type AB. Type A connectors have alignment features and coding keys. Type B connectors are plain without these features. Type AB connectors have alignment features without coding keys. The Type AB connector is new and has not been incorporated into the IEC specifications at the date of this writing, see *PICMG Type AB 2mm Connector Guideline Document* for information.

To avoid confusion, all products involving rear panel I/O boards (boards, systems, backplanes, etc) **should** clearly state in customer documentation which level of compliance the product conforms to, either Revision 2.X or Revision 3.X of the CompactPCI specification.

System and backplane vendors **shall** use Type AB shrouds in locations rP2/rP3/rP5 to insure backward compatibility with legacy rear panel I/O boards and forward compatibility with rear panel I/O boards being produced today.

Refer to Appendix B for more information on 2mm Connector usage.

5.1.3 Connector Tail Lengths

In CompactPCI connector implementations, feed-to connectors are defined as connectors that interface to the front side of the backplane only and do not extend through the backplane. Feed-thru connectors are defined as having long tails that extend through the backplane for rear-panel I/O interfacing.

Connectors defined for rear-panel I/O **shall** have feed-thru tails of 16mm length. Connectors that are not defined for rear-panel I/O **shall** be feed-to.

5.1.4 Backplane / Board Population Options

At a minimum, the J1 connector is required for 32-bit CompactPCI and J2 is required for the additional 64-bit CompactPCI signals. The other connectors may or may not be populated depending upon the system requirements. See the various platform specifications for their specific connector population requirements.

5.2 J1 (32-Bit PCI Signals)

CompactPCI board connector J1 is used for the 32-bit PCI signals as illustrated in **Table 13**. 32-bit boards **shall** always use this connector. Use of the J2 connector is optional.

5.3 J2 Connector

J2 **may** be used for 64-bit PCI transfers or for rear-panel I/O. The keying of this connector function is provided by the IEEE 1101.10 front panel key. J2 **shall** be used on System Slot boards to provide arbitration and clock signals for peripheral boards. J2 **shall** be used if 64-bit PCI operation, rear-panel I/O, or geographic addressing is supported.

5.3.1 Peripheral Slot 64-Bit PCI

The mapping of 64-bit PCI within J2 is shown in **Table 13**.

5.3.2 Peripheral Slot Rear-Panel I/O

The mapping of rear-panel I/O for peripheral boards within J2 is shown in **Table 14**.

5.3.3 System Slot 64-bit PCI

The mapping of 64-Bit PCI for the system slot is shown in **Table 15**.

5.3.4 System Slot Rear-Panel I/O

The mapping of rear-panel I/O for system slot boards is shown in **Table 16**.

5.4 Bussed Reserved Pins

The BRSVPxxx signals **shall** be bussed between connectors and are reserved for future definition.

5.5 Non-Bussed Reserved Pins

The RSV signals **shall** be non-bussed between connectors and are reserved for future definition.

5.6 Power Pins

All CompactPCI connectors provide pins for +5V, +3.3V, +12V and -12V operating power. Additional power pins labeled +V(I/O) provide power for Universal boards utilizing I/O buffers driving backplane signals that **may** operate from +5V or +3.3V.

On these boards, the PCI component's I/O buffers **shall** be powered from V(I/O), not from +5V or +3.3V power pins.

Backplane pins labeled V(I/O) are connected to +5V on 5 V keyed systems and +3.3V on 3.3 V keyed systems. Alternatively, a separate V(I/O) power plane may be provided to supply 5 V or 3.3 V power.

The IEC 61076-4-101 connector is a press-fit connector. Connections between the voltage planes and connector pins **should** be a solid (no thermal relief) interconnect. This provides a low inductance connection between the connector pin and each power plane.

5.7 5V/3.3V PCI Keying

CompactPCI implements a keying mechanism to differentiate 5 V or 3.3 V signaling operation. The keying mechanism is designed to prevent a board built with one buffer technology (5 V or 3.3 V) from being inserted into a system designed for the other buffer technology (3.3 V or 5 V, respectively). Universal boards **may** operate in either +5V or +3.3V systems and are not keyed. Positions 12-14 of the CompactPCI connector are used for the keying mechanism. Backplanes **shall** be configured as either 5V or 3.3V and **shall** provide the appropriate key. It is not possible to have a "universal" backplane. Refer to the *PICMG 2.10, Keying of CompactPCI Boards and Backplanes specification* for additional details on keying.

Table 12. Coding Key Color Assignments and Part Numbers.

Signaling Voltage V(I/O)	**Color Reference**		**Code #**	
	Color	**RAL # (1)**	**Male (Backplane)**	**Female (Board)**
3.3 V	Cadmium Yellow	1021	3456	1278
5 V	Brilliant Blue	5007	1567	2348
3.3 V or 5 V (Universal Board)	-	-	N/A(2)	No Key

Notes:

1. RAL is a trademark of the central organization for product assurance in Germany. One of its tasks is harmonization in the use of colors. Color samples may be ordered from: Muster-Schmidt KG, RAL - Farbkartenvertrieb, Postfach 2751, D - 3400 Gottingen, Germany.

2. Backplanes **shall** be configured for either 5 V or 3.3 V V(I/O). Plug in boards may be designed to be universal and **shall** therefore have no key loaded.

5.8 Pin Assignments

Table 13. CompactPCI Peripheral Slot 64-Bit Connector Pin Assignments[1][10, 11].

22	GND	GA4[13]	GA3[13]	GA2[13]	GA1[13]	GA0[13]	GND	
21	GND	RSV	RSV	RSV	RSV	RSV	GND	
20	GND	RSV	RSV	RSV	GND	RSV	GND	
19	GND	RSV	RSV	RSV	RSV	RSV	GND	P2
18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND	/
17	GND	BRSVP2A17	GND	RSV	RSV	RSV	GND	J2
16	GND	BRSVP2A16	BRSVP2B16	RSV	GND	BRSVP2E16	GND	
15	GND	BRSVP2A15	GND	RSV	RSV	RSV	GND	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND	
13	GND	AD[38]	GND	V(I/O)[2]	AD[37]	AD[36]	GND	C
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND	O
11	GND	AD[45]	GND	V(I/O)[2]	AD[44]	AD[43]	GND	N
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND	N
9	GND	AD[52]	GND	V(I/O)[2]	AD[51]	AD[50]	GND	E
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND	C
7	GND	AD[59]	GND	V(I/O)[2]	AD[58]	AD[57]	GND	T
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND	O
5	GND	C/BE[5]#	GND	V(I/O)[2]	C/BE[4]#	PAR64	GND	R
4	GND	V(I/O)[2]	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND	
3[3]	GND	RSV	GND	RSV	RSV	RSV	GND	
2[3]	GND	RSV	RSV	UNC[4]	RSV	RSV	GND	
1[3]	GND	RSV	GND	RSV	RSV	RSV	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	
24	GND	AD[1]	5V	V(I/O)[2],	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	P1
21	GND	3.3V	AD[9]	AD[8]	M66EN[5]	C/BE[0]#	GND	/
20	GND	AD[12]	GND	V(I/O)[2]	AD[11]	AD[10]	GND	J1
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)[2]	STOP#	LOCK#	GND	C
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#[7]	TRDY#	GND	O
12-14	KEY AREA							N
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	N
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	E
9	GND	C/BE[3]#	IDSEL[7]	AD[23]	GND	AD[22]	GND	C
8	GND	AD[26]	GND	V(I/O)[2]	AD[25]	AD[24]	GND	T
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	O
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	R
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	
4	GND	IPMB_PWR	HEALTHY#[18]	V(I/O)[2]	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK[15]	5V	TMS[15]	TDO[15]	TDI[15]	GND	
1	GND	5V	-12V	TRST#[15]	+12V	5V	GND	
Pin	Z[14]	A	B	C	D	E	F[9]	

= long pins (front only) = short pins (front only) = medium length pins (front only)

Notes: (See page 69)

Table 14 CompactPCI Peripheral Slot Rear-Panel I/O Connector Pin Assignments[1][3][8, 9]

22	GND	GA4[13]	GA3[13]	GA2[13]	GA1[13]	GA0[13]	GND	
21	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
20	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
19	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
18	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	P2
17	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	/
16	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	J2
15	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
14	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
13	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	C
12	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	O
11	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	N
10	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	N
9	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	E
8	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	C
7	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	T
6	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	O
5	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	R
4	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
3	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
2	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
1	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	
24	GND	AD[1]	5V	V(I/O)[2],	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	P1
21	GND	3.3V	AD[9]	AD[8]	M66EN[5]	C/BE[0]#	GND	/
20	GND	AD[12]	GND	V(I/O)[2]	AD[11]	AD[10]	GND	J1
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)[2]	STOP#	LOCK#	GND	C
15	GND	3.3V	FRAME#	IRDY#	BD_SEL#[7]	TRDY#	GND	O
12-14	KEY AREA							N
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	N
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	E
9	GND	C/BE[3]#	IDSEL[7]	AD[23]	GND	AD[22]	GND	C
8	GND	AD[26]	GND	V(I/O)[2]	AD[25]	AD[24]	GND	T
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	O
6	GND	REQ#	GND	3.3V	CLK	AD[31]	GND	R
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND	
4	GND	IPMB_PWR	HEALTHY# [18]	V(I/O)[2]	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK[15]	5V	TMS[15]	TDO[15]	TDI[15]	GND	
1	GND	5V	-12V	TRST#[15]	+12V	5V	GND	
Pin	Z[14]	A	B	C	D	E	F[9]	

= long pins (front only) = short pins (front only) = medium length pins (front only)

Notes: (See page 69)

Table 15. CompactPCI System Slot 64-bit Connector Pin Assignment

22	GND	GA4[13]	GA3[13]	GA2[13]	GA1[13]	GA0[13]	GND	
21	GND	CLK6	GND	RSV	RSV	RSV	GND	
20	GND	CLK5	GND	RSV	GND	RSV	GND	
19	GND	GND	GND	RSV[16]	RSV[16]	RSV[16]	GND	P2
18	GND	BRSVP2A18	BRSVP2B18	BRSVP2C18	GND	BRSVP2E18	GND	/
17	GND	BRSVP2A17	GND	PRST#	REQ6#	GNT6#	GND	J2
16	GND	BRSVP2A16	BRSVP2B16	DEG#	GND	BRSVP2E16	GND	
15	GND	BRSVP2A15	GND	FAL#	REQ5#	GNT5#	GND	
14	GND	AD[35]	AD[34]	AD[33]	GND	AD[32]	GND	
13	GND	AD[38]	GND	V(I/O)[2]	AD[37]	AD[36]	GND	C
12	GND	AD[42]	AD[41]	AD[40]	GND	AD[39]	GND	O
11	GND	AD[45]	GND	V(I/O)[2]	AD[44]	AD[43]	GND	N
10	GND	AD[49]	AD[48]	AD[47]	GND	AD[46]	GND	N
9	GND	AD[52]	GND	V(I/O)[2]	AD[51]	AD[50]	GND	E
8	GND	AD[56]	AD[55]	AD[54]	GND	AD[53]	GND	C
7	GND	AD[59]	GND	V(I/O)[2]	AD[58]	AD[57]	GND	T
6	GND	AD[63]	AD[62]	AD[61]	GND	AD[60]	GND	O
5	GND	C/BE[5]#	GND	V(I/O)[2]	C/BE[4]#	PAR64	GND	R
4	GND	V(I/O)[2]	BRSVP2B4	C/BE[7]#	GND	C/BE[6]#	GND	
3[3]	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND	
2[3]	GND	CLK2	CLK3	SYSEN#[4]	GNT2#	REQ3#	GND	
1[3]	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	
24	GND	AD[1]	5V	V(I/O)[2],	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	P1
21	GND	3.3V	AD[9]	AD[8]	M66EN[5]	C/BE[0]#	GND	/
20	GND	AD[12]	GND	V(I/O)[2]	AD[11]	AD[10]	GND	J1
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)[2]	STOP#	LOCK#	GND	C
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND	O
12-14	KEY AREA							N
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	N
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	E
9	GND	C/BE[3]#	GND	AD[23]	GND	AD[22]	GND	C
8	GND	AD[26]	GND	V(I/O)[2]	AD[25]	AD[24]	GND	T
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	O
6	GND	REQ0#	GND	3.3V	CLK0	AD[31]	GND	R
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT0#	GND	
4	GND	IPMB_PWR	HEALTHY# [18]	V(I/O)[2]	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK[15]	5V	TMS[15]	TDO[15]	TDI[15]	GND	
1	GND	5V	-12V	TRST#[15]	+12V	5V	GND	
Pin	Z[14]	A	B	C	D	E	F[9]	

= long pins (front only) = short pins (front only) = medium length pins (front only)

Notes: (See page 69)

Table 16. CompactPCI System Slot Rear-Panel I/O Connector Pin Assignments.

22	GND	GA4[13]	GA3[13]	GA2[13]	GA1[13]	GA0[13]	GND	
21	GND	CLK6	GND	BP(I/O)	BP(I/O)	BP(I/O)	GND	
20	GND	CLK5	GND	BP(I/O)	BP(I/O)	BP(I/O)	GND	
19	GND	GND	GND	BP(I/O)[16]	BP(I/O)[16]	BP(I/O)[16]	GND	P2
18	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	/
17	GND	BP(I/O)	BP(I/O)	PRST#	REQ6#	GNT6#	GND	J2
16	GND	BP(I/O)	BP(I/O)	DEG#	GND	BP(I/O)	GND	
15	GND	BP(I/O)	BP(I/O)	FAL#	REQ5#	GNT5#	GND	
14	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
13	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	C
12	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	O
11	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	N
10	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	N
9	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	E
8	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	C
7	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	T
6	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	O
5	GND	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	R
4	GND	V(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	BP(I/O)	GND	
3[3]	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND	
2[3]	GND	CLK2	CLK3	SYSEN#[4]	GNT2#	REQ3#	GND	
1[3]	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND	
25	GND	5V	REQ64#	ENUM#	3.3V	5V	GND	
24	GND	AD[1]	5V	V(I/O)[2],	AD[0]	ACK64#	GND	
23	GND	3.3V	AD[4]	AD[3]	5V	AD[2]	GND	
22	GND	AD[7]	GND	3.3V	AD[6]	AD[5]	GND	P1
21	GND	3.3V	AD[9]	AD[8]	M66EN[5]	C/BE[0]#	GND	/
20	GND	AD[12]	GND	V(I/O)[2]	AD[11]	AD[10]	GND	J1
19	GND	3.3V	AD[15]	AD[14]	GND	AD[13]	GND	
18	GND	SERR#	GND	3.3V	PAR	C/BE[1]#	GND	
17	GND	3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND	
16	GND	DEVSEL#	GND	V(I/O)[2]	STOP#	LOCK#	GND	C
15	GND	3.3V	FRAME#	IRDY#	GND	TRDY#	GND	O
12-14	KEY AREA							N
11	GND	AD[18]	AD[17]	AD[16]	GND	C/BE[2]#	GND	N
10	GND	AD[21]	GND	3.3V	AD[20]	AD[19]	GND	E
9	GND	C/BE[3]#	GND	AD[23]	GND	AD[22]	GND	C
8	GND	AD[26]	GND	V(I/O)[2]	AD[25]	AD[24]	GND	T
7	GND	AD[30]	AD[29]	AD[28]	GND	AD[27]	GND	O
6	GND	REQ0#	GND	3.3V	CLK0	AD[31]	GND	R
5	GND	BRSVP1A5	BRSVP1B5	RST#	GND	GNT0#	GND	
4	GND	IPMB_PWR	HEALTHY#[18]	V(I/O)[2]	INTP	INTS	GND	
3	GND	INTA#	INTB#	INTC#	5V	INTD#	GND	
2	GND	TCK[15]	5V	TMS[15]	TDO[15]	TDI[15]	GND	
1	GND	5V	-12V	TRST#[15]	+12V	5V	GND	
Pin	Z[14]	A	B	C	D	E	F[9]	

= long pins (front only) = short pins (front only) = medium length pins (front only)

Notes: (See page 69)

Notes for Table 13 through Table 16:

1. These diagrams define the pin assignments from the front of the system chassis. Refer to Chapter 3 for pin assignment differences between the system and board slots.
2. The V(I/O) signals are either 5 V or 3.3 V, depending on the system implementation.
3. Table 13 and Table 14 define the signals for Peripheral slots. Table 15 and Table 16 define the signals for System slots.
4. Connector P2 pin C2 is grounded at the System Slot only. Peripheral slots leave C2 unconnected (UNC). Boards that use this signal (e.g., CPU boards that may be used in the System Slot or Peripheral Slot) **shall** provide a local pull-up to V(I/O). Boards designed for System Slot only use should tie this pin directly to the ground plane.
5. Connector P1 pin D21 (M66EN) is defined as GND for 33 MHz backplanes. 66 MHz backplanes **shall** bus this signal to all slots.
6. The following signals are long (level 3) pins in P1 for early power to hot swap boards: D3, D5, D7, D9, D11, D17, D19, D23, C4, C6, C22, C24.
7. Connector P1 pin D15 (BD_SEL#) is defined as a short length pin and is used for the final connection sequence by hot swap boards. Connector P1 pin B9 (IDSEL) is defined as a short length pin. Refer to PICMG 2.1, CompactPCI Hot Swap Specification for details.
8. These signals are defined as bused reserve (BRSVPxxx) signals. They were defined as PCI cache signals SDONE# and SBO# (Defined in the PCI 2.1 Specification) in earlier revisions of this specification.
9. Board Observation: Some manufacturers of top shields utilize every other ground pin while some use every ground pin.
10. CompactPCI connector pin numbering is intentionally different from the connector manufacturer's pin numbering. This was done to allow the connectors to start at the bottom of the board and "grow" upward from J1/P1 through J5/P5.
11. BP(I/O) signals are defined as "long" tail connectors with 16.0 mm tails. Refer to IEEE 1101.11 for details. All other signals in P1 and P2 are defined to be "short" tail connectors with 4.5 mm tails.
12. BRSVPxxx signals accommodate PCI reserved signals. Bus segments **shall** bus these signals between connectors.
13. If P2 is populated, GA[4..0] **shall** be used for geographic addressing on the backplane. Each backplane connector in a CompactPCI system has a unique encoding for GA[4..0]. See Section 3.2.7.6 for details.
14. Row Z is not required on plug-in boards. If row Z contacts are populated on the backplane at P1 and P2, they **shall** be connected to logic ground.
15. Usage of JTAG signals is discouraged. These signal definitions will be redefined in a future revision of the CompactPCI specification. Backplanes **shall** bus TCK, TMS and TRST# to all CompactPCI Slots. TDO and TDI **should** be non-bussed.
16. System slot connector P2, pins C19 (ICMB_SDA), D19 (ICMB_SCL) and E19 (ICMB_PWR) have been defined by the System Management Subcommittee as the appropriate rear-panel I/O pins to be used for a secondary I^2C bus local to the system board. Refer to the PICMG 2.9 System Management Specification for further information.
17. Signals IDSEL and BD_SEL# are connected to GND on the System Slot. The Dual Host Subcommittee may further define their use on the system slot.
18. P1 pin B4 is reserved for HEALTHY#. Backplane must leave this pin open and include a bypass capacitor, refer to section 3.2.10 and the CompactPCI Hot Swap Specification, PICMG 2.1 for details.

Revision History

This chapter documents the changes made to the CompactPCI Specification.

Table 17. Revision History.

Revision	Date	Description
R1.0	November 1, 1995	Initial release
R2.1	September 2, 1997	Version 2.0 Release 2.1
D3.0	September 23, 1999	Draft Version 3.0

A. CompactPCI Buffer Models

The following plots represent the models used for simulating the CompactPCI environment for both 5V and 3.3V buffers. The buffer models were constructed from information that represents the widest PCI buffer variation that that could be manufactured with realistic process technology. Note that some regions that the PCI specification allows are excluded from the simulated, real models. Several silicon manufacturers have verified these models against their actual processes.

Additional, detailed information can be obtained in the full simulation report available from PICMG.

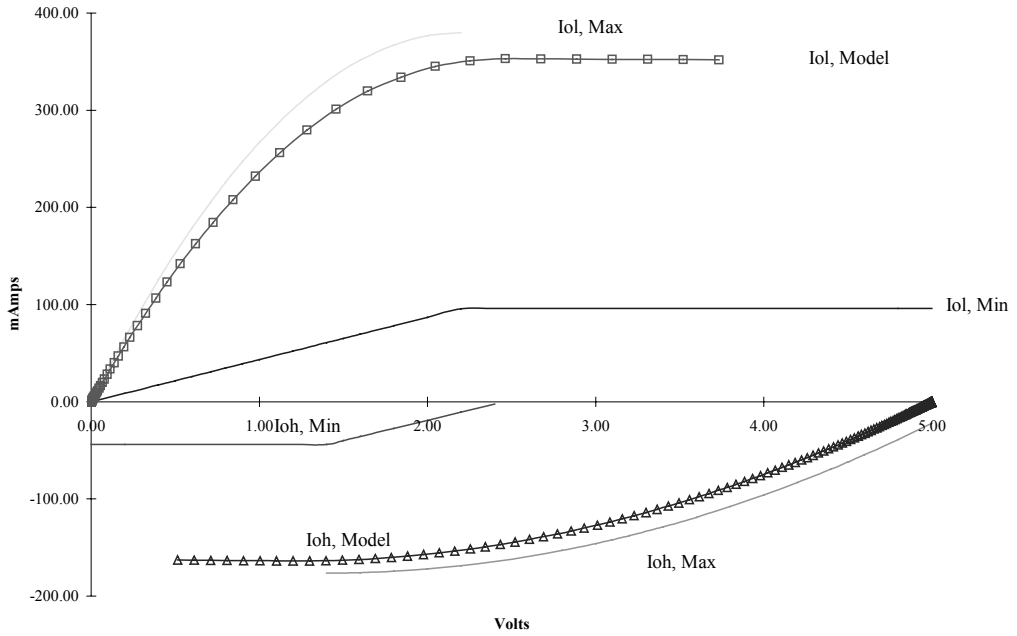


Figure 23. 5V Strong PCI Model

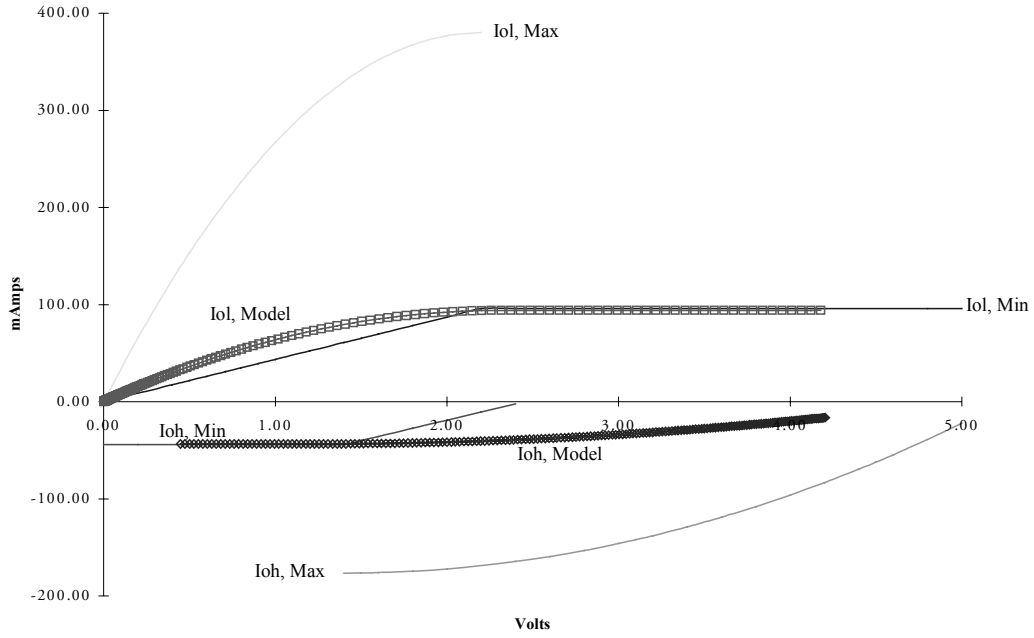


Figure 24. 5V Weak PCI Model

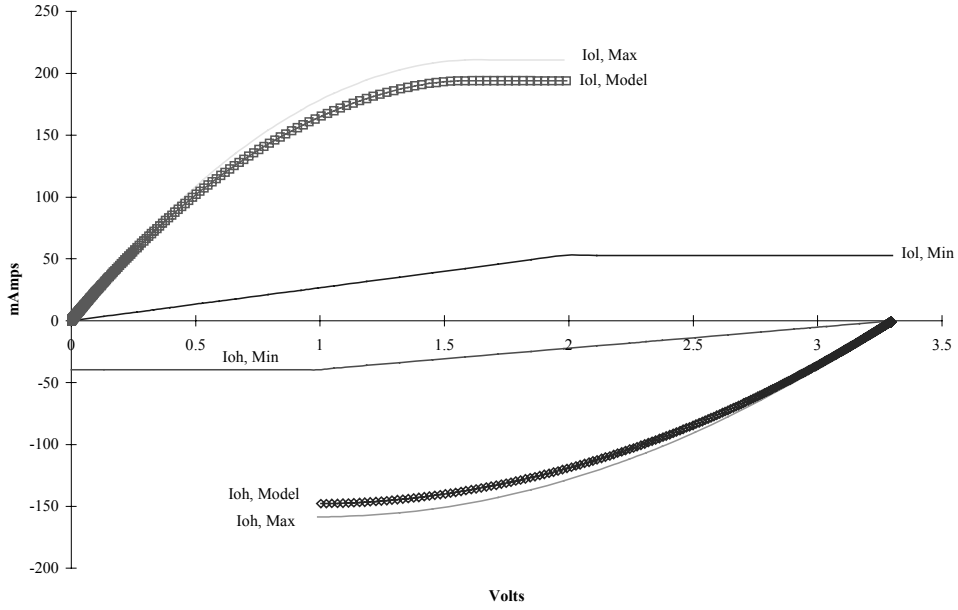


Figure 25. 3.3V Strong PCI Model

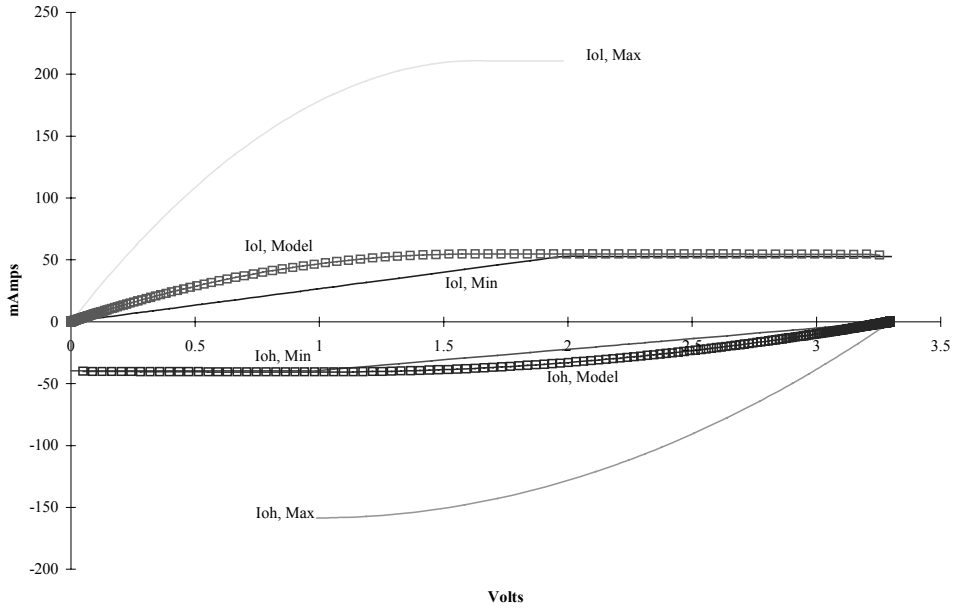


Figure 26. 3.3V Weak PCI Model

B. Connector Implementation

B.1 General

This appendix provides more descriptive information on the use of 2mm connectors including backward compatibility issues. The accompanying PICMG Type AB 2mm Connector Guideline Document provides specification information on the Type AB shroud in advance of an approved IEC specification. Once an IEC specification is available the Guideline Document **shall** be superceded.

B.2 Connectors

When the CompactPCI pinout was originally defined using the IEC-61076-4-101 family of connectors, there was a dilemma. In a 3U form-factor, only 47 rows of pins would fit mechanically in the 100 mm board dimension, with allowance made for the card guides. The original CompactPCI “J1” connector consisted of a single piece "A" module, now designated J1, and a separate “B” module which is now designated as J2. Simple 32-bit boards could be developed populated with only the A module for cost savings.

This left the "B" module, as the logical connector to cut down by three rows to create the 47 row pair. Because of the way that the J2 connector had to be cut down, rows 1-3 had to be removed because the mating surface between J1 and J2 is keyed to prevent connectors from being inserted 180 degrees from one another. This would have left the connector starting at row 4.

To address this problem a decision was made to number connector pins from bottom to top, in the reverse order from IEC 61076-4-101.

It should be noted that the reversal in numbering is not, strictly speaking, on a pin for pin basis. Therefore the pins are numbered from 1 at the bottom of J1P1 to 25 at the top with three numbered positions in the middle that are taken up by the alignment and keying area. J2/P2 connector is numbered from the bottom to top 1 through 22 in an uninterrupted pattern. The column designations, z, a, b, c, d, e, and f used by CompactPCI are unchanged and conform to IEC 61076-4-101.

B.3 Alignment

B.3.1 Front Plug-In Board Alignment

Front plug-in boards have alignment features on the Type A connectors to insure the board mates correctly with the backplane. These are used in locations J1/P1 and J4/P4.

B.3.2 Rear Panel I/O Board Alignment

Due to the connector population options on rear panel I/O boards for various platform options, all connectors used in the transition area **shall** have alignment features to insure the board mates correctly to the backplane. This is achieved through the use of Type A and Type AB connectors on the rear panel I/O boards and backplane in locations shown in Figure 21 and Figure 22.

B.3.3 Backward Compatibility for Rear Panel I/O Boards

Legacy rear panel I/O boards based on the connector implementation for Revision 2.X and below of the CompactPCI specification will plug into systems that follow the connector implementation for Revision 3.X and above of the CompactPCI specification. However, rear panel I/O boards based on the connector implementation for Revision 3.X and above of the CompactPCI specification will not plug into the systems that follow the connector implementation for Revision 2.X and below of the CompactPCI specification.

This occurs due to a compatibility issue between Type B and Type AB connectors required. In Revision 3.X and above of the CompactPCI Specification, Type AB connectors are specified in the rP2/rP3/rP5 and rJ2/rJ3/rJ5 locations to insure that any combination of connectors used for rear panel I/O always have an alignment feature. In Revision 2.X and below, Type B connectors were specified in the rP2/rP3/rP5 and rJ2/rJ3/rJ5 locations. TypeAB shrouds are backwards compatible with Type B right angle receptacles. The converse is not true. Type B shrouds are not backward compatible with Type AB right angle receptacles.

2 mm TYPE AB CONNECTOR SYSTEM

Introduction

The use of rear transition boards on which only a Type B connector is populated has resulted in the development of a hybrid version of the IEC 61076-4-101 2 mm connector. In order to provide alignment during mating for the normally unguided connector, the extended guidance features of the Type A connector body have been modified and incorporated into the Type B connector housing. The resulting configuration provides Type A alignment and guidance with no loss of signal contact count, however, there is no coding feature as is typical with the Type A housings.

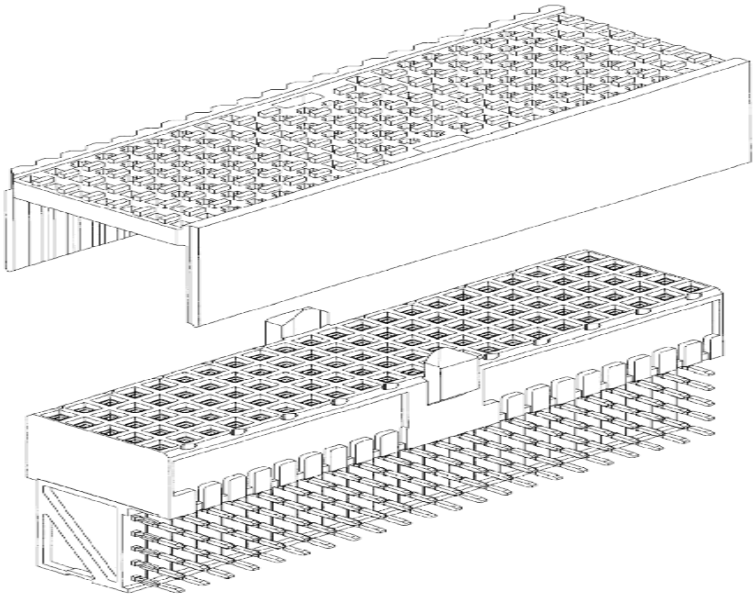


Figure A-1

Connector configuration

The Type AB version of the IEC 61076-4-101 2 mm connectors shall be configured as shown in Figures A1 through A4. There are several parts to the system. The first is a rear pin shroud that is used to transform the fixed board connector pins that project through the backplane into a rear side pin header. The second component is a right angle

free board connector designed to mate with the Type AB shroud/pin combination. The third is a pre-assembled fixed board connector (pin header).

The Type AB extended guidance feature is similar to that found on the Type A version of the IEC 61076-4-101 connectors. It is designed to provide premating guidance and alignment for rear transition modules, especially those which have only the Type B connectors. The feature can also be successfully used to provide guidance for rear transition modules which have additional connectors, even those which have Type A guidance/keying modules.

Connector naming

The proposed naming convention for the new connector will be Type AB. This is a combination of the Type A and B naming conventions utilized and already defined in the IEC 61076-4-101 specification. The new "family" of connectors will have three components, excluding variations on shields, number of rows, pin lengths, etc. These are:

- Type AB shroud (19, 22 and 25 x 7 positions)
- Type AB pin header (19, 22 and 25 x 7 positions)
- Type AB right angle receptacle (free board) connector (19, 22 and 25 X 7 positions)

Recommended Method of Mounting

The Type AB connector components are mounted in the same manner as other IEC 61076-4-101 connectors. Shrouds must be supported and dimensionally located in accordance with the rear transition module system defined in the IEEE 1101.11 equipment practice.

Ratings and characteristics

All ratings and characteristics shall be in accordance with IEC 61976-4-101.

Technical data

All definitions, styles and variants and application information shall be in accordance with IEC 61076-4-101 except as shown in figures A2 through A4.

Dimensional information

The Type AB shroud, pin header and receptacle connector design details are shown in Figures A2 through A4. All dimensions not affected by the incorporation of the Type A alignment features on the Type B connector bodies are controlled by the IEC 61076-4-101 standard.

Mating information

It shall be possible to mate a Type B receptacle (free board) connector to a Type AB shroud/pin assembly or pin header (fixed board) connector. Type A receptacle (free board) connectors will not mate with Type AB shroud/pin or pin header assemblies. Mating misalignment tolerances shall be in accordance with IEC 61076-4-101.

Accessories
Coding devices cannot be used with the Type AB versions of the IEC 61076-4-101 connectors.

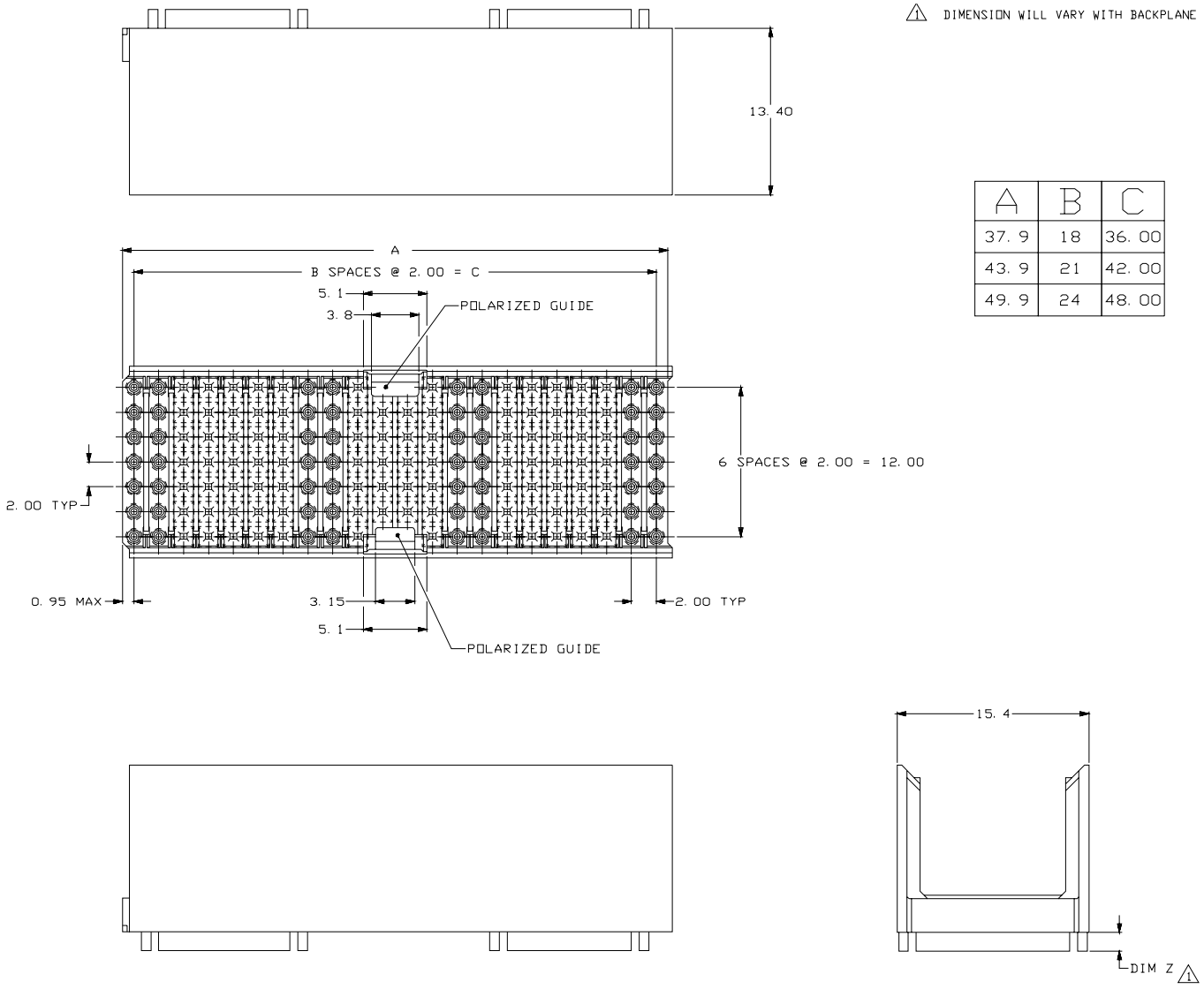
Electrical characteristics
All electrical characteristics (creepage and clearance, voltage proof, current carrying capacity, contact resistance and insulation resistance) shall be in accordance with IEC 61076-4-101.

Mechanical characteristics
All mechanical characteristics (mechanical operation, engaging and separating forces, contact retention, transverse static load, gage retention force, vibration, shock, and polarizing method) shall be in accordance with IEC 61076-4-101.

Application Tooling
Tooling designed for the application of Type A receptacle (free board) connectors can be used to apply Type AB receptacle connectors. Tooling for the Type B receptacle connectors can be used if the design includes a relieved section that provides clearance for the guidance feature on the Type AB connector housing. Some manufacturers provide only one receptacle tooling design (for the Type A) that is used on both the Type A and B receptacle connectors. This can be used to apply the Type AB receptacle connectors to printed boards.
Tooling to press Type AB pin header assemblies onto printed boards differs from that used for both the Type A and Type B pin headers, and tooling designed for the Types A and B pin headers may not function in the Type AB pin headers. In Type AB tooling, provision is required to press contacts into the board in the area that would be reserved for keying in the Type A connectors, allowance must be made to provide clearance for the guidance feature on the outer connector housing walls.

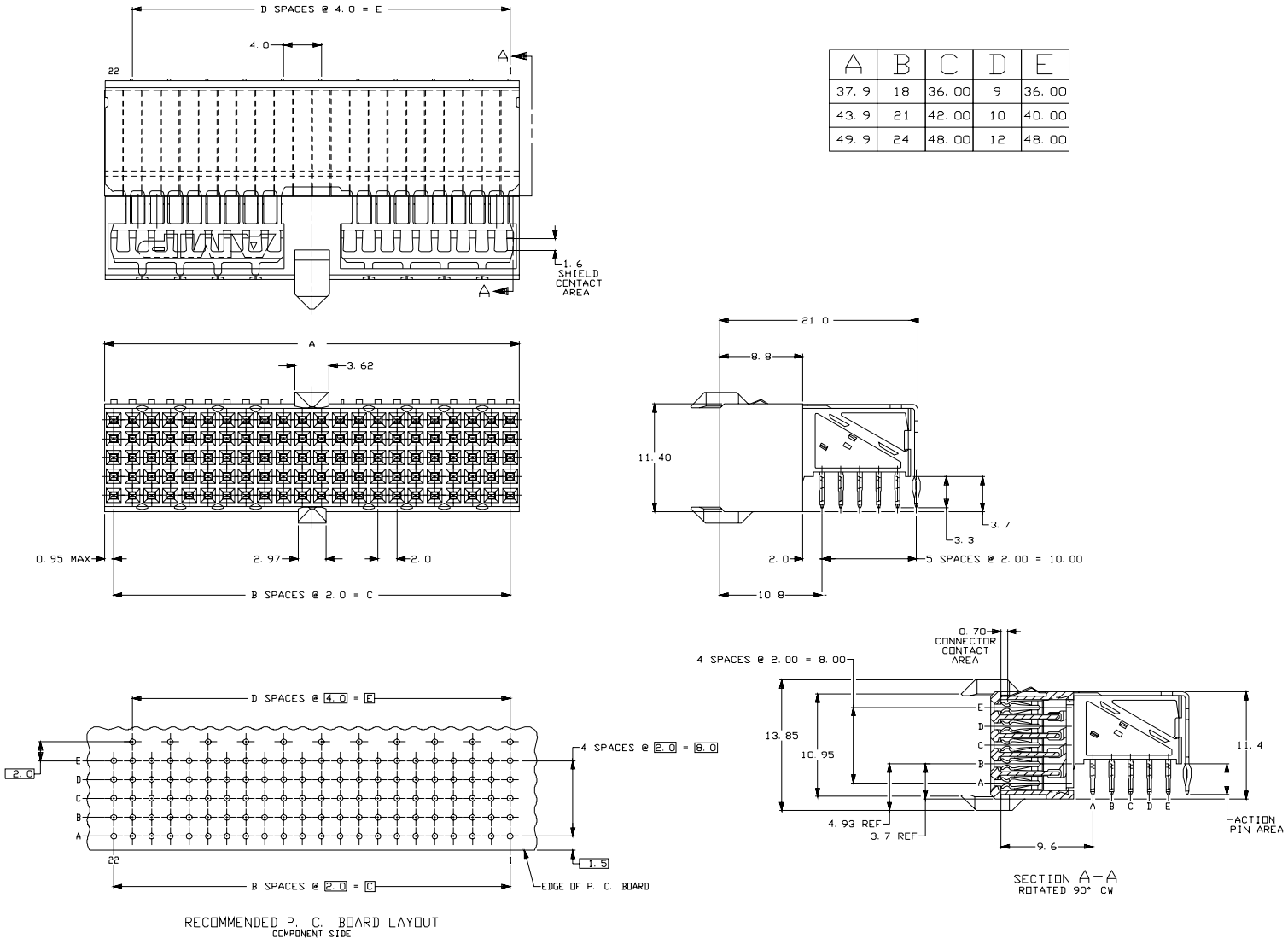
Test schedules
All test schedules shall be in accordance with the applicable sections of IEC 61076-4-101.

Quality assessment procedures
Quality assessment procedures shall be in accordance with IEC 61076-4-101.



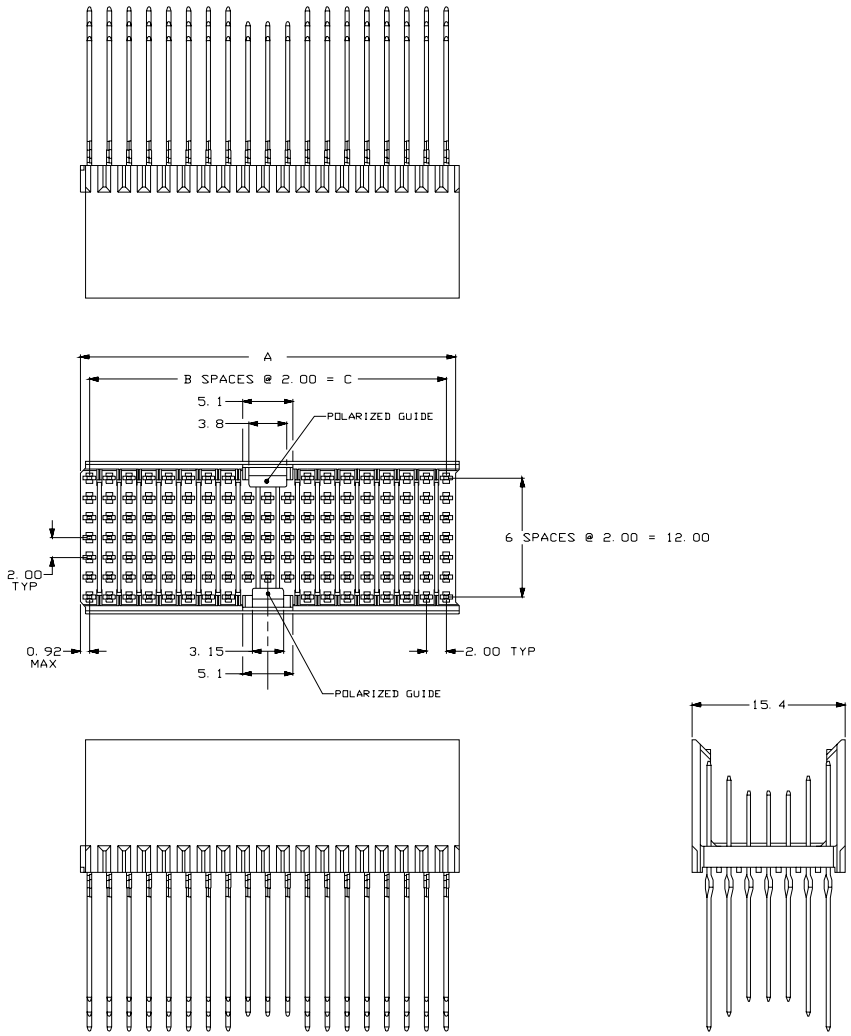
A	B	C
37.9	18	36.00
43.9	21	42.00
49.9	24	48.00

Figure A-2
Shroud



A	B	C	D	E
37.9	18	36.00	9	36.00
43.9	21	42.00	10	40.00
49.9	24	48.00	12	48.00

Figure A-3
Receptacle



A	B	C
37.9	18	36.00
43.9	21	42.00
49.9	24	48.00

Figure A-4
A-B Pin