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SPECTRAL PERFORMANCE OF FREQUENCY MULTIPLIERS AND DIVIDERS

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ABSTRACT

This paper constitutes a review of phase noise performance data accumulated by the authors for commonly used, frequency multiplier (transistor and step-recovery diode impulse generator, and diode and transistor full-wave rectifier doubler) circuits and frequency divider (digital logic-level, analog regenerative and varactor diode) circuits.

The data reveals large variations in the spectral performance exhibited by the various circuit types, and can be used as an important, database guide in the design of low noise, frequency synthesizer hardware.

INTRODUCTION

Low noise signal generator near-carrier spectral performance is usually limited by the corresponding spectral performance achieved in the oscillator(s) incorporated in the hardware. However, as oscillator/resonator short-term frequency stability performance has improved along with increased signal generator capability and circuit complexity, the net, additive effect of necessary use of large numbers of individual signal amplification, frequency addition and subtraction (mixer), and frequency multiplication and division stages often limits attainable output signal spectral performance.

With regard to frequency multiplication and division circuitry, it is usually necessary to tradeoff frequency synthesis circuit spectral performance with other circuit performance parameters including bandwidth, cost, complexity, efficiency, reliability, etc. Intelligent design choices require knowledge of the spectral performance characteristics attainable using alternative frequency multiplier and divider circuitry and an understanding of the mechanisms involved that determine device phase noise performance.

IMPULSE GENERATION-TYPE FREQUENCY MULTIPLIERS

1. Step Recovery Diode Frequency Multipliers

Step recovery diodes (SRD) are usually used for single-step, high-order (multiplication factor) signal frequency multiplication. The SRD operates as a charge-controlled switch. A forward diode bias stores charge, and a reverse bias depletes the stored charge. In the SRD, current conduction turn-off occurs fast enough to produce an extremely narrow, impulse-like, output waveform. For periodic (sinusoidal) diode excitation, the output signal frequency "comb" spectrum consists of harmonics of the input signal extending from the input frequency to the reciprocal of the output waveform, impulse width. Used as a frequency multiplier, the desired, input signal harmonic is extracted via a bandpass filter. Coaxial-connectorized, self-contained, SRD comb generator modules are available from several suppliers, and standard input/output frequency ranges extend from 100 MHz (input) to 25 GHz (output). Device input impedance matching bandwidths are relatively narrow, and recommended input drive and per-harmonic output power levels lie in the range 20 to 27 dBm and 0 to -20 dBm, respectively [1–3].

Experiments conducted at Westinghouse indicate that lossless (direct) connection of the harmonic selection, bandpass filter to the SRD output, as well as attempts to increase multiplier efficiency by optimizing the match at the diode output-bandpass filter interface, can result in significant increase in multiplier phase noise. Use of isolators and/or circulators at the SRD output do not always constitute a solution, owing to device bandwidth limitations. Use of a small amount of broadband, resistive attenuation at the interface for controlling the effective diode load impedance at all output signal spectral component frequencies results in uniform, improved, phase noise performance. Figures 1 and 2 show the results of measurement of (times ten multiplication) SRD multipliers, operating at 100 MHz and 1 GHz input frequency. Figure 1(b) shows the phase noise performance of the 100 MHz–1.1 GHz multiplier with SRD direct (lossless connection between the diode and output bandpass filter. As shown in the figure, the result is a 50 dB increase in white phase noise (floor) level. For the 1–10 GHz multiplier phase noise measurements (figure 2), the X-Band, GaAs, output amplifiers constitute the dominant source of additive, flicker-of-phase noise. In contrast to figure 1, figure 3 shows the results of additive phase noise measurements made a number of years ago by Hewlett-Packard for a pair of times twenty (100 MHz–2 GHz), SRD multipliers [4].

2. Narrow Pulse Generation, Transistor Frequency Multipliers

High-order multiplication can also be accomplished (at lower frequency ranges than those used with the SRD) using transistor circuits. Figure 4 shows a simplified schematic diagram for a 10 MHz to 80 MHz multiplier fabricated and tested specifically for the purpose of the additive phase noise performance for this class of multiplier circuit. As shown in

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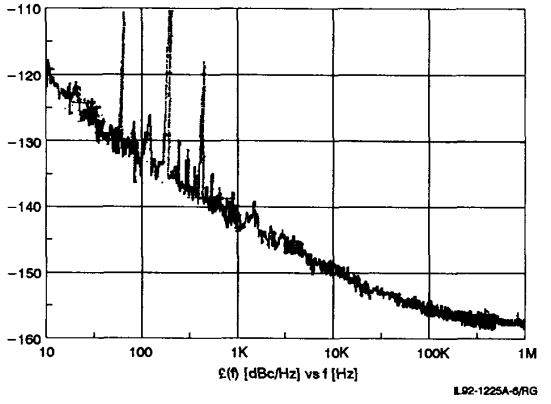

Figure 1(a). Phase Noise Measurement Results for a Pair of Times Eleven (100 MHz – 1.1 GHz) Step Recovery Diode Multipliers

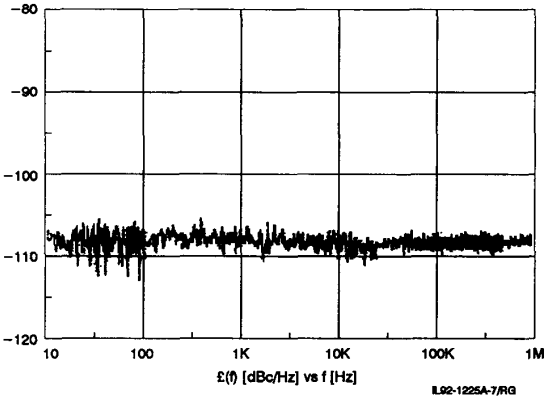

Figure 1(b). Phase Noise Measurement Results for the Figure 1(a) Multipliers with Lossless Connection Between Diode and Output Filter

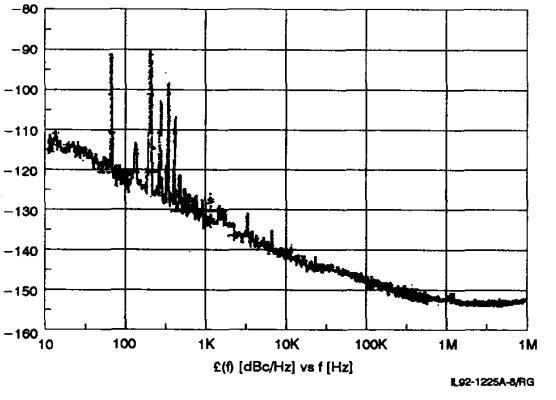

Figure 2. Phase Noise Measurement Results for a Pair of Times Ten (1 – 10 GHz) Step Recovery Diode Multipliers

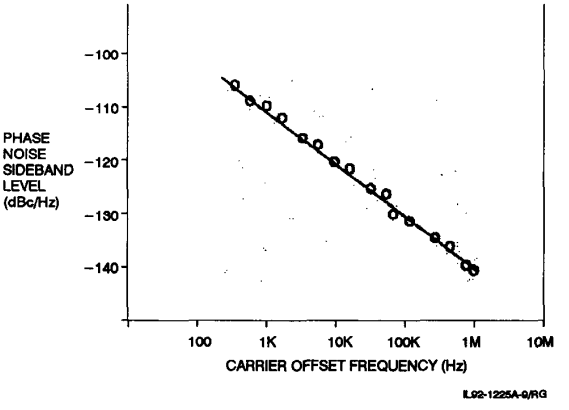

Figure 3. Phase Noise (Hewlett-Packard) Measurement Results for a Pair of Times Twenty (100 MHz – 2 GHz) Step Recovery Diode Multipliers

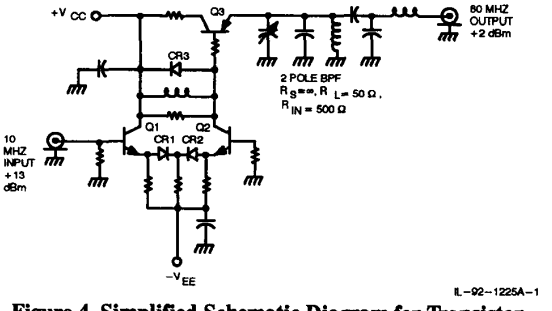

Figure 4. Simplified Schematic Diagram for Transistor "Impulse" Generation Type Frequency Multiplier

the figure, the impulse-generating portion of the circuit consists of two, emitter-coupled, switching transistors. In order to increase switching speed, the circuit incorporates a pair of schottky diodes and is arranged so that the transistors conduct during the entire waveform cycle. A single-ended, "impulse" waveform is created by differentiating the transistor, "square wave" collector current using a inductor/resistor/diode combination. A class-C, output amplifier with a multipole, bandpass output matching structure is used for waveform amplification and desired signal harmonic extraction. The circuit is similar in nature to one first described by Dick Baugh in 1972 [5]. Figure 5 shows the measured phase noise performance for a pair of the figure 4, test circuits. As shown in the figure, the per-device, phase noise floor level, referred to the input frequency, is -166 dBc/Hz and is likely a result of un-optimized, relatively small, class-C amplifier drive level. To the extent that the output amplifier of the figure 4 circuit conducts over a small portion of the input signal period, one might expect to obtain similar spectral performance from frequency multipliers designed using sinusoidal excitation, small conduction angle, transistor amplifiers. With regard to flicker-of-phase noise, the results shown in figure 5 are 15 dB

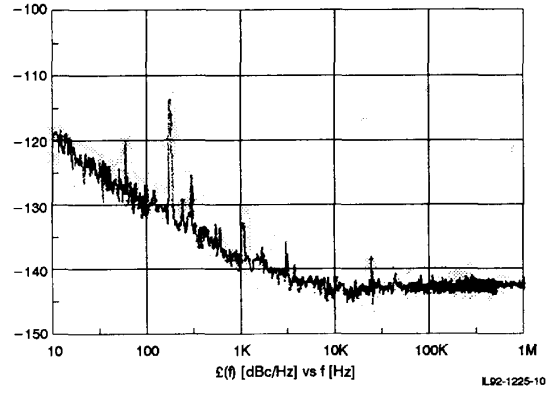

Figure 5. Phase Noise Measurement Results for a Pair of Times Eight (10 – 80 MHz) Transistor Impulse Generation Type Multipliers

poorer, compared to the (1 MHz input frequency) Baugh multiplier, which additionally incorporated an emitter-coupled, zero-crossing detector-type output limiter.

FULL WAVE RECTIFIER-TYPE, FREQUENCY DOUBLERS

1. Diode Doublers

Multiple-decade bandwidth, schottky diode-type, frequency doublers are available as standard, vendor components that operate over the HF to microwave frequency region. Doubler conversion loss is approximately 10 dB, and units are available for optimized efficiency at moderate (10 dBm) and high (23 dBm) input drive levels. Similar performance can and has been obtained by splitting the input signal and driving two ports of a double-balanced mixer. Doubler spectral performance, in terms of flicker-of-phase noise, is excellent, but varies with the type of diodes used and, to a much lesser extent, with device operating frequency [6].

In general, use of individual, cascaded stages of schottky diode-type, frequency doublers and low, flicker-of-phase noise, interstage amplifiers provides best obtainable, frequency multiplier spectral performance. Figures 6 to 8 show the phase noise performance obtained for low drive level diode doublers, high drive level diode doublers, and for a pair of times-sixteen, frequency multipliers incorporating a cascade of four similar type doublers. For the times-sixteen multipliers, the 2.56 GHz, silicon bipolar, doubler interstage amplifier used constituted the dominant source of multiplier flicker-of-phase noise [7].

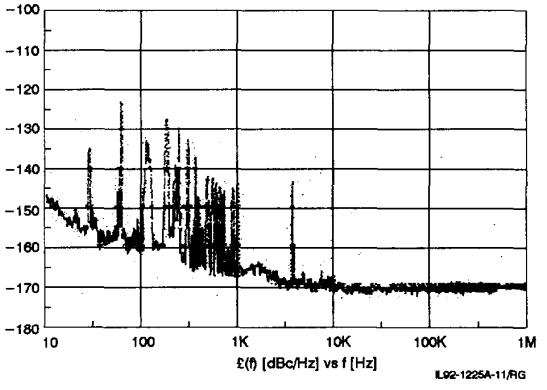

Figure 6. Phase Noise Measurement Results for a Pair of (13 dBm Drive Level, 100 – 200 MHz) Schottky Diode Frequency Doublers with Output Amplifiers

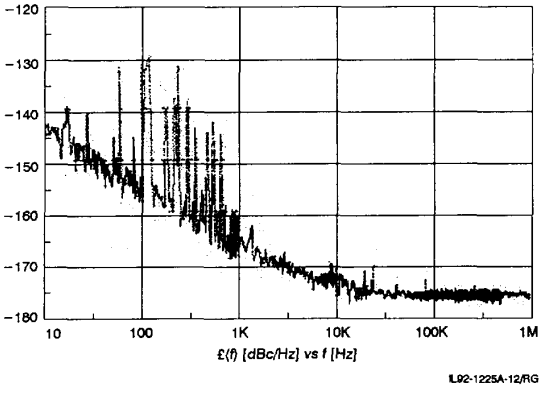

Figure 7. Phase Noise Measurement Results for a Pair of (23 dBm Drive Level, 80 – 160 MHz) Schottky Diode Frequency Doublers

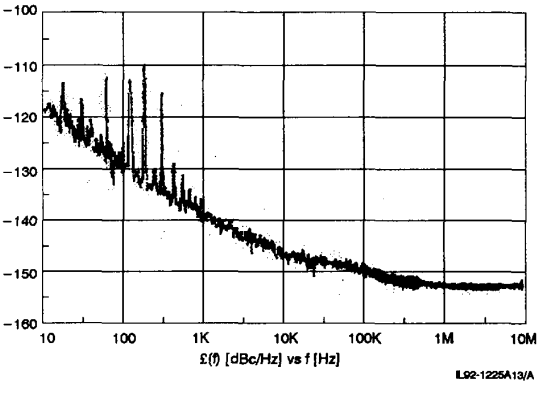

Figure 8. Phase Noise Measurement Results for a Pair of Times Sixteen (640 MHz – 10.24 GHz) Frequency Multipliers Incorporating Cascaded Stages of Schottky Diode Doublers with Interstage Amplifiers and Bandpass Filters

2. Transistor Doublers

Class C, transistor amplifiers can be arranged in a "push-push" circuit configuration to perform frequency doubling in much the same manner as the diode doubler. In the case of the transistor doubler, there is a net conversion gain of typically 6 to 10 dB. Figure 9 shows a simplified schematic diagram for the transistor doubler, and figure 10 shows additive phase noise measurement results for a pair of 80 MHz–160 MHz, transistor doublers. As shown in the figure, both the flicker-of-phase and white phase noise performance of the transistor doubler are poorer than those exhibited by the schottky diode doublers. In the case of the transistor doublers, phase noise performance is influenced by transistor type, drive level, operating frequency, and emitter degeneration [6,8].

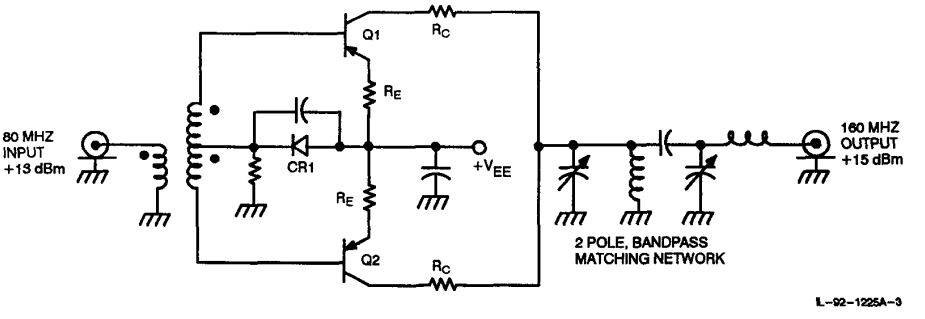

Figure 9. Simplified Schematic Diagram for a Transistor "Push-Push" Type Frequency Doubler

Figure 11 shows a summary of the measurement results obtained for various types of frequency multipliers. As can be seen from the figure, there is a wide variation in device type near-carrier and noise floor performance, with the schottky diode doublers exhibiting lowest noise performance, but also lowest multiplication factor. Multiplier circuit spectral performance must therefore be traded off against other circuit performance parameters such as overall circuit cost, complexity, and power consumption.

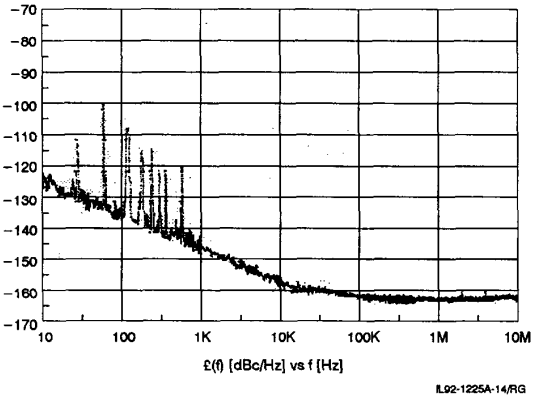

Figure 10. Phase Noise Measurement Results for a Pair of (13 dBm Drive Level, 80 – 160 MHz) Transistor "Push-Push" Type Frequency Doublers

VARACTOR DIODE FREQUENCY DIVIDERS

Varactor diode or parametric, frequency dividers (and multipliers) are well-known [1,9–10]. Although various analyses of circuit operation have been described in detail in the literature, not much information is available with regard to circuit phase noise performance. The divide-by-two, varactor frequency divider operates by generating negative conductance at half the input (diode pump) frequency. A generalized block diagram is shown in figure 12. Experiments performed at Westinghouse using a straightforward, 'cookbook' design for a relatively low frequency (40 MHz to 20 MHz) divider indicated: (1) optimum efficiency is typically

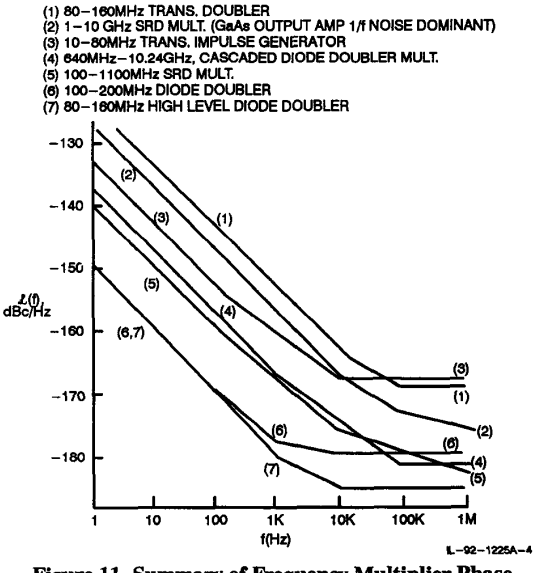

Figure 11. Summary of Frequency Multiplier Phase Noise (Referred to Device Input) Measurement Results

obtained for moderately high (20 dBm) input drive levels, (2) input and output matching networks are relatively narrow-band, owing to the large ratio between diode and generator/load resistances, (3) in spite of matching network losses, divider efficiency is quite good, and (4) compared to digital, logic-level dividers, varactor divider flicker-of-phase noise level is similar, and white phase noise (floor) level is much lower [9]. Figure 13 shows the additive phase noise spectra measured for the (figure 12) divider circuits.

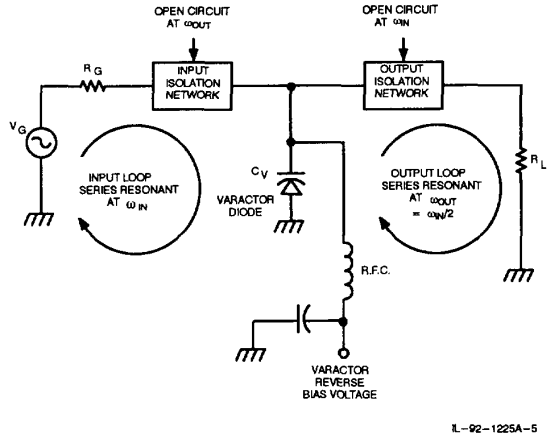

Figure 12. Simplified Schematic Diagram for a Varactor Diode Type (Divide-by-Two) Frequency Divider

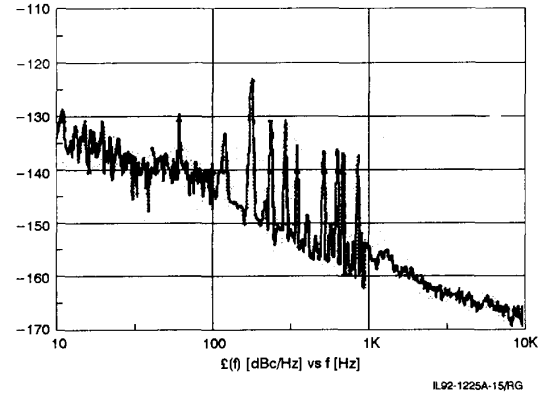

Figure 13. Phase Noise Measurement Results for a Pair of Varactor Diode Type (40–20 MHz) Frequency Dividers

REGENERATIVE FREQUENCY DIVIDERS

Regenerative frequency (divide-by-two) division, while not providing the (divide ratio) versatility of digital, logic level devices, offers several important circuit performance advantages [1,11–13]. As shown in figure 14, the regenerative divider acts as an oscillator operating at the output frequency and incorporates a frequency conversion (double-balanced

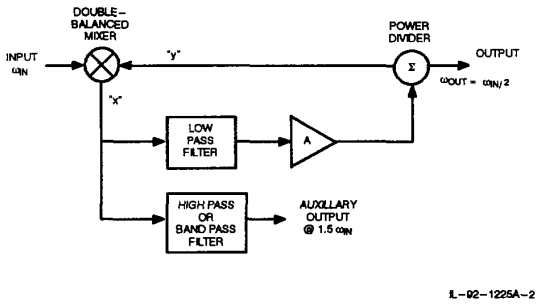

Figure 14. Simplified Schematic Diagram for a Regenerative Type (Divide-by-Two) Frequency Divider

mixer) in the oscillator positive feedback loop signal path. Steady-state, loop (unity) gain and (2Nπ radians) phase requirements are the same as for a conventional, feedback loop oscillator, except that the requisite signal phase shift across the mixer (from nodes x to y in figure 14) occurs when the oscillating output signal assumes the corresponding, requisite time relationship with that of the input signal. Although conditions for stable circuit operation have been defined differently, depending on circuit analysis approach, a common point of agreement is that widest, stable operating bandwidth requires use of minimal loop signal propagation/group delay. Analyses of divider signal phase relationships show that the loop amplifier and mixer open-loop, flicker-of-phase noise sideband level is reduced by 6 dB at the divider output [13]. The circuit can be configured so that mixer conversion loss is feedback signal level-dependent. The mixer can therefore provide the requisite loop AGC mechanism so that steady-state operation is obtained for signal levels below those driving the loop amplifier into gain compression. The advantages of the regenerative divider include: (1) very low flicker-of-phase noise and noise floor performance (coincident with use of high compression point mixers and loop amplifiers exhibiting low flicker-of-phase noise, (2) typical octave, stable operating bandwidth, and (3) straightforward design using 50-ohm modular components. In addition, a potentially useful, second output signal at 1.5 times the input signal frequency is available at the mixer output.

Figure 15 shows the (typical) measured phase noise performance for a pair of VHF regenerative dividers designed at Westinghouse [11].

DIGITAL, LOGIC-LEVEL DIVIDERS

Due to low cost and design flexibility, logic dividers play an important role in both commercial and military frequency synthesis applications. Bipolar, fixed-modulus dividers are available with input frequencies up to 2.5 GHz, dual-modulus dividers with input frequencies up to 1 GHz, and fully programmable counters and dividers with input frequencies up to 600 MHz.

Logic divider phase noise characteristics are normally not vendor-specified. As is the case with many types of analog frequency synthesis components such as RF amplifiers, mixers, frequency doublers, it is necessary, then, to accumulate a "library" of phase noise performance data on a variety of

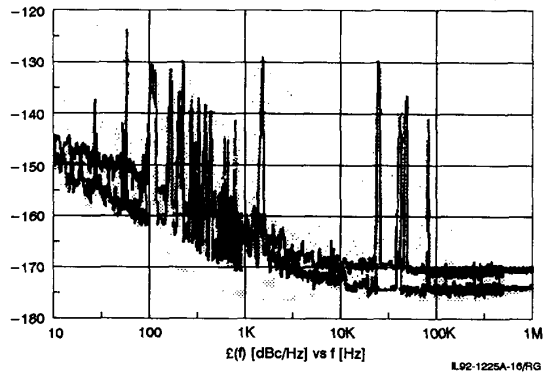

Figure 15. Phase Noise Measurement Results for a Pair of Regenerative (160 – 80 MHz) Frequency Dividers. Top Curve: Measured Performance for Two Dividers. Bottom Curve: Measured Instrumentation Noise Level

candidate devices. The following portion of this paper contains a brief analysis of phase noise characteristics followed by measurement results.

1. Analysis

In a logic divider output, transitions occur in response to a clock input signal. Phase noise is a measure of unpredictable, random variations in transition times at the output for a well defined input and can be modelled in the following way. In figure 16, the solid-lined waveform represents an ideal output response, and the dashed-lined waveform represents an actual response. The difference is a sequence of narrow, random-amplitude pulses which characterize the noise. The delay variations in figure 16 are exaggerated. In practice, delay variations are on the order of a few picoseconds and the rise and fall times on the order of a few nanoseconds, so that, to a good approximation, the width of a particular noise pulse is equal to the rise or fall time of the output signal and the amplitude $A_n = \Delta\tau_n\, dV/dt$ is proportional to the random variations in delay. It is convenient to suppose that the noise pulse train repeats every second so that a Fourier series representation of the n^{th} pulse consists of discrete frequencies at 1 Hz intervals. The power spectral density of this pulse is:

$$S_{nk} = 2A_n^2 t_r^2 \frac{\sin^2(\pi f_k t_r)}{(\pi f_k t_r)^2} \qquad (1)$$

If the risetime t_r is small compared to the period of the output waveform, the spectral density of the frequency components close to the carrier can be approximated by:

$$S_{nk} = 2(A_n t_r)^2 = 2(\Delta\tau_n \frac{dV}{dt} t_r)^2 = 2(\Delta\tau_n V)^2 \qquad (2)$$

Also, if the random variations in the output are uncorrelated pulse-to-pulse, the power spectral density of the entire noise pulse train is the sum of the spectral densities of the individual pulses,

$$S_k = \sum_{n=1}^{2f_c} 2\Delta\tau_n^2 V^2 = 4f_C(\Delta\tau_{RMS})^2 V^2 \qquad (3)$$

where f_c is the frequency of the output waveform. Finally, if the ideal output response is approximated by a square wave, the ratio of the noise power spectral density to the fundamental component of the output signal is

$$\mathcal{L}(f) = 10\ log[2\pi^2 f_c(\Delta\tau_{RMS})^2] \qquad (4)$$

This result characterizes single-sideband, wideband phase noise in logic devices in terms of the frequency of the output signal and the RMS jitter; it is independent of risetime and, in general, insensitive to the transition characteristics of the output signal.

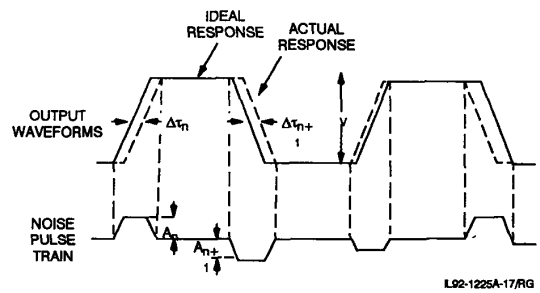

Figure 16. Representation of Divider Wideband Phase Noise as a Narrow Pulsewidth, Pulse Train

If the input to a divider is corrupted with wideband phase noise, the effect of the divider is to reduce the frequency f_c so that a noiseless divider would reduce phase noise at the output by 10 logN where N is the divide ratio. If the delay variations in figure 16 are correlated pulse-to-pulse then the noise is characterized as narrowband. In this case, the effect of a noiseless divider is to reduce the phase noise by 20 logN. From a frequency point of view, phase noise improvement in the wideband case is degraded by folding of the frequency components about zero frequency.

2. Measurement Results

Table 1 summarizes additive phase noise obtained for a number of different logic dividers. The table includes measurements on comparators and translators because it is often convenient to use these devices in practical designs. Figures 17 and 18 show actual measurement data obtained for ACT CMOS and ECL dividers. These are two source measurements. Assuming equal noise contributions from each device, per-device phase noise levels are 3 dB lower than indicated by the plots. The table 1 results are consistent with results obtained by others and available in published literature [6, 14–15].

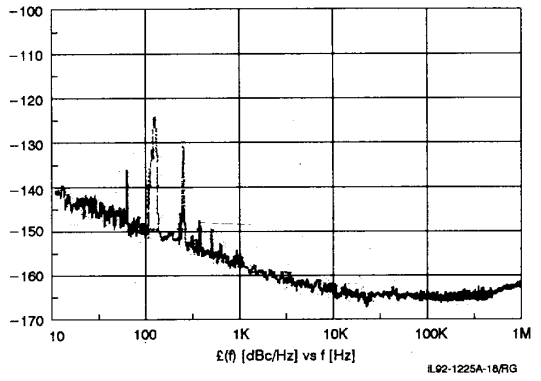

Figure 17. Phase Noise Measurement Results for a Pair of CMOS ACT (Divide-by-Four, 20 – 5 MHz) Frequency Dividers

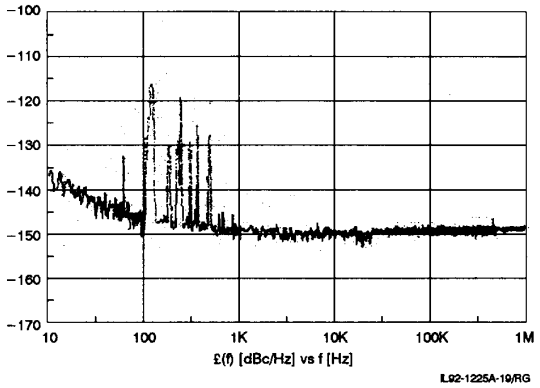

Figure 18. Phase Noise Measurement Results for a Pair of ECL (Divide-by-Eight, 400 – 50 MHz) Frequency Dividers

Table 1. Summary of Phase Noise Measurement Results (Referred to Device Output) for Logic Dividers

DEVICE	DESCRIPTION	OUTPUT LOGIC LEVEL	OUTPUT FREQUENCY (MHz)	$\mathcal{L}$(f) FLOOR (dBc/Hz)	$\mathcal{L}$(f) @100 Hz (dBc/Hz)
10H125	TRANSLATOR	TTL	20	161	153
LT1016	COMPARITOR	TTL	12	152	150
74ACT161	DIVIDE-BY-4	TTL	5	169	153
74HC161	DIVIDE-BY-4	TTL	5	166	150
74AS161	DIVIDE-BY-4	TTL	5	162	152
74F161	DIVIDE-BY-4	TTL	5	163	152
74LS161	DIVIDE-BY-4	TTL	5	157	151
74161	DIVIDE-BY-4	TTL	5	157	151
10115	RECEIVER	ECL	12	159	156
MC12011	DIVIDE-BY-8	ECL	50	153	150
SP8828	DIVIDE-BY-8	ECL	60	149	145
SP8828	DIVIDE-BY-8	ECL	230	141	134
SP8818	DIVIDE-BY-8	ECL	60	154	148
SP8818	DIVIDE-BY-8	ECL	230	149	141

CONCLUSIONS

For frequency multiplication circuitry, schottky diode doublers exhibit lowest overall phase noise performance over the entire HF through microwave frequency range. Unfortunately, per-device multiplication factor is lowest. In contrast, SRD multipliers offer single-step, high-order multiplication but poorer noise performance, compared to the diode doublers. When consideration is given to necessary use of interstage amplifiers in high-order multipliers using cascaded doublers, the SRD approach is superior from a DC power consumption standpoint.

Ironically, a similar situation exists for frequency division circuitry, with analog regenerative (divide-by-two) dividers providing superior noise performance, compared to (higher division ratio) logic dividers.

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