2 Practical PCB Design Rules

Because many things can affect transmission lines, EMI problems can occur. In order to reduce these problems, good PCB design is important and with some simple design rules, the PCB designer can minimize these problems. It is important to make prudent decisions during new circuit design, like the minimum number of layers. The easiest way to get a good, new design is to copy the recommended design from the TI evaluation modules (EVM).

A good PCB layout starts with the circuit design. Do not postpone considerations about the layout. One of the most important aspects affecting the layout is the location of each functional block. Keep their devices and their traces together.

2.1 PCB Considerations During the Circuit Design

- What is the highest frequency and fastest rise time in the system?
- What are the electrical specifications at the inputs and outputs of the sinks and sources?
- Are there sensitive signals to route – for example, think about controlled impedance, termination, propagation delay on a trace (clock distribution, buses, etc.)?
- Is a microstrip adequate for the sensitive signals, or is it essential to use stripline technique?
- How many different supply voltages exist? Does each supply voltage need its own power plane, or is it possible to split them?
- Create a diagram with the functional groups of the system – e.g., transmitter path, receiver path, analog signals, digital signals, etc.
- Are there any interconnections between at least two independent functional groups? Take special care of them. Think about the return current and crosstalk to other traces.
- Clarify the minimum width, separation and height of a trace with the PCB manufacturer. What's the minimum distance between two layers? What about the minimum drill and the requirements of vias? Is it possible to use blind vias and buried vias?

Equipped with this information, a designer can do a lot of basic design.

2.2 Board Stackup

There is no fundamental information about how many layers should be used and how the board stackup should look. Again, the easiest way the get good results is to use the design from the EVMs of Texas Instruments. The magazine *Elektronik Praxis* [11] has published an article with an analysis of different board stackups. These are listed in Table 3 and Table 4.

Generally, the use of microstrip traces needs at least two layers, whereas one of them must be a GND plane. Better is the use of a four-layer PCB, with a GND and a VCC plane and two signal layers. If the circuit is complex and signals must be routed as stripline, because of propagation delay and/or characteristic impedance, a six-layer stackup should be used.

Table 3. Possible Board Stackup on a Four-Layer PCB

	Model 1	Model 2	Model 3	Model 4
Layer 1	SIG	SIG	SIG	GND
Layer 2	SIG	GND	GND	SIG
Layer 3	VCC	VCC	SIG	VCC
Layer 4	GND	SIG	VCC	SIG
Decoupling	Good	Good	Bad	Bad
EMC	Bad	Bad	Bad	Bad
Signal integrity	Bad	Bad	Good	Bad
Self disturbance	Satisfaction	Satisfaction	Satisfaction	High

Table 4. Possible Board Stackup on a Six-Layer PCB

	Model 1	Model 2	Model 3	Model 4	Model 5	Model 6
Layer 1	SIG	SIG	GND	SIG	SIG	SIG
Layer 2	SIG	GND	VCC	GND	GND	GND
Layer 3	VCC	VCC	SIG	VCC	VCC	VCC
Layer 4	GND	VCC	SIG	SIG	GND	GND
Layer 5	SIG	GND	VCC	GND	Not used	SIG
Layer 6	SIG	SIG	GND	SIG	SIG	SIG
Decoupling	Good	Good	Good	Good	Good	Good
EMC	Bad	Good	Satisfaction	Satisfaction	Good	Good
Signal integrity	Bad	Good	Bad	Good	Good	Bad

To determine the right board stackup, consider the following points:

- Define the location of each section on the board by means of the functional diagram. Try to keep the devices together to avoid interaction (crosstalk, influence of noise) between two separate blocks (like transmitter–receiver or analog–digital).
- At which functional block is which supply voltage used?
- It is necessary in high-speed designs to have at least one complete ground plane as a reference for microstrip traces for sensitive signals.
- With a complete power plane as close as possible to the ground plane, it is possible to create capacitive coupling between them to get low impedance at high frequencies. This reduces the amount on small decoupling capacitors at the power pins of the devices. The closer the planes, the less impedance is present [13].

2.3 Power and Ground Planes

As previously mentioned, a complete ground plane in high-speed design is essential. Additionally, a complete power plane is recommended as well. In a complex system, several regulated voltages can be present. The best solution is for every voltage to have its own layer and its own ground plane. But this would result in a huge number of layers just for ground and supply voltages. What are the alternatives? Split the ground planes and the power planes? In a mixed-signal design, e.g., using data converters, the manufacturer often recommends splitting the analog ground and the digital ground to avoid noise coupling between the digital part and the sensitive analog part.

Take care when using split ground planes because:

- Split ground planes act as slot antennas and radiate.
- A routed trace over a gap creates large loop areas, because the return current cannot flow beside the signal, and the signal can induce noise into the nonrelated reference plane (Figure 7).
- With a proper signal routing, crosstalk also can arise in the return current path due to discontinuities in the ground plane. Always take care of the return current (Figure 10).

Figure 7: Do not route a signal referenced to digital ground over analog ground and vice versa. The return current cannot take the direct way along the signal trace and so a loop area occurs. Furthermore, the signal induces noise, due to crosstalk (dotted red line) into the analog ground plane.

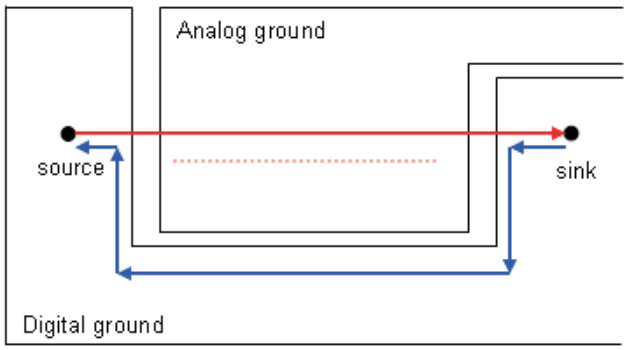

Figure 7. Loop Area and Crosstalk Due to Poor Signal Routing and Ground Splitting

Figure 8: Do not let one ground plane pass another ground plane to get connected to the common ground (a). Every ground plane must have its own path to the common ground to reduce noise (b).

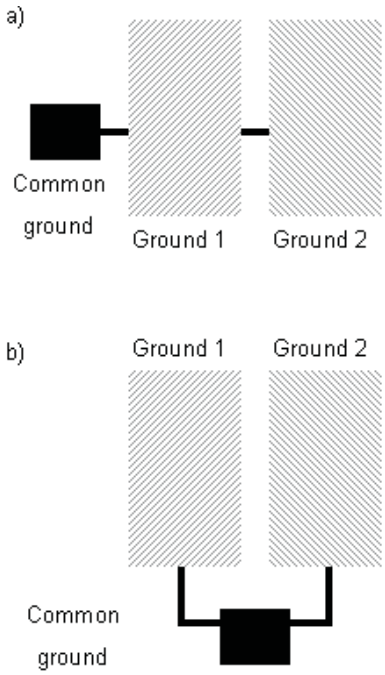

Figure 8. Poor and Good Placement of the Common Ground in a Split Ground Environment

Figure 9: The use of a complete ground plane is a better solution. Place the devices by function and route their signals only in their region. If any interconnection between analog and digital occurs, be careful with crosstalk and the return current path.

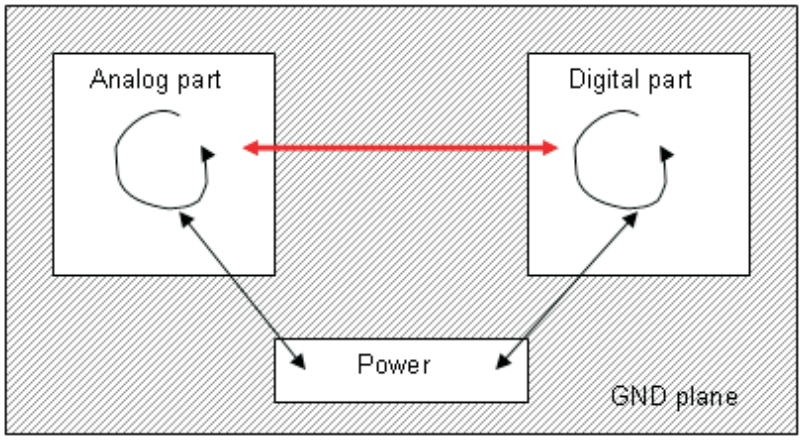

Figure 9. Good Placement of Different Functional Blocks Without the Need of a Split Ground Plane

Figure 10: If the trace routing of two signals is done properly, it is still possible to induce noise in the return current path by means of crosstalk. In this case, a loop area and crosstalk in the return current path have been created.

- If possible, use a continuous ground plane; do not split them. This can be achieved by a proper placement selection. Again, create functional blocks, and place and route them together. By doing this, the traces of a digital part cannot influence any trace of the analog part if these sections do not cross each other.

If split ground planes are essential:

- Do not route signals over a gap. Always strive for the return current flow with the smallest loop area.
- Connect split ground planes only at one point. More common ground connections can create ground loops, and this increases radiation.
- The return current of a subsystem (e.g., an analog system or transmitter path) must not be in the path of the other subsystem (digital system or receiver path). The return current should flow directly to the common ground point (Figure 8).
- Power planes should only reference their own ground plane. They should not overlap with another ground plane. This leads to capacitive coupling between the power plane and a not-referenced ground plane. Noise can couple into the other system.
- Do not connect bypass capacitors between a power plane and an unrelated ground plane. Again, noise can be coupled from one supply system into the other. This mistake can occur in the circuit design section.

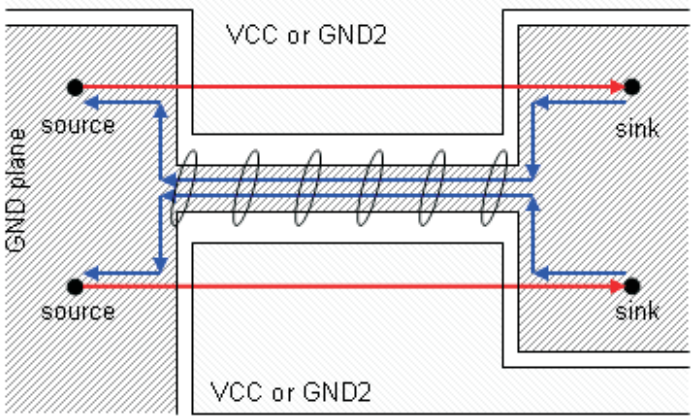

Figure 10. Crosstalk Induced by the Return Current Path

2.4 Decoupling Capacitors

Decoupling capacitors between the power pin and ground pin of the device ensure low ac impedance to reduce noise and to store energy. To reach low impedance over a wide frequency range, several capacitors must be used. This is why, a real capacitor consists of its capacitance and a parasitic inductance and resistance. Therefore, every real capacitor behaves as a resonant circuit. The capacitive characteristics are only valid up to its self-resonant frequency (SRF). Above the SRF, the parasitic effects dominate, and the capacitor acts as an inductor. With the use of several capacitors with different values, low ac impedance over a wide frequency range can be provided.

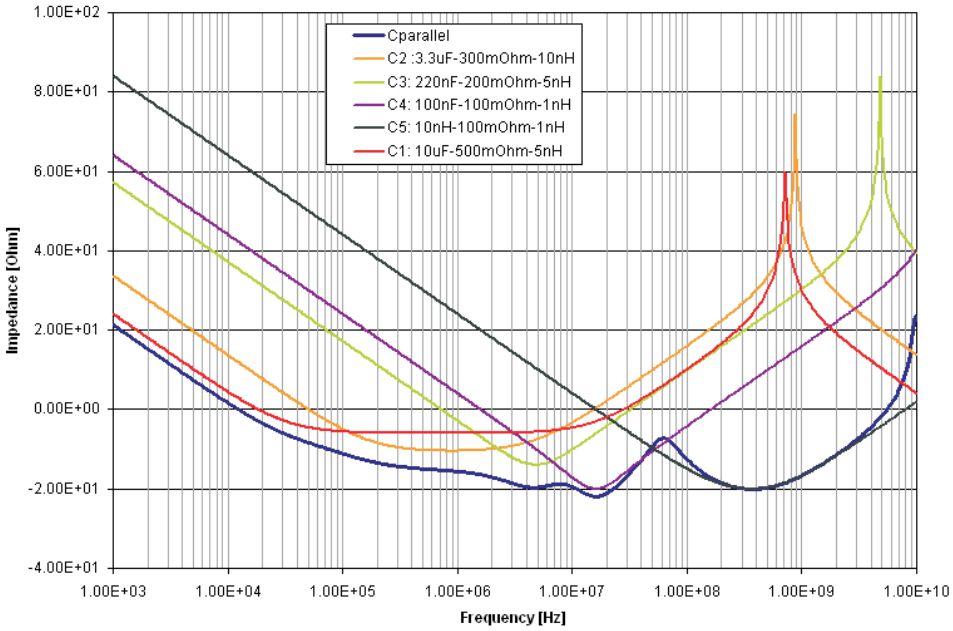

Figure 11. Impedance of Different Capacitors Over a Wide Frequency Range and the Resulting Impedance of Their Parallel Connection

Figure 11 shows this context. Capacitors with high values have low impedance in the lower frequency range and a low SRF, whereas small-valued capacitors have their SRF in the upper frequency range. This depends on the equivalent series resistance (ESR) and the equivalent series inductance (ESL). A good combination of several capacitors leads to a low impedance over a wide frequency range. This is shown with the *Cparallel* curve in Figure 11. The *gap* (increase of the impedance) at around 60 MHz is the result of a missing capacitance. If there were a value between 100 nF and 10 nF, the Cparallel curve would not increase.

As previously mentioned, a power and GND plane can represent a capacitance that ensures low impedance at high frequencies. Therefore, a well-designed board stackup can minimize the number of capacitors required having low-capacitance values.

General rules for placing capacitors:

- Place the lowest valued capacitor as close as possible to the device to minimize the inductive influence of the trace. This is especially important for small capacitor values, because the inductive influence of the trace is not negligible anymore.
- Place the lowest valued capacitor as close as possible to the power pin/power trace of the device.
- Connect the pad of the capacitor directly with a via to the ground plane. Use two or three vias to get a low-impedance connection to ground. If the distance to the ground pin of the device is short enough, you can connect it directly.
- Make sure that the signal must flow along the capacitor.

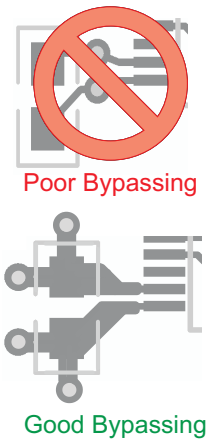

Figure 12. Poor and Good Placement and Routing of Bypass Capacitors

2.5 Traces, Vias, and Other PCB Components

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner, and the characteristic impedance changes. This impedance change causes reflections.

- Avoid right-angle bends in a trace and try to route them at least with two 45° corners. To minimize any impedance change, the best routing would be a round bend (see Figure 13).
- Separate high-speed signals (e.g., clock signals) from low-speed signals and digital from analog signals; again, placement is important.
- To minimize crosstalk not only between two signals on one layer but also between adjacent layers, route them with 90° to each other.

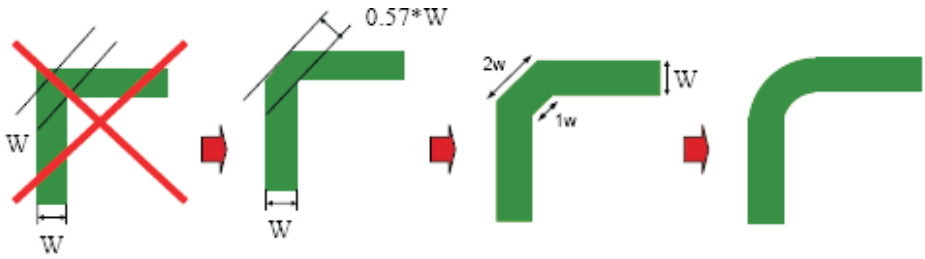

Figure 13. Poor and Good Right Angle Bends

The use of vias is essential in most routings. But the designer has to be careful when using them. They add additional inductance and capacitance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length.

- Avoid vias in differential traces. If it is impossible to avoid them, use vias in both traces or compensate the delay also in the other trace.

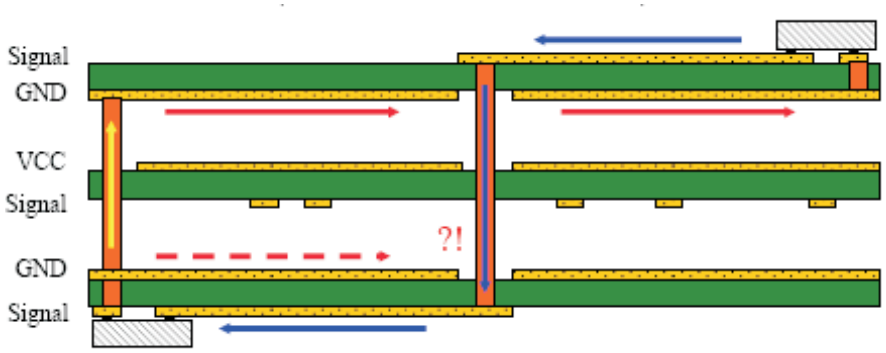

Figure 14. Loop Areas Caused by Poor Via Placement

Figure 14 illustrates another problem with vias – loop areas. The designer has to make sure that the return current can flow ideally underneath (beside) the signal trace. A good way to realize this is to add some ground vias around the signal via. This is a similar structure to a coaxial line. Care must be taken, if the new layer has another distance to the reference plane. This can cause reflections due to an impedance change.

Figure 15 shows, how good via placement avoids loop areas, if there is need for multiple vias.

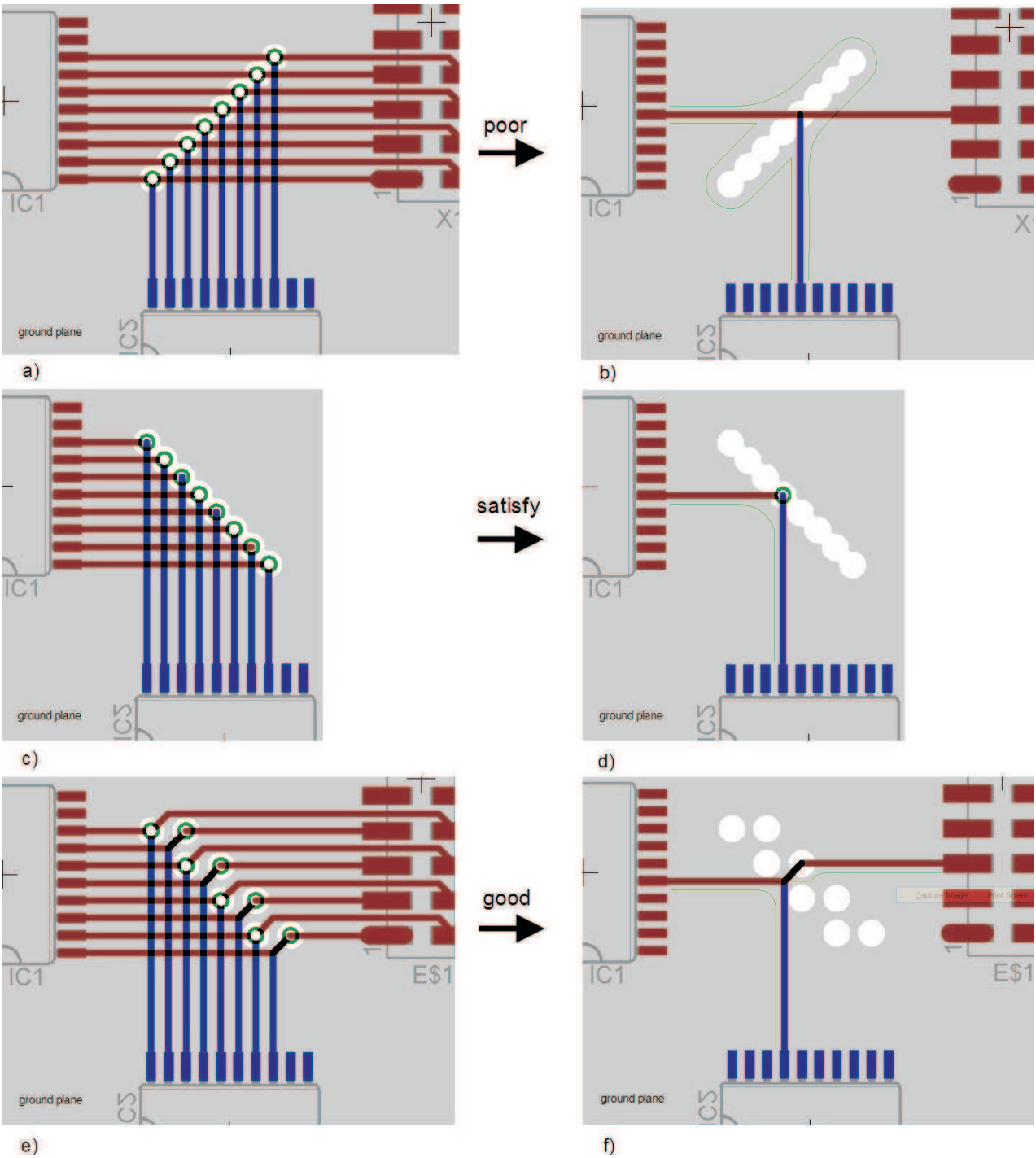

Figure 15. Poor and Good Via Placement

Figure 15: Because of wrong via placement, especially with bus signals, slots in the ground plane can arise. Further, the return current can create a loop area when placing the vias in the wrong direction. Three different routings are shown on the left. On the right, some traces are masked out to see how the return current (green trace) will flow.

In Figure 16, a four-layer stackup can be seen. The signal changes from layer 1 to layer 2. The via passes through all four layers. Thus, we get the structure of an open-end transmission line with no termination

and thereby a 100% reflection. Due to the length of the stub, a delay also occurs. The worst case is now that the two signals (original one → red and reflected one → gray) on layer 2 have a phase shift of 180°, and so they cancel each other. The phase shift is due to the delay which arises from the stub length. The time delay is twice the stub length divided by the signal speed. To avoid this problem, use blind vias or buried vias.

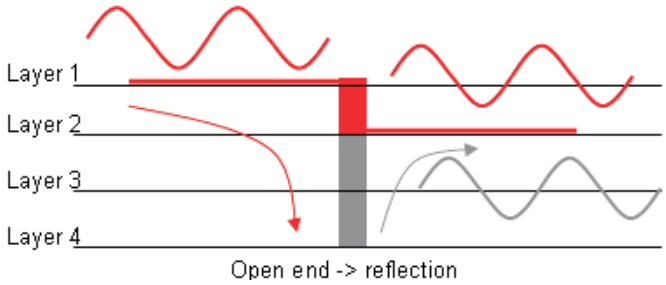

Figure 16. Reflection Caused by Stubs in a Via

Tips for routing traces and the use of vias:

- Do not use right-angle bends on traces with controlled impedance and fast rise time, respectively.
- Route the traces orthogonally to each other on adjacent layers to avoid coupling.
- To minimize crosstalk, the distance between two traces should be approximately 2 to 3 times the width of the trace.
- Differential traces should be routed as close as possible to get a high coupling factor. As a result of this, influenced noise is then a common-mode noise and is not a problem for a differential input stage.
- Do not use vias on traces with sensitive signals, if unnecessary.
- Be careful with the return current when changing the layers. Use ground vias around the signal via to make sure that the return current can flow as close as possible to the signal (Figure 14).
- Do not create slots, for example in the ground plane, by using closely placed vias (Figure 15).
- Consider stubs created by vias. If necessary, use blind vias or buried vias (Figure 16).

2.6 Clock Distribution

Figure 17 shows four possible clock distribution circuits. The problems in Figure 17a are the enormous reflections at the branches and the different trace length to the devices. Because of the delay, it is possible that the system cannot function properly. To avoid the reflection at the branches, do not use them (Figure 17b). Route the signal in a chain from one device to the other and realize a proper termination. Be careful with the delay. In a high-speed environment, it is possible that the data, sent from device A to device B, is out of date when the clock signal arrives at device B. A star connection as shown in Figure 17c is a good solution to minimize the delay. A clock driver is used to distribute the clock signals to the different devices. To minimize the skew, the same trace length for every clock signal should be used. Figure 17d illustrates a solution for a complex system. A main clock feeds several clock drivers. Again, to reach low skew, implement delay-time compensation and use a proper termination to avoid reflections.

- Be careful with trace length in a clock distribution layout. Consider the delay for each trace. The best solution is to route these signals with the same length.
- Avoid branches to reduce reflections. Use a clock driver to distribute the signal to every device and consider a proper termination.

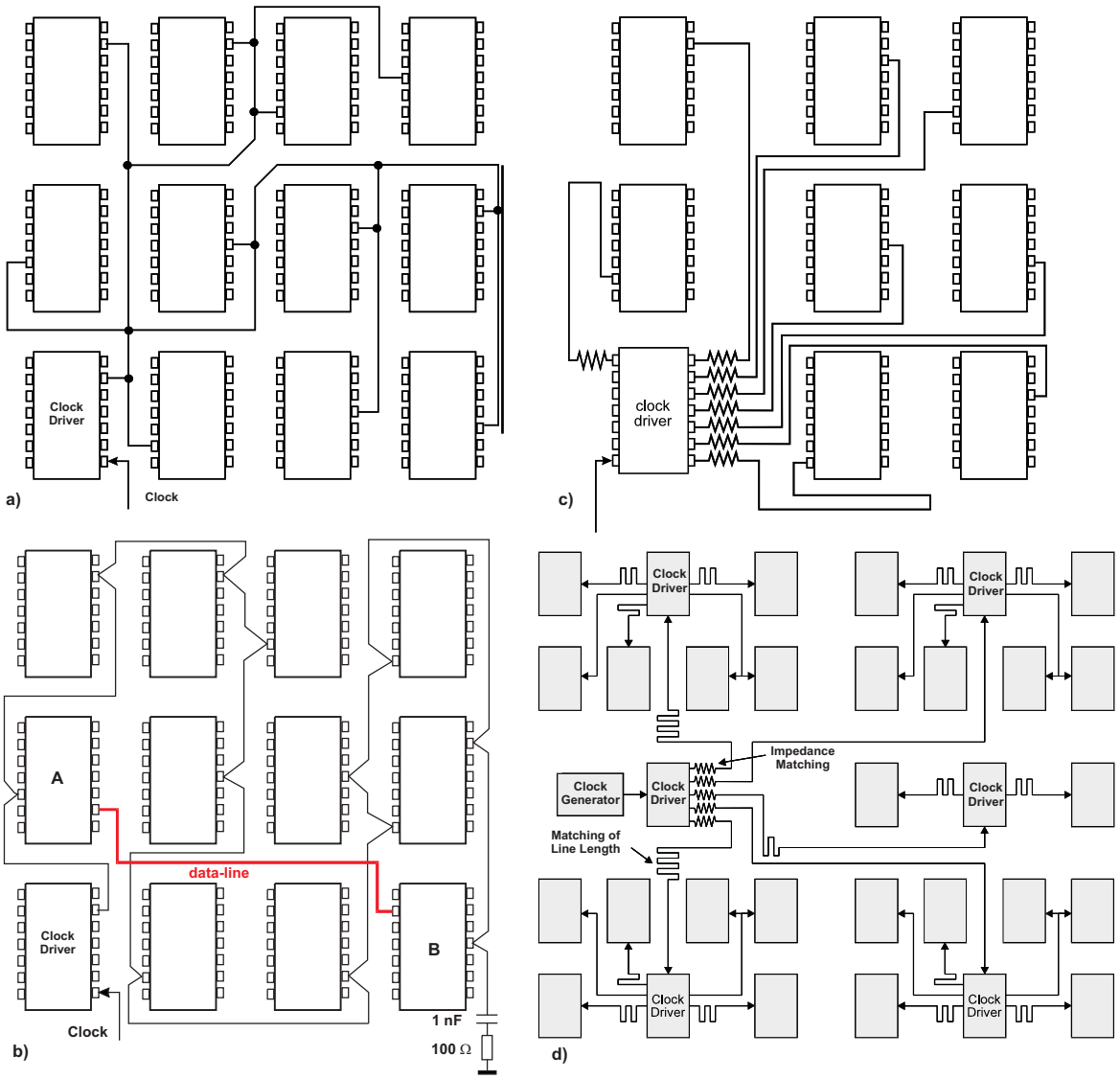

Figure 17. Poor and Good Clock Distribution on a PCB

3 Summary

This document presents an introduction to designing a PCB, a complex topic. However, the rules presented in this introduction can assist the designer in creating proper PCB designs. The higher the signal frequency with which the designer must contend, the more complicated will be the PCB design. Complicated PCB designs require a deep knowledge, experience, and simulation tools. However, it is not always necessary to route traces as short as possible, differential signals as close as possible, or to avoid crosstalk as much as possible. Rather, it depends on the signal on the trace. Basically, the designer must know which are the sensitive parts in the circuit or where problems due to reflections can occur. With this knowledge, a good placement of the devices can be made. Because placement is such an important step in high-speed design, the designer will do well to always keep it and the return current in mind.

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