



APPLICATION NOTE 3702

MAX2235—Layout Optimization Techniques

Abstract: The MAX2235 is a three-stage power amplifier that operates in the 800MHz to 1000MHz range and has been shown to produce up to 30dBm in GSM and ISM applications. Achieving maximum performance is not a trivial matter, and the best starting point is a good PC board layout. This article reviews proven layout practices and helps the reader understand both the nature of the PA and rationale behind the proposed techniques.

General

The MAX2235 is a three-stage power amplifier that operates from 800MHz to 1GHz and produces up to 30dBm of output power in GSM and ISM applications. Achieving this type of performance is not a trivial matter, and the best starting point is a good PC board layout. Conversely, and more importantly, a poorly designed PC board layout will absolutely preclude achieving optimum performance.

This article will review proven layout practices and help the reader understand both the nature of this IC and rationale behind the proposed techniques. Used as a guideline for new layouts, it will help anyone designing with the MAX2235 avoid common pitfalls and get the most out of their design.

Supply Bypassing and the Interstage Match

Perhaps one of the least understood and most important aspects of this IC is the interstage match. Because the amplifier is actually comprised of three separate stages, and each stage has slightly different impedance characteristics, they must be matched to each other to provide maximum power transfer.

The V_{CC} pins 3, 5, 8, and 9 on the device are not purely supply inputs in need of bypassing. The lumped element capacitance (and parasitics) applied to these pins interact with the device internally and provide some measure of interstage matching. This allows the designer to customize the match for their particular application.

In order to capitalize on the flexibility of this design, the bypass capacitor positions should be somewhat adjustable along the V_{CC} trace, with the cap between the V_{CC} via and the device pin. The optimum amount of trace length between the interstage cap and the IC pin can be established empirically for a desired operating frequency by sliding the cap along the V_{CC} trace (see **Figure 1**). Use of high-Q capacitors at these locations generally provides the best match, and 0402 size components make the physical process of tuning manageable (as opposed to 0603s that leave little room for adjustment, and 0201s that may be more difficult to physically manipulate). The Murata GJM1555 series (previously GJ615) has been used in this application with good results. They have a Q factor of greater than 100 at 900MHz.

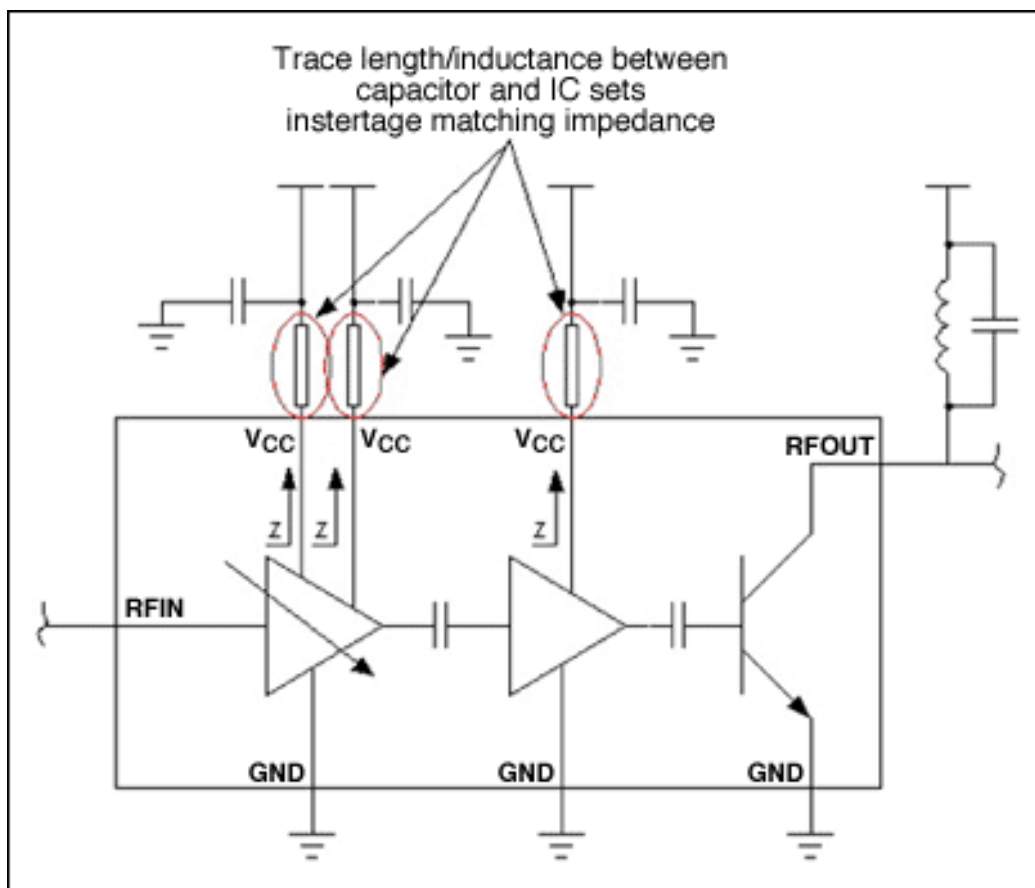


Figure 1. Adjustable bypass capacitor positions along the V_{CC} trace.

Given that the supply pins of the PA are acting as the interstage match, it is important to isolate the lines from each other as much as possible. (Note: The term "isolate" is used here in a purely RF sense. Of course, the lines are DC-coupled.) If this is not accomplished, RF energy may couple from one stage to another in a way that is detrimental to performance. Using a "star topology" is a way to effectively isolate the supply lines for each stage. In this configuration, each supply line originates from a single point where it is bypassed with a large capacitor. The lines are then run on the bottom layer of the PC board and are physically separated from each other as much as reasonably possible. Coupling between V_{CC} lines is reduced on the bottom layer because the lines are separated by a ground plane, as opposed to the dielectric of an inner layer. Each separate line is bypassed locally by the interstage matching cap, which simultaneously matches the interstage node. Placing the caps on the top side is preferable, as this allows for very close positioning and maximal control of the match. **Figure 2** shows recommended placement and orientation of these components.

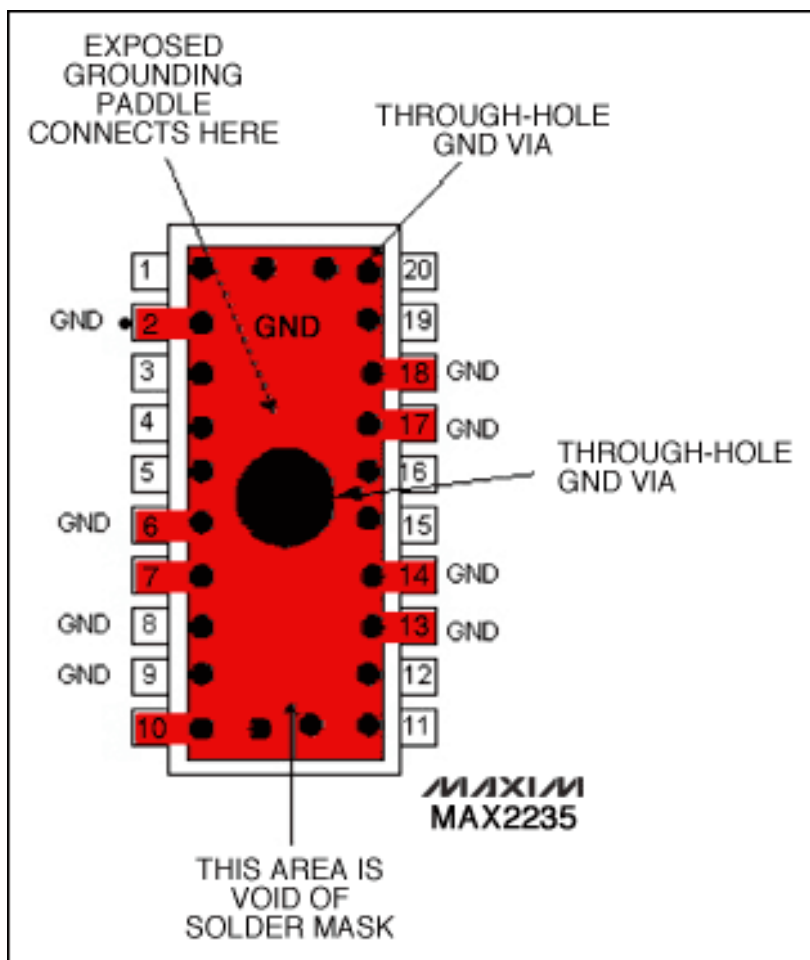


Figure 3. Exposed paddle must be connected to ground.

Output Network

The current evaluation kit can be misleading in this area. It was designed for a very specific performance band and, while functional, should not necessarily be copied for other applications. The EV kit uses a 30AWG wire in parallel with a 0Ω resistor running from pin 16 to V_{CC} . Maxim does not currently recommend using the wire short and resistor pullup for the output on new designs. Instead, good performance has resulted from using an L||C combination pulled up to V_{CC} . If the parallel resonance of the LC is carefully chosen, it will look like high impedance at the frequency of interest (therefore not affect the match), but will help to greatly attenuate harmonics. On designs at 915MHz, the values of 10nH and 3.3pF have produced very good harmonic suppression and minimal disturbance of the output match.

When designing the output match, a similar method can be used to that of the interstage. Sliding the output shunt cap along the transmission line allows for precise adjustment of the impedance presented to the PA output. The EV kit demonstrates this method using a two-element match. For more adjustment capability, a four-element match (Series L, Shunt C, Series L, Shunt C) has been shown to work well (see **Figure 4**). Regardless of the method for impedance conversion, using a controlled impedance transmission line surrounded by numerous adjacent ground vias is recommended. This minimizes PC board loss and improves harmonic suppression by providing an unobstructed RF ground return path along the line. Also note that using high-Q components (>100 at the frequency of interest) in the match is vital to achieving the best performance in prototype and production. Again the Murata GJM1555 series (or equivalent) is recommended.

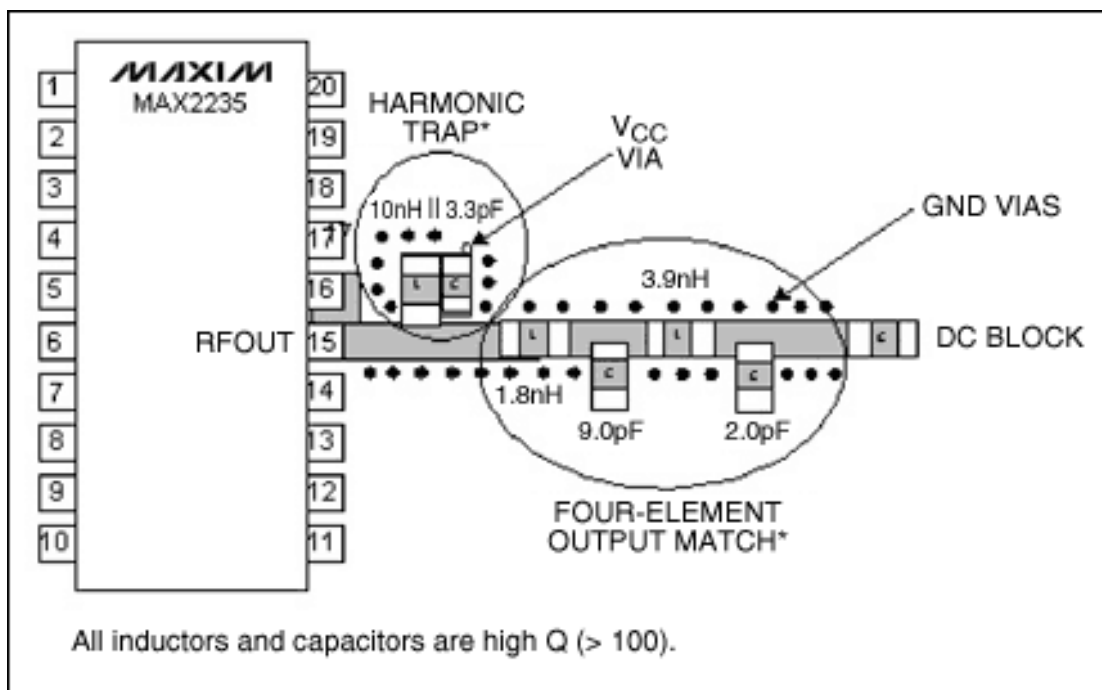


Figure 4. Four-element output match with high-Q inductors and capacitors.

Summary

As with all RF power amplifiers, achieving optimum performance with the MAX2235 depends on careful and deliberate decisions made during the PC board layout process. The following items should be thoroughly considered before a first prototype is built:

Interstage Match Place the V_{CC} bypass/interstage-matching caps as close as possible to the IC pins (3, 5, 8, and 9), and allow for positional adjustment during initial tuning. Use high-Q components for best results.

V_{CC} Routing Use a topology that allows for maximum distance between supply lines (and thus minimum coupling) for different PA stages. A "star topology" on the bottom layer of the PC board is very effective here. Bypass V_{CC} globally.

Grounding Provide the shortest, lowest inductance path to ground for the IC pins. Consider solder flow and manufacturing capability of exposed paddle on bottom of IC. This must be tied to the ground plane!

Output Match Use high-Q components and a four-element match, followed by controlled impedance transmission line. A harmonic trap can be implemented at the pullup inductor prior to the match without affecting impedance transformation.

Figure 5 illustrates the implementation of these key items, and **Figure 6** shows an actual example of a "star topology" on another Maxim EV kit.

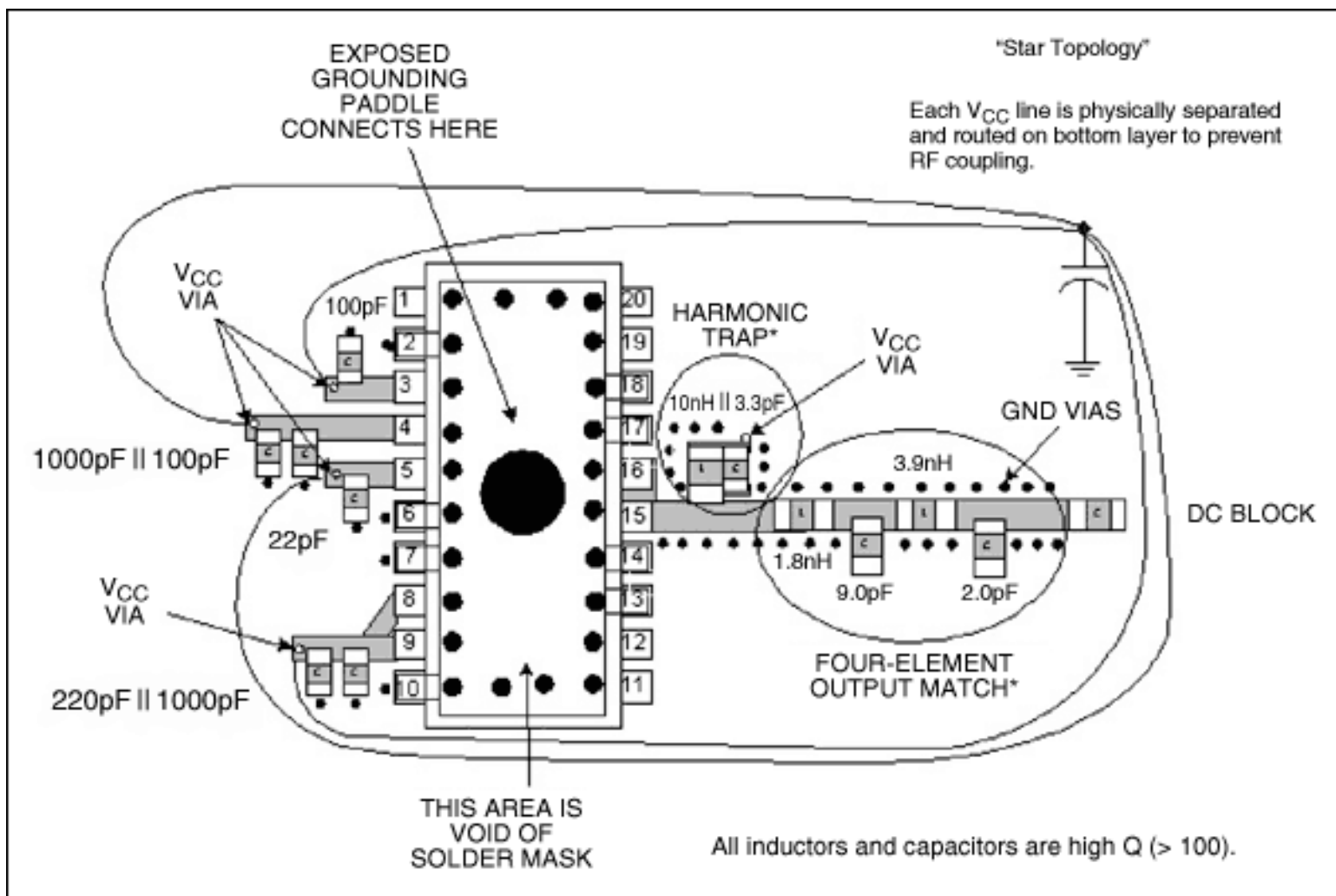


Figure 5. Implementation of key items to consider before first prototype is built.

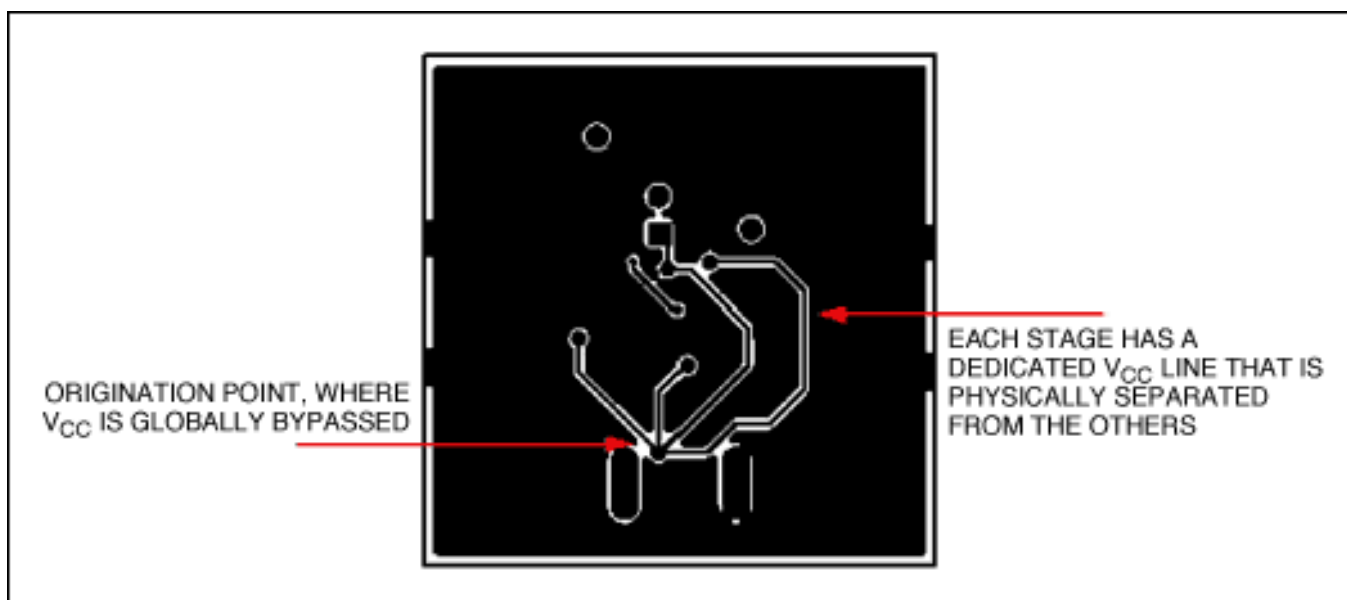


Figure 6. Example of a "Star Topology" on a Maxim EV Kit.

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