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SEMICONDUCTOR DEVICES, HIGH RELIABILITY, SPACE USE, GENERAL SPECIFICATION FOR

JAXA
JAPAN AEROSPACE EXPLORATION AGENCY

This specification was originally written and established in the Japanese language. This specification has been translated into English for international users. Note that this document is a working document for international users and is not subject to configuration control by JAXA. Any discrepancies found in this document should be verified against the latest Japanese document before any significant decisions are made.

Revision Record

Rev.	Date	Revised Contents
NC	31 Mar. 03	Original
A	31 Mar. 04	Revised with reorganization from NASDA to JAXA. - Renumbered the specification no. from “NASDA-QTS-2030” to “JAXA-QTS-2030”. - Reflected change of organization name to the text.
B	28 Dec. 06	Change with revision to JAXA-QTS-2000C. - Paragraph 1.4: Changed “NASDA*****” to “JAXA*****” in part number definition. Corrected clerical errors and matched terminology in the text. - Changed the part number descriptions from “NASDA” to “JAXA” in entire text. - Paragraph 2.2: Reflected number change of JAXA Parts Application Handbook from “NASDA-HDBK-4” to ”JERG-0-035”.

Contents

SEMICONDUCTOR DEVICES, HIGH RELIABILITY, SPACE USE, GENERAL SPECIFICATION FOR

1. GENERAL

1.1 Scope

This specification establishes the general requirements and quality assurance provisions for space use high reliability semiconductor devices (hereinafter referred to as "semiconductor devices") used for electronic equipment installed on spacecrafts. This specification complies with JAXA-QTS-2000 (Common Parts/Materials, Space Use, General Specification for) which was recently established to transition to the qualified manufacturing line system and replaces the following specifications.

NASDA-QTS-19500A	Discrete Semiconductor Device, Reliability Assured, Space Development Use, General Specification for

1.2 Terms and Definitions

The definitions for terms used herein are as shown in JAXA-QTS-2000, paragraph 6.3 of this specification and each appendix.

1.3 Classification

Semiconductor devices covered by this specification shall be classified by materials, construction, characteristics, and applications and named according to provisions of JEITA ED-4001.

1.4 Part Number

The part number shall consist of JAXA, radiation hardness, constituent, identification number and suffix letters as follows:

(Example)

JAXA(1) R – 2SC – 4307 – A

R	2SC	4307	A
Radiation hardness (paragraph 1.4.1)	Constituent (paragraph 1.4.2)	Identification number (paragraph 1.4.3)	Suffix letter (paragraph 1.4.4)

Note: (1) "JAXA" indicates the part is for space use and may be abbreviated “J”.

1.4.1 Radiation Hardness

The radiation hardness shall be identified by a single capital letter and indicates the radiation hardness assurance level.

Letter	Radiation hardness assurance level
M	30 Gy (Si) {$3x10^3$ rad (Si)}
D	100 Gy (Si) {$1x10^4$ rad (Si)}
P	300 Gy (Si) {$3x10^4$ rad (Si)}
R	1,000 Gy (Si) {$1x10^5$ rad (Si)}
F	3,000 Gy (Si) {$3x10^5$ rad (Si)}
H	10,000 Gy (Si) {$1x10^6$ rad (Si)}

Note: Values in parentheses { } are for reference only.

1.4.2 Constituent

The constituent shall be the combination of a one-digit number and a single or double capital letter(s), and assigned according to the types, polarity or application of the semiconductor devices as specified in JEITA ED-4001.

1.4.3 Identification Number

The identification number shall be consecutive numbers starting from 11 and assigned for each registration as specified in JEITA ED-4001.

1.4.4 Suffix Letter

Part changes shall be identified by a capital letter starting from A. ”R” shall be additionally used for reverse characteristics diodes or thyristors. The suffix letter shall be assigned as specified in JEITA ED-4001.

2. APPLICABLE DOCUMENTS

2.1 Applicable Documents

The documents listed below form a part of this specification to the extent specified herein. These documents are the latest issues available at the time of contract award or application. If it is necessary to designate an issue, the issue shall be specified in the detail specification.

a)	JAXA-QTS-2000	Common Parts/Materials, Space Use, General Specification for
b)	MIL-STD-750	Test Method Standard, Semiconductor Devices
c)	JIS B 0205	ISO General Purpose Metric Screw Threads Part1: Basic Profile to Part 4: Basic Dimensions
d)	JEITA ED-4001	Type Designation System for Discrete Semiconductor Devices
e)	ISO 14644-1:1999	Cleanrooms and Associated Controlled Environments --Part 1: Classification of Air Cleanliness
f)	ISO 14644-2:2000	Cleanrooms and Associated Controlled Environments -- Part 2: Specifications for Testing and Monitoring to Prove Continued Compliance with ISO 14644-1

2.2 Reference Documents

Following document is a reference document.

JERG-0-035 JAXA Parts Application Handbook

2.3 Order of Precedence

In the event of a conflict between the text of this specification and the applicable documents, the following order of precedence shall apply.

a) Detail specification
b) This specification
c) JAXA-QTS-2000
d) Applicable documents of this specification (paragraph 2.1, except for JAXA-QTS-2000)

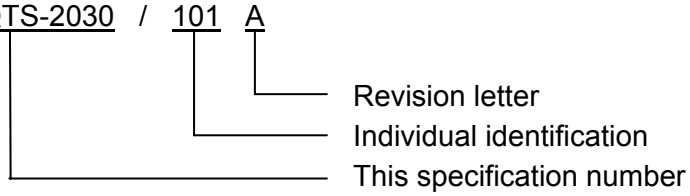
2.4 Detail Specification

Detailed requirements for the type and performance of the semiconductor devices are specified in each detail specification.
The detail specification shall be prepared and established by the manufacturer in accordance with Section A.4, Appendix A of JAXA-QTS-2000, and shall be registered with the Japan Aerospace Exploration Agency (hereinafter referred to as “JAXA”).

2.4.1 Detail Specification Number

The detail specification number shall be indicated in the following form in accordance with paragraph A.2.2.2, Appendix A of JAXA-QTS-2000.

Example: JAXA-QTS-2030 / 101 A



2.4.2 Revision Letter of Detail Specification

A revision letter in the detail specification number shall be assigned in accordance with paragraph A.2.2.2.4, Appendix A of JAXA-QTS-2000.

2.4.3 Independency of Detail Specification

The detail specification shall be a stand-alone document with a unique number defined in accordance with paragraph 2.4.1.

2.4.4 Format of Detail Specification

The detail specification format shall be in accordance with Appendix F of this specification.

3. REQUIREMENTS

3.1 Certification

3.1.1 Qualification Coverage

Qualification shall be valid for semiconductor devices that are produced by the manufacturing line that conforms to design, construction, and materials specified in paragraph 3.3 and the quality assurance program. The qualification coverage shall be limited to the range of construction and designing limit values typified by evaluation

devices or samples which have passed the qualification test. Within this coverage, the manufacture is allowed to supply qualified products in compliance with the detail specification.

3.1.2 Initial Qualification

To acquire certification of the semiconductor devices in compliance with this specification, a manufacturer shall establish a quality assurance program in accordance with paragraph 3.2.1, perform the qualification tests specified in paragraph 4.6, and acquire a certification status from JAXA as specified in paragraph 3.4.1 of JAXA-QTS-2000. The manufacturer shall be listed on the Qualified Manufacturers List of the Japan Aerospace Exploration Agency (JAXA QML).
The manufacturer shall prepare design documents of the semiconductor devices to be qualified in accordance with Appendix E and submit them with Quality Assurance Program Plan at the time of application for qualification test.

3.1.3 Retention of Qualification

To continue supplying semiconductor devices in accordance with this specification, a manufacturer must apply for QML certification retention in accordance with paragraph 3.4.2.1 of JAXA-QTS-2000 commencing between 30 and 60 days prior to the expiration date of the certification period (paragraph 3.1.4).
If products were not shipped during the effective period of certification and a quality conformance inspection was not conducted, the manufacturer may apply for retention of certification without conducting the quality conformance inspection.

3.1.4 Effective Period of Certification

The effective period of certification granted in compliance with this specification shall be three years.

3.1.5 Change of Qualification Coverage

To change the qualification coverage, the manufacturer shall perform procedures for re-qualification in accordance with paragraph 3.4.3 of JAXA-QTS-2000.

3.2 Quality Assurance Program

3.2.1 Establishment of a Quality Assurance Program

To acquire certification in compliance with this specification, the manufacturer shall be responsible for establishing a quality assurance program that meets the requirements specified in paragraph 3.3.1 of JAXA-QTS-2000 and this specification. The manufacturer shall generate a Quality Assurance Program Plan in accordance with paragraph 3.3.2 of JAXA-QTS-2000 and provide the plan to JAXA for review in accordance with paragraph 3.3.6 of JAXA-QTS-2000.

3.2.2 TRB Formation

To acquire a certification status in compliance with this specification, the manufacturer shall form and operate the Technology Review Board (TRB) in accordance with paragraph 3.3.5 of JAXA-QTS-2000.

3.3 Design and Construction

3.3.1 Operating Temperature

Unless otherwise specified in the detail specification, the minimum and maximum operating temperatures of the semiconductor devices shall be -55ºC and +200ºC, respectively.

3.3.2 Metallization

Unless otherwise specified in the detail specification, the metallization thickness shall be 0.80µm or more. The maximum allowable current densities shall not exceed the values specified below at any point of the metallized surface including the thinnest areas such as levels of the substrate.

Unit: A/cm^2

Metallization material	Maximum allowable current density
Aluminum (99.99% pure or doped, without glassivation)	$2x10^5$
Aluminum (99.99% pure or doped, with glassivation)	$5x10^5$
Gold	$6x10^5$
All Others	$2x10^5$ (Unless otherwise specified in the detail specification)

Maximum current densities shall be calculated using current and cross section areas which are determined as follows.

a) The current shall be the maximum continuous current at the maximum load or equal to the simple time-averaged current obtained at the maximum rated frequency or duty cycle with the maximum load, whichever results in the greater current value. Currents shall be calculated on the assumption that currents flow uniformly through the conductor's cross section driven by the maximum recommended operating voltage.

b) The metallization thickness shall be the minimum allowed metallization thickness defined in the manufacturing specifications.

c) The metallization width shall be an actual minimum design value (not mask widths) which is calculated in consideration of thinning and undercutting of the metal which is expected to occur during the etching process.

d) Areas of barrier metals and nonconductive materials shall not be added to the cross section.

e) To compensate for reduction of the cross section due to thinning, voids and scratches, the cross section shall be obtained from steps b) through d) and multiplied by 0.75.

3.3.3 Glassivation

Unless otherwise specified in the detail specification, silicon transistors shall be glassivated. The glassivation thickness shall be 0.40μm or more for SiO_2 and 0.20μm or more for Si_3N_4. The glassivation shall cover all conductor surfaces except for bonding pads.
The spacing between all conductors that are not glassivated (e.g., spacing between bonding pads, bonding pads and scribed region) shall be 50μm or more.

3.3.4 Thickness of Die

Unless otherwise specified in the detail specification, thickness of dies shall be 150μm or more.

3.3.5 Die Mounting and Plating

Glass shall not be used for die mounting. When the bottom surface of the die is gold plated, the plating thickness shall be between 0.10μm and 1.00μm.

3.3.6 Internal Lead Wire and Bonding Method

a) Internal lead wires
Unless otherwise specified in the detail specification, the diameter of internal lead wires shall be 25μm as a minimum. For leads with a non-circular cross section, use a circular wire diameter which has the same cross section area. The material of the lead wires shall be the same metal used for the die metallization.

b) Bonding method
All diodes, except the schottky barrier and point contact UHF diodes, shall be connected using metallurgical bonding (item v), paragraph 6.3).

c) Maximum allowable current
Internal lead wires or other conductors which are in thermal contact with the die along their entire length shall be designed such that the maximum rated current (continuous current for DC, effective current for AC and peak current multiplied by $1/\sqrt{2}$ for pulsed current) shall not exceed the maximum allowable current calculated by the following formula.

$$I = \frac{1}{128} \times K \times d^{\frac{3}{2}}$$

Where:
I = Maximum allowable current
d = Wire/conductor diameter
(When the cross section is not circular, the diameter of a circular wire or conductor of the same cross section area)
K = A constant obtained from the length and composition of the wire or conductor as shown in Table 1.

Table 1. Material and K Value

Material	"K" value for bond-to-bond total conductor length	
	Length ≤ 1.0mm	Length > 1.0mm
Aluminum	22,000	15,200
Gold	30,000	20,500
Copper	30,000	20,500
Silver	15,000	10,500
Others	9,000	6,300

3.3.7 Package

a) General

The semiconductor device shall be hermetically sealed in a package made of glass, metal, ceramic or a combination of these materials.

No organic or polymer materials (e.g., lacquers, varnishes, coatings, adhesives, greases, etc.) or desiccants shall be used in the package.

b) Package material

External metal surfaces of the package shall be corrosion resistant. Nonmetallic materials of the package and coatings including markings shall be non-nutrient to fungus and shall not display blister, crack, outgas, softening, outflow or other defects under the specified test conditions.

c) External lead material and finish

1) External lead material

Unless otherwise specified in the detail specification, the external lead material composition shall meet one of the following material composition types.

1.1) Type A

Iron	53% nominal
Nickel	29±1%
Cobalt	17±1%
Manganese	0.65% max.
Carbon	0.06% max.
Silicon	0.20% max.
Aluminum	0.10% max.
Magnesium	0.10% max.
Zirconium	0.10% max.
Titanium	0.10% max.

(The summation of aluminum, magnesium, zirconium, and titanium contents shall not exceed 0.20%.)

1.2) Type B

Nickel	40 to 43%
Manganese	0.80% max.
Silicon	0.30% max.
Carbon	0.10% max.
Chrome	0.25% max.
Cobalt	0.50% max.
Phosphorus	0.025% max.
Sulfur	0.025% max.
Aluminum	0.10% max.
Iron	Remainder

1.3) Type C

Nickel	41 to 43%
Manganese	0.75 to 1.25% max.
Silicon	0.30% max.
Carbon	0.10% max.
Sulfur	0.02% max.
Phosphorus	0.02% max.
Iron	Remainder

2) External lead finish

Unless otherwise specified in the detail specification, the external lead finish shall be one of the following options.

2.1) Solder dip

The solder dip shall be homogeneous with the minimum thickness at the major flats of 5.08μm solder (Sn60 to Sn63) over a primary finish in accordance with type 2.2) or 2.3) below, or nickel plating of a thickness between 2.54 and 7.62μm.

2.2) Acid tin plating

Acid tin plating thickness shall be between 2.54μm and 12.7μm. Nickel or copper under-plating (electroless or electrolysis) may be used. In this case, the under-plating shall be between 0.25μm and 7.62μm.

Remark: It is known that there are different tin platings with different compositions and reflectances. However, the acid tin plating specified herein shall be uniform and dense, and satisfy all the requirements specified herein.

2.3) Gold plating

The purity of gold shall be a minimum of 99.7% (i.e., a total of impurities and other metals shall not exceed 0.3%). The thickness of the plating shall be a minimum of 1.27μm. This finish requires electrolysis nickel or copper undercoating with a thickness between 1.27μm and 7.62μm.

3.3.8 Screw Threads

If screw threads are specified as one of the mechanical requirements, the screw threads shall meet standard screw threads specified in JIS B 0205-1 to JIS B 0205-4.

3.4 Marking

3.4.1 Marking Items

Unless otherwise specified in the detail specification, the following marking items shall be placed on each product.

a) Index and polarity (paragraph 3.4.1.1)
b) Part number (paragraph 3.4.1.2)
c) Inspection lot identification code (paragraph 3.4.1.3)
d) Serial number (paragraph 3.4.1.4)
e) Manufacturer's identification (paragraph 3.4.1.5)

If there is insufficient surface area for the required markings, marking items may be omitted in the following order of priority.

a) "JAXA" or "J" of part number
b) "Constituent" of part number. Last capital letter must be marked.
c) Serial number. In this case, attach a tag to the lead or body of the product.

3.4.1.1 Index and Polarity Marking

The index and polarity marking shall meet the following requirements. The manufacturer's identification shall not be used for this purpose. These items shall be visible from the top when the product is mounted in a normal manner.

a) Index
The index indicates the start of lead numbers or mechanical orientation and shall be shown by a stamp, tab, notch or groove, among other means.

b) Polarity of diodes
The polarity of diodes shall be marked in one of the following ways.
1) A diode symbol or arrow pointing toward the cathode terminal in forward bias.
2) A noticeable color band or a dot close to the cathode terminal in forward bias.

c) Polarity of thyristor
A graphic symbol of the thyristor with an arrow indicating the direction of cathode terminal.

3.4.1.2 Part Number

The part number shall be as specified in paragraph 1.4.

3.4.1.3 Inspection Lot Identification Code

An inspection lot identification code shall be assigned to each inspection lot (item p) of paragraph 4.3.1).

3.4.1.4 Serial Number

A serial number shall be assigned to each semiconductor device in the inspection lot prior to the radiographic inspection in the screening test (paragraph 4.7).

3.4.1.5 Manufacturer's Identification

The manufacturer's identification identifies the certified manufacturer. Manufacturer's name, abbreviated name, trademark or any combination of them shall be marked.

3.4.2 Marking Location and Layout

Unless otherwise specified in the detail specification, markings including the part number, inspection lot identification code, and serial number shall be placed on the surface which is visible when the product is mounted in a normal manner. The marking items may be placed in any layout as long as they function properly and do not interfere with any other markings.

3.4.3 Marking Option

The manufacturer shall complete marking on all products in the inspection lot by the end of the screening test or shall mark on only the samples used for Groups B, C, D and E tests of the qualification test or quality conformance inspection. When the manufacturer chooses the latter, the procedure shall be as follows.

a) Samples shall be marked prior to the Groups B, C, D, and E tests of the qualification test or quality conformance inspection.
b) Confirm that all markings meet all requirements upon completion of the test.
c) Mark on the products in the same inspection lot as samples and perform the external visual inspection as part of the screening test. The marking materials and processes shall be the same as those applied to the samples.

4. QUALITY ASSURANCE PROVISIONS

4.1 General Requirements

The manufacturer shall be responsible for implementing the quality assurance program specified in paragraph 3.2 of this specification and operating the TRB.

4.2 Incoming Material Control

Incoming materials shall be subjected to an appropriate receiving inspection and controlled to ensure that each material is traceable to the receiving inspection lot. The manufacturer shall establish and implement procedures to store and distribute incoming materials and to remove life limited materials.

4.2.1 Receiving Inspection

Receiving inspection for each incoming materials shall include at least the following items shown in Table 2.

Table 2. Materials and Items for Receiving Inspection

Material	Receiving inspection item
Substrates	Thickness, flatness, parallelism, dislocation density, plane direction, specific resistance, and visual inspection
Wire	Composition, uniformity, hardness, diameter, elongation, tensile strength, purity, and cleanliness
Packaging and lead materials	Dimensions, composition, strength, purity, and plating
Other metals	Composition and purity
Chemicals and gasses	Composition, purity, and grade
Masks	Configuration (width and length), pinholes (density, size, and distribution), scratches, and roughness of edges

4.2.2 Records of Incoming Material Control

The records of incoming materials shall be classified into a) Incoming inspection records and b) storage, distribution and disposal records.

a) Incoming inspection records
   1) Material name
   2) Inspection items
   3) Lot size
   4) Lot identification code
   5) Document number and established date of inspection instructions
   6) Pass/fail of each lot and quantity of failed materials
   7) Date of inspection and name or identification code of the inspector

b) Storage, distribution and disposal records
   1) Material name
   2) Storage conditions
   3) Lot identification code
   4) Storage date and quantity of storage materials
   5) Distribution date, quantity, and lot identification code of finished/semi-finished products for which the material is used.
   6) Disposal date

4.3 Manufacturing Process Control

The manufacturer shall establish and maintain procedures, control parameters, and control methods of manufacturing processes.

4.3.1 Task Control of Manufacturing Process

The manufacturer shall define and control each manufacturing process including at a minimum the items listed below. Rework shall be performed in accordance with paragraph 4.3.2. The manufacturer shall also establish and implement a storage method for finished or semi-finished products between processes. Following die

mounting process (item k)), the manufacturer shall perform additional sampling visual inspection in 100% visual inspection process.

a) Wafer lot formation
   1) Formation procedure for wafer lots
   2) Assignment method of wafer lot identification codes

b) Oxidation process
   1) Oxide layer materials
   2) Forming method
   3) Control methods of oxide layer thickness, and pinhole/crack dimensions and density
   4) Furnace control method

c) Pattern formation process
   1) Forming method
   2) Etching method
   3) Visual inspection method

d) Epitaxial growth process
   1) Materials
   2) Forming method
   3) Pretreatment procedure of wafer
   4) Conditions
   5) Methods of inserting and extracting wafer
   6) Control methods of epitaxial layer thickness, sheet resistance and number of stacking faults
   7) Cleaning methods and frequency for susceptors and tubes

e) Junction formation process
   1) Dope source
   2) Forming method
   3) Control method of diffusion depth

f) Metallization formation process
   1) Metallization materials
   2) Forming method
   3) Forming conditions
   4) Sinter conditions
   5) Inspection method specified in Appendix A
   6) Cleaning method and frequency for chamber

g) Glassivation formation process
   1) Forming material
   2) Forming method
   3) Conditions
   4) Control method of dope concentration
   5) Inspection method specified in Appendix A

h) Back surface polishing process
   1) Materials
   2) Polishing methods
   3) Polishing conditions
   4) Protection method of front surface
   5) Removing and cleaning method of protective coating

6) Control method of parallelism
7) Inspection method specified in Appendix A

i) Scribing and dicing process
1) Scribing method
2) Dicing method
3) Method of100% visual inspection:
The criteria of 100% visual inspection shall be as specified in the test methods 2069, 2070, 2072 and 2073 of MIL-STD-750.

j) Formation of production lots
1) Formation method of production lots(1)
2) Assignment method of production lot identification code

Note: (1) It is desirable that the production lot is prepared such that inspection sublots can be easily organized (item o) of paragraph 4.3.1).

k) Die mounting process
1) Materials of mounting and mounting area of package
2) Mounting structure
3) Conditions
4) Method of 100% visual inspection:
The criteria of 100% visual inspection shall be as specified in test methods 2069, 2070, 2072 and 2073 of MIL-STD-750.
5) Control method of adhesive strength

l) Interconnect bonding process
1) Materials
2) Lead type
3) Bonding method
4) Bonding conditions
5) Method of 100% visual inspection:
The criteria of 100% visual inspection shall be as specified in test methods 2069, 2070, 2072 and 2073 of MIL-STD-750. This inspection may be included in item m) below.
6) Control method of bond strength

m) Pre-cap visual inspection process
The procedure and criteria of the visual inspection shall be as specified in test methods 2069, 2070, 2072 and 2073 of MIL-STD-750.

n) Sealing process
1) Package and sealing materials
2) Sealing method
3) Pre-sealing stabilization bake
4) Sealing conditions

o) Formation of inspection sublots
1) Formation method of inspection sublots(1)
2) Assignment method of inspection sublot identification code

Note: (1) Inspection sublots shall meet the following requirements.

i) An inspection sublot shall consist of semiconductor devices with identical die design, package type and lead finish.

ii) An inspection sublot shall be manufactured using dies from a single wafer lot.
iii) Semiconductor chips shall be made on a die produced from a single wafer lot.
iv) Each assembly process shall be completed using the same machines during a single shift. The die mounting and lead bonding shall be performed during 2 and 4 shifts, respectively.
v) All assembly operations from die mounting through package sealing shall be completed within the same 6-week period.
vi) Each inspection lot shall consist of 1,000 semiconductor devices maximum.

p) Formation of inspection lots
1) Formation method of inspection lots(1)
2) Assignment method of inspection lot identification code

Note: (1) Inspection lots shall meet the following requirements.

i) An inspection lot shall consist of semiconductor devices with identical die design, package type and lead finish.
ii) An inspection lot shall consist of five sublots as a maximum.
iii) All assembly operations from die mounting through package sealing shall be completed within the same 8-week period.

4.3.2 Rework Control

Rework shall be documented in work records for the production process in accordance with paragraph 4.3.5. Reworked products shall be clearly distinguished from other products. Reworks on the metallization, oxidizing, glassivation, and all assembly processes prior to sealing processes shall not be performed. Once sealed, rework shall be limited to re-cleaning, correction of defective marking, and lead straightening (e.g., reshaping of lead tips which does not affect hermeticity of the product).

4.3.3 Environmental Control

Temperature, relative humidity, and air cleanliness shall be controlled for manufacturing processes such as wafer manufacturing and assembly operations which are significantly affected by the environment. The air cleanliness shall be measured in accordance with ISO 14644-1 and 14644-2.

4.3.4 Water Purity

The purity of water shall be controlled with respect to the minimum specific resistivity, maximum total solids, maximum organic impurity, maximum bacteria concentration and maximum chlorine contents at room temperature.

4.3.5 Production Records

Production records shall be categorized as either a) work records for the production process or b) control records such as for environmental conditions. Production records shall be managed in accordance with the quality assurance program specified in paragraph 3.2.1 and include at least the following items.

a) Work records for the production process
   1) Name of work
   2) Lot identification code of materials and products (including semi-finished products)
   3) Document number and established date of work instructions
   4) Quantity of incoming and outgoing products (including semi-finished products) for each work and their disposition
   5) Date of work and name or identification code of operator
   6) Identification of equipment used

b) Control records such as for environmental conditions
   1) Document number and established date of control instruction
   2) Date of measurement and name or identification code of operator

4.4 Classification of Inspections and Tests

Inspections and tests shall include screening in addition to three categories specified in paragraph 4.3 of JAXA-QTS-2000.

a) In-process inspection
b) Qualification test
c) Screening test
d) Quality conformance inspection

4.5 In-Process Inspection

The manufacturers shall perform the in-process inspections during the manufacturing process to detect any failure which could seriously affect the reliability and quality of the products, assure the workmanship, and characterize properties which cannot be measured from the finished products. The manufacturer shall perform wafer lot inspection specified in Appendix A and other in-process inspections such as those listed below. The manufacturing flow chart in the Quality Assurance Program Plan shall define the inspection process.

a) Internal visual inspection of semi-finished products (non-destructive, 100% or sampled inspection)
b) Physical and chemical inspection of semi-finished products (destructive or non-destructive, sampled inspection)
c) Characterization of semi-finished products (non-destructive, 100% or sampled inspection)

4.5.1 In-Process Inspection Records

The manufacturer shall control in-process inspection records in accordance with the quality assurance program specified in paragraph 3.2.1.

4.6 Qualification Test

The qualification test shall be performed on inspection lots which have passed screening test in accordance with Appendix C using the evaluation devices or samples produced using the same design, construction, materials and manufacturing line as those to be qualified.

4.6.1 Evaluation Devices or Samples

Evaluation devices or samples shall be produced using the manufacturing line that satisfies designs, constructions and materials requirements defined in the Quality Assurance Program Plan and shall have the ability of proving that the manufacturing line to be certified has an adequate capability with respect to the structure and design limits of the products.

4.7 Screening

To supply semiconductor devices in compliance with this specification, screening shall be conducted in accordance with Appendix B. Prior to screening, production lots (item j) of paragraph 4.3.1) shall be re-grouped into inspection lots (item o) of paragraph 4.3.1). Screenings may be performed anytime after the final sealing process has been completed. In addition, each product shall be marked with a unique serial number within the inspection lot prior to the radiograph inspection to provide traceability between each measurement and individual product.

4.8 Quality Conformance Inspection

The quality conformance inspection is defined as a lot assurance inspection for delivery. It shall be performed in accordance with Appendix C for inspection lots which passed the screening test. Only those semiconductor devices that passed the quality conformance inspection are considered in compliance with this specification and allowed to be delivered. Products selected as samples shall be handled as specified in paragraph C.3.5, Appendix C.

4.9 Long-Term Storage

4.9.1 Disposition of Lots Stored for a Long Term at the Manufacturer's Site

When products have been stored at the manufacturer's site for 24 months or longer after the quality conformance inspection, the manufacturer shall repeat the Group A quality conformance inspection and the 100% visual inspection prior to delivery. Only the products that have passed such tests can be shipped as products. If products fail in any subgroup inspection, 100% inspection shall be performed for items in that subgroup. Only the semiconductor devices that have passed the inspection can be shipped as products. Failed products shall be removed and shall not be delivered.
The date of re-inspection shall be marked on the package or storage box.

4.9.2 Storage by Purchasers

The conditions and period of storage by purchasers shall be specified in the detail specification, if necessary.

4.10 Change of Tests and Inspections

Any change in the in-process inspection, screening test or quality conformance inspection specified in this specification shall be made in accordance with paragraphs 4.4 and 6.1 of JAXA-QTS-2000.

5. PREPARATION FOR DELIVERY

Preparation for delivery shall be as follows and as specified in Section 5 of JAXA-QTS-2000.

5.1 Packaging

Prior to delivery, the products shall be packaged individually. The package shall hold the products securely and prevent direct impact on the products. The package shall protect the products from moisture and be free from any sharp edge or burr on the external surfaces. It is desirable that the package allows visual inspection. The packaging material shall not break, peel off, crumble, loosen, accumulate static electricity, or corrode. Tape or adhesives shall not be used to secure the products. Special care shall be given to the products which require protection against electrostatic discharge. Individual shipping packages shall be kept in a shipping container to protect the products from possible damage during shipment.

5.2 Marking on Package

Each shipping package shall have the markings as specified in items b) through e) of paragraph 3.4.1. However, when the markings on the products are clearly visible in a packaged configuration, those markings on the package may be omitted. For packages with anti-electrostatic measures, a marking item “ESD sensitive” shall be added. All markings shall be waterproof. When individual packages are kept in a shipping container, marking items on the individual packages shall be duplicated on the container except for marking item d). Quantity, contract (order) number, applicable specification number, date of packaging and inspection result shall be added as the marking items.

6. NOTES

6.1 Notes for Manufacturer

6.1.1 Preparation and Registration of Application Data Sheet

The manufacturer shall prepare the application data sheet in accordance with Appendix G of JAXA-QTS-2000 and register it with JAXA.

6.2 Notes for Acquisition Officers

6.2.1 Items to be Specified for Procurement

To purchase semiconductor devices manufactured in compliance with this specification, the purchaser shall provide the following information.

a) Part number
b) This specification number
c) Detail specification number
d) Indication of test data or source inspection results to be submitted for delivery
e) Others

Requirements other than those defined in this specification may be specified for special applications as item e). However, if the requirements conflict with the existing requirements in this specification, the purchaser shall not request the manufacturer to indicate that the semiconductor devices complies with this specification.

6.2.2 Review of Application Data Sheet

The application data sheet details additional product information necessary for parts selection and designing that is not contained in the detail specification such as the qualification test data. The acquisition officers are requested to carefully review the Application Data Sheet prior to acquisition.

6.3 Terms and Definitions

a) Absolute maximum rating
The values specified as "ratings", "maximum ratings", or "absolute maximum ratings" are based on the "absolute system." Unless a specific test method is required, the values shall not be exceeded under any operating or test conditions. Unless otherwise specified, the voltage, current and power ratings are determined based on continuous DC power conditions with unconstrained thermal radiation at an ambient temperature of +25ºC. For pulsed or similar operating conditions, the current, voltage, and power loss ratings are functions of time and duty cycle.

b) Breakdown voltage
The breakdown voltage is the maximum instantaneous voltage, including repetitive and non-repetitive transients, which can be applied across a junction in the reverse direction without limiting the current by an external means (circuit). Breakdown voltage is also an instantaneous voltage which occurs during a transition from a small-signal high impedance region to a small-signal low impedance region.

c) Constant current source
A constant current source is a current source that does not cause any measurement changes greater than the required measurement precisions when the generator impedance is halved.

d) Constant voltage source
A constant voltage source is a voltage source that does not cause any measurement changes greater than the required measurement precisions when the generator impedance is doubled.

e) Noise figure
The noise figure of a given frequency is a ratio of the total noise power per unit bandwidth (determined by the output frequency) at the output to the noise power of the frequency at the input.
The noise temperature at the input is 293°K at all frequencies.

f) Open circuit
An open circuit is a circuit that does not cause any measurement changes greater than the required measurement precisions when the terminating impedance is halved.

g) Pulse
A pulse is a flow of electrical energy of short duration. Figure 1 shows an illustrative explanation of the characteristics defined in items h) through m).

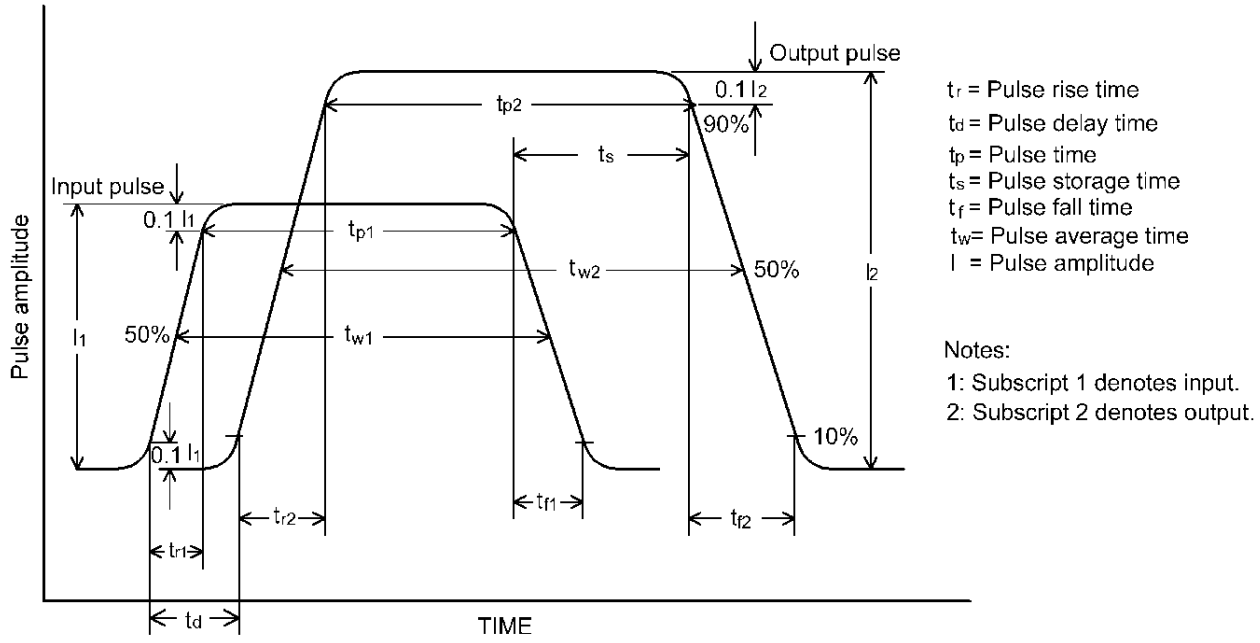


Figure 1. Pulse Measurements

h) Pulse average time
The average pulse time is the time from a point where the amplitude of the pulse has risen to 50% of the maximum amplitude to a point where the amplitude of the pulse has fallen to 50% of the maximum amplitude.

i) Pulse delay time
The delay time is the time from a point where the amplitude of the input pulse has risen to 10% of its maximum amplitude to a point where the amplitude of the output pulse has risen to 10% of its maximum amplitude.

j) Pulse fall time
The fall time is the time that the pulse amplitude takes to decrease from 90% to 10% of the maximum amplitude.

k) Pulse rise time
The rise time is the time that the pulse amplitude takes to increase from 10% to 90% of the maximum amplitude.

l) Pulse storage time
The storage time is a time from a point where the amplitude of the input pulse has decreased to 90% of its maximum amplitude to a point where the amplitude of the output pulse has decreased to 90% of its maximum amplitude.

m) Pulse time
The pulse time is the time between 90% of amplitude on the leading edge and 90% of amplitude of the trailing edge.

n) Short circuit
A short circuit is a circuit that does not cause any measurement changes greater than the required measurement precisions when the terminating impedance is doubled.

o) Small signal
A small signal is a signal that does not cause any measurement changes greater than the required measurement precisions when the signal amplitude is doubled.

p) Ambient temperature
Ambient temperature is the air temperature measured under a semiconductor device in an environment of sufficiently uniform temperature, cooled only by natural air convection and not practically affected by reflection or radiation.

q) Case temperature
Case temperature is the temperature measured at a specified point on the case of a product.

r) Storage temperature
Storage temperature is the temperature at which the semiconductor devices can be stored without any applied power.

s) Thermal equilibrium
Thermal equilibrium is a state that does not cause any measurement changes greater than the required measurement precisions when the test duration is doubled.

t) Thermal resistance
Thermal resistance is a temperature rise per unit power consumption at the junction with respect to an external temperature reference in thermal equilibrium.

u) Package type
A package type is characterized by the case outline, configuration, materials (including bonding wire, ribbon and die attach), piece parts (excluding preforms which differ only in size) and assembly processes.

v) Metallurgical bond
Metallurgical bond is a bond of constituent materials (metals or semiconductors) achieved by solidification of the constituent materials after re-growth and re-crystallization of the materials under a temperature and pressure where eutectic melt, normal melt, or solid diffusion of the materials occurs.

w) Production lot
A production lot is a group of semiconductor devices manufactured (or in the middle of the manufacturing process) on the same production line using the same manufacturing technology, materials, controls and design.

x) Inspection lot
An inspection lot is a group of semiconductor devices with the same die design, package type and lead finish. Inspection lots are usually divided into inspection sublots.

y) Inspection sublot
An inspection sublot is a group of products with the same die design, package type, and lead finish. Inspection sublots are processed together at all production processes.

z) Final seal
The final seal is a manufacturing process, after which access to internal elements of the product is not possible unless it is disassembled.

aa) Delta limits
A delta limit is the maximum allowable deviation of a parameter from an acceptance criteria of a given test.

Remark: Delta limit given as a percentage value means that the deviation of the parameter is calculated as a percentage of the post test measurement to the pre test measurement.

ab) Wafer lot
A wafer lot is a group of wafers formed together at each process.

ac) Percent Defective Allowable (PDA)
The PDA is allowable failure rate.

ad) Inspection
The inspection is a process to judge acceptance in a simple manner by comparison to specifications or limit samples.

ae) Test
A test is a process to obtain measurement data, judge acceptance, and evaluate workmanship of the product totally based on large or small, distribution, deviation of obtained data, and series of test data.