DVIO IP
User Guide

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Document version revision history

DATE	DOCUMENT VERSION	REVISION HISTORY	APPLICABLE IP AND CORRESPONDING VERSIONS
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IP Version change history

IP VERSION	RELEASE NOTES	RELEASE TIME
V1.0	1.DVIO IP initial version.	2023-02- 28

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Chapter 1 Preface

This chapter describes the scope of application, manual structure, and related writing conventions of this manual to help users quickly find the information they need.

1.1 About this manual

This manual is the user guide for the DVIO (Debugger Virtual Input/Output) IP product launched by Unisoc. The content mainly includes the IP usage guide and related appendices. Through this manual, users can quickly understand the related features and usage of DVIO IP.

1.2 Manual writing standards

Table 1-1 Writing specifications

WORD	USAGE PRINCIPLES
Notice	If the user neglects to pay attention to the content, there may be certain adverse consequences due to misoperation or the operation may not be successful.
Description	Instructions and tips provided to users.
Recommended	Recommended settings and usage instructions for users.

Chapter 2 IP usage guide

This chapter describes DVIO IP Related usage guides, including IP Introduction, IP Block diagram, IP Generation process, Example Design , IP interface description, IP register description, typical applications, instructions and precautions, and IP debugging methods. For more detailed information about the design process, please refer to the following PDS help document.

- Pango_Design_Suite_Quick_Start_Tutorial [1]
- Pango_Design_Suite_User_Guide [2]
- IP_Compiler_User_Guide[3]
- Simulation_User_Guide[4]

2.1 Introduction to IP

DVIO IP and DVIO_Jtag_Hub IP are IP developed by Shenzhen Unisoc Electronics Co., Ltd. for FPGA product debugging. They are applicable to all FPGA product series of Unisoc and can realize the driving and monitoring of FPGA internal signals. Users can use the company's PDS (The IPC (IP Compiler) tool in the Pango Design Suite completes the configuration and generation of IP modules.

The overall block diagram of DVIO IP and DVIO_Jtag_Hub IP is shown in Figure 2-1. DVIO_Jtag_Hub IP serves as the communication channel between the JTAG interface and user logic, parsing user operation instructions. DVIO IP consists of four modules: hub_decode, probe_in_inst, probe_out_inst, and tdo_mux.

- hub_decode: Receives the signal from the DVIO_Jtag_Hub module, decodes the signal to generate the chip select signal of the corresponding sub-module, and enables access to the current sub-module;
- probe_in_inst: Receive data from user logic and return the data to the software through the DVIO_Jtag_Hub module;
- probe_out_inst: DVIO output generation module, used to drive FPGA user logic devices;
- tdo_mux: used to select a tdo signal (INFO information, DVIO configuration information, DATA) to return to the software.

Description:

Used with the Fabric Debugger tool in the PDS suite, you can obtain a more intuitive presentation of debugging results..

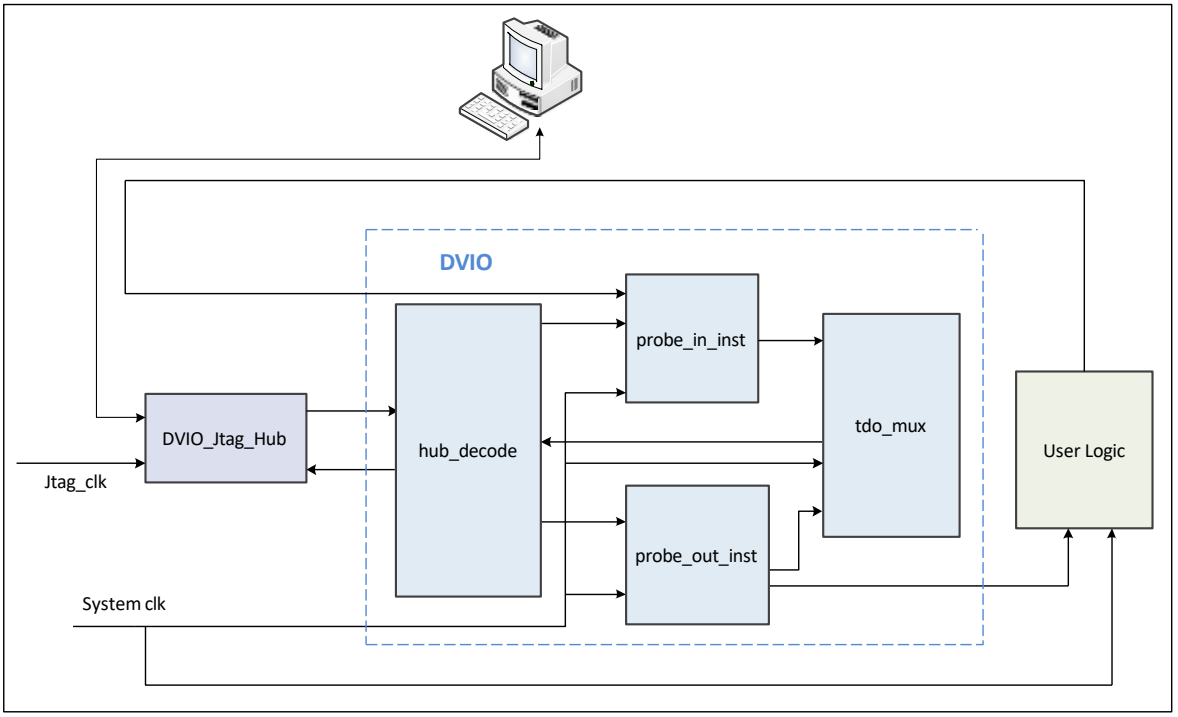

FIGURE 2-1 OVERALL STRUCTURE DIAGRAM

2.2 DVIO IP

2.2.1 Functional Overview

DVIO IP can be connected to the corresponding JTAG interface through DVIO_Jtag_Hub IP to realize user logic driving and monitoring. In the design, the user connects the signal to be debugged to the input/output port of the DVIO IP and debugs it with the PDS suite tool (Fabric Debugger).

The main features of DVIO IP are as follows:

- Support input/output port number configuration: 0~256;
- Support input/output port bit width configuration: 1~256 Bit;
- The input port supports Activity Detectors enabling configuration;
- The output port supports customized initialization configuration.

2.2.2 Interface Description

1. Interface diagram

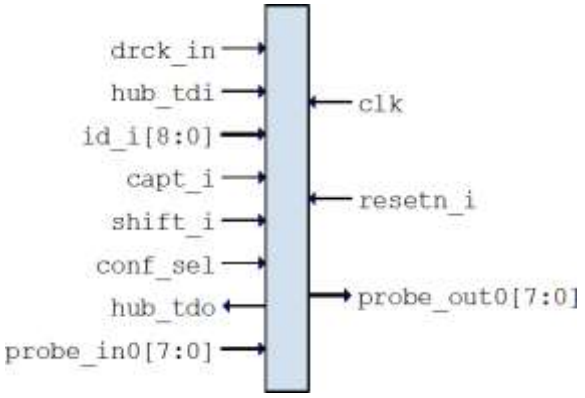

FIGURE 2-2 DVIO IP INTERFACE DIAGRAM

2. Interface list

Table 2-1 DVIO IP interface list

PORT	I/O	DESCRIPTION
drck_in	I	JTAG clock from DVIO_Jtag_Hub IP.
hub_tdi	I	tdi data from DVIO_Jtag_Hub IP.
id_i[8:0]	I	id selection signal from DVIO_Jtag_Hub IP.
shift_i	I	shift signal from DVIO_Jtag_Hub IP.
capt_i	I	capture signal from DVIO_Jtag_Hub IP.
conf_sel	I	Select enable signal from DVIO_Jtag_Hub IP.
hub_tdo	O	tdo data output to DVIO_Jtag_Hub IP.
resetn_i	I	Global reset signal, active low.
clk	I	User-supplied sampling clock signal.
probe_in<$N >[1]	I	Input port<$N>[1] signal input; The bit width is controlled by the Probe_in Ports page parameter Probe Width (1-256).
probe_out<$N >[2]	O	Output port<$N>[2] signal output; The bit width is controlled by the Probe_out_Ports page parameter Probe Width (1-256); The power-on initial value can be configured through the Initial Value parameter on this interface.

[1] <$N> value range: 0~255, corresponding to input ports probe_in0~probe_in255 respectively.
[2] <$N> value range: 0~255, corresponding to the output ports probe_out0~probe_out255 respectively.

2.2.3 Timing model

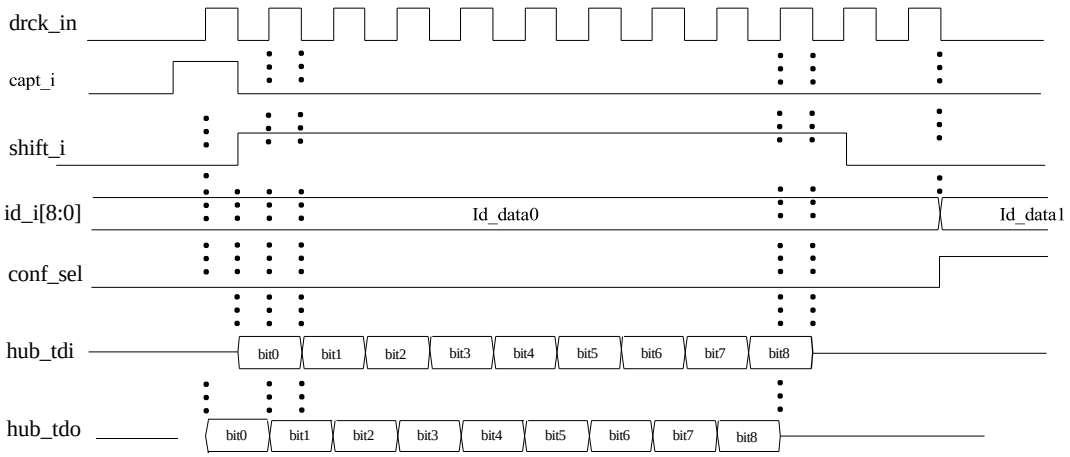

FIGURE 2-3 JTAG_HUB WITH DVIO INTERFACE TIMING

2.2.4 Module instantiation

Customized configuration of DVIO IP can be completed through the IPC tool, and the required IP modules can be instantiated and generated. For specific usage of IPC tools, please refer to IP_Compiler_User_Guide[3].

The main steps of instantiating the DVIO IP module are described below.

1. Select IP

Open the IPC software and enter the IP selection interface, as shown in Figure 2-4 below. Select the corresponding version of DVIO in the System/Tools/Debug directory, and then set the Pathname and Instance Name on the right page. The project instantiation interface is as shown in Figure 2-5.

Notice:

The software must be:

- 2022.2-SP2 SP and above Version;
- 2023.1 and above versions.

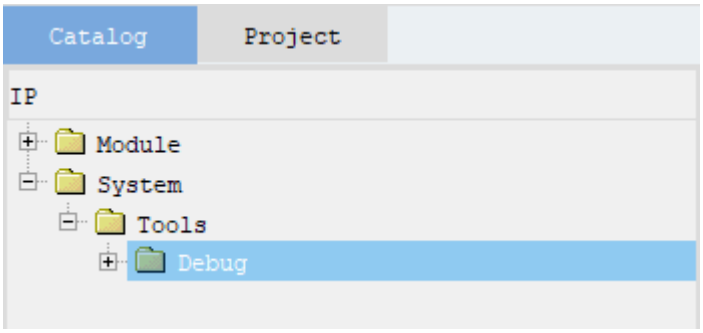

FIGURE 2-4 DVIO IP SELECT PATH

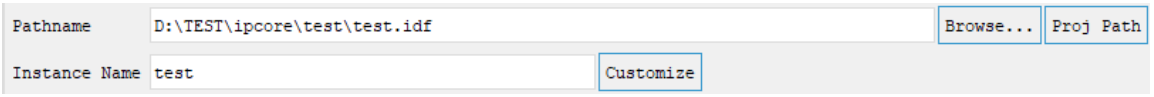

FIGURE 2-5 PROJECT INSTANTIATION INTERFACE

2. Configure IP parameter

After IP selection is completed, click <Customize> to enter the DVIO IP parameter configuration interface. The Symbol on the left is the interface block diagram, as shown in Figure 2-6; the right is the parameter configuration window, as shown in Figure 2-7.

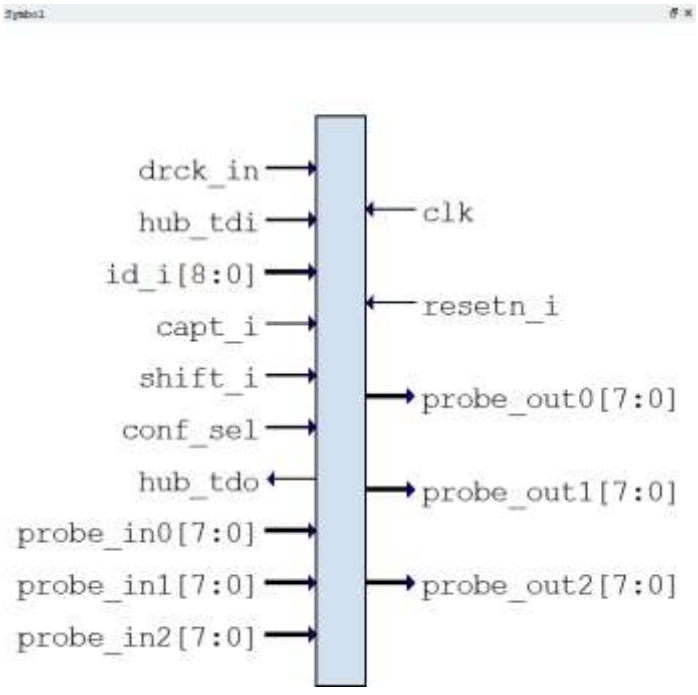

FIGURE 2-6 DVIO IP INTERFACE DIAGRAM

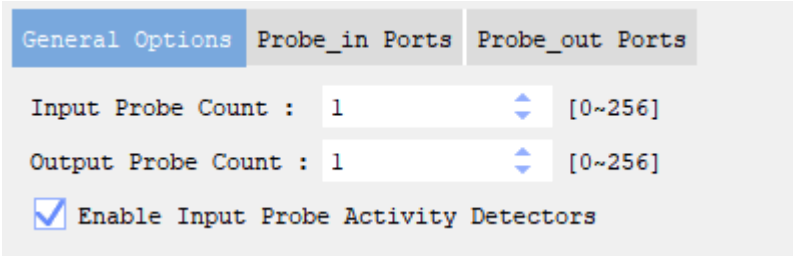

FIGURE 2-7 CONFIGURE DVIO IP PARAMETER INTERFACE

DVIO IP parameter configuration is divided into three interfaces: General Options, Probe_in Ports and Probe_out Ports pages.

(1) General Options

General Options is the IP port number configuration page. The interface is shown in Figure 2-8. For detailed parameters, see Table 2-2.

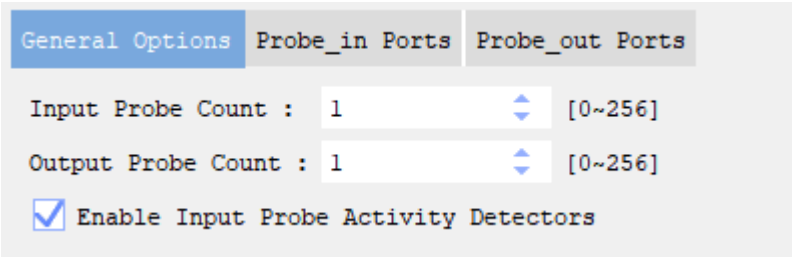

FIGURE 2-8 GENERAL OPTIONS PAGE

Table 2-2 General Options Page parameter configuration instructions

PARAMETERS / CONFIGURATION OPTIONS	PARAMETER DESCRIPTION	IP CONFIGURATION INTERFACE DEFAULT VALUE
Input Probe Count (0-256)	Probe_in Port number selection Configuration range: 0-256	1
Output Probe Count (0-256)	Probe_out Port number selection Configuration range: 0-256	1
Enable Input Probe Activity Detectors	Input port activity detector enable selection Check: Enable (can use software to monitor changes in the upper and lower edges of the signal)	Enable

(2) Probe_in Ports

The Probe_in Ports interface is shown in Figure 2-9. According to the Input Probe Count (0-256) parameter value on the General Options page, the input port is determined and displayed accordingly. Each probe_in port contains the same parameters. See Table 2-3 for relevant parameter setting instructions.

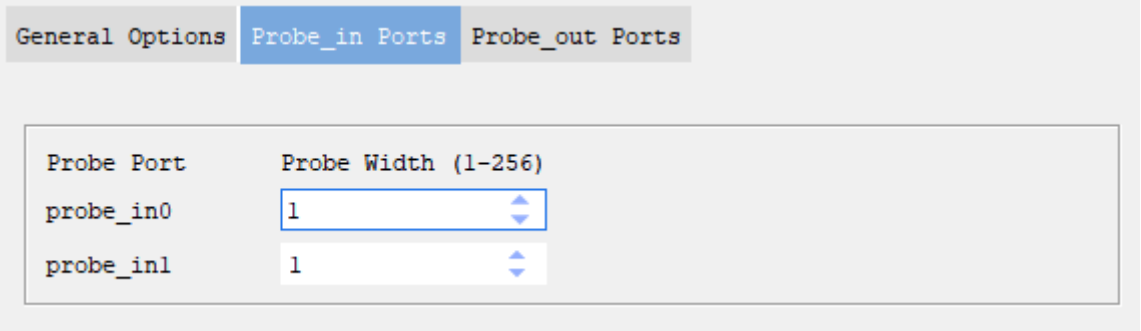

FIGURE 2-9 PROBE_IN PORTS PAGE

Table 2-3 Probe_in Ports page parameter configuration instructions

PARAMETERS / CONFIGURATION OPTIONS	PARAMETER DESCRIPTION	IP CONFIGURATION INTERFACE DEFAULT VALUE
Probe Port	Input port probe_in<$N>[3] Quantity by Input Probe Count Determined by parameter value	N/A
Probe Width (1-256)	Input port bit width setting Optional bit width : 1-256	1

Note: " N / A " means this parameter is not configurable.

(3) Probe_out Ports

The Probe_out Ports interface is shown in Figure 2-10. According to the Output Probe Count (0-256) parameter value on the General Options page, the output port is determined and displayed accordingly. Each probe_out port contains the same parameters. See Table 2-4 for relevant parameter setting instructions.

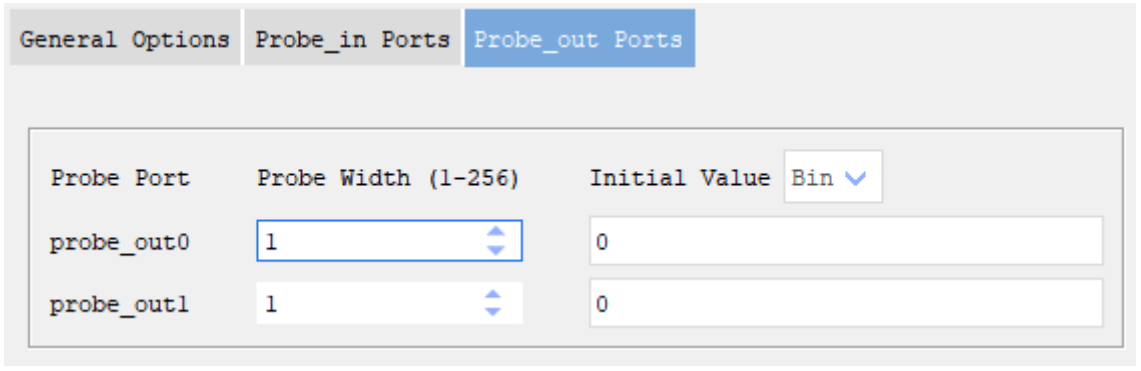

FIGURE 2-10 PROBE_OUT PORTS PAGE

[3] <$N> value range: 0~255, corresponding to input ports probe_in0~probe_in255 respectively.

Table 2-4 Probe_out Ports Page parameter configuration instructions

PARAMETERS / CONFIGURATION OPTIONS	PARAMETER DESCRIPTION	IP CONFIGURATION INTERFACE DEFAULT VALUE
Probe Port	Output port probe_out<$N>[4] Quantity by Output Probe Count Determined by parameter value	N/A
Probe Width (1-256)	Output port bit width setting Optional bit width : 1-256	1

Note: " N / A " means this parameter is not configurable.

3. Generate IP

After the parameter configuration is completed, click the <Generate> button in the upper left corner to generate the DVIO IP code corresponding to the user-specific settings. The generated IP information report interface is shown in Figure 2-11.

FIGURE 2-11 DVIO IP GENERATE REPORT INTERFACE

After the IP is successfully generated, the file shown in Table 2-5 will be output under the Project path specified in Figure 2-5.

Table 2-5 DVIO IP Generated output file

OUTPUT FILE[5]	DESCRIPTION
$instname.v	Generated IP top level.v document.
$instname.idf	Generated IP configuration file.
/rtl/*	Generated IP RTL _ code files.
/rev_1	The default output path of comprehensive reports. (This folder will only be generated after specifying the synthesis tool)
readme.txt	readme File describing the IP After generation, the structure of the directory is generated.

2.3 DVIO_Jtag_Hub

2.3.1 Functional Overview

DVIO_Jtag_Hub IP is used to connect the JTAG port and DVIO IP. By supporting Hub id, the number of supported DVIO units is expanded, supporting up to 15 DVIO connections. The system connection diagram is shown in Figure 2-12.

[4] <$N> value range: 0~255, corresponding to the output ports probe_out0~probe_out255 respectively.
[5] $instname is the instantiated name entered by the user; "*" is a wildcard character, replacing files of the same type.

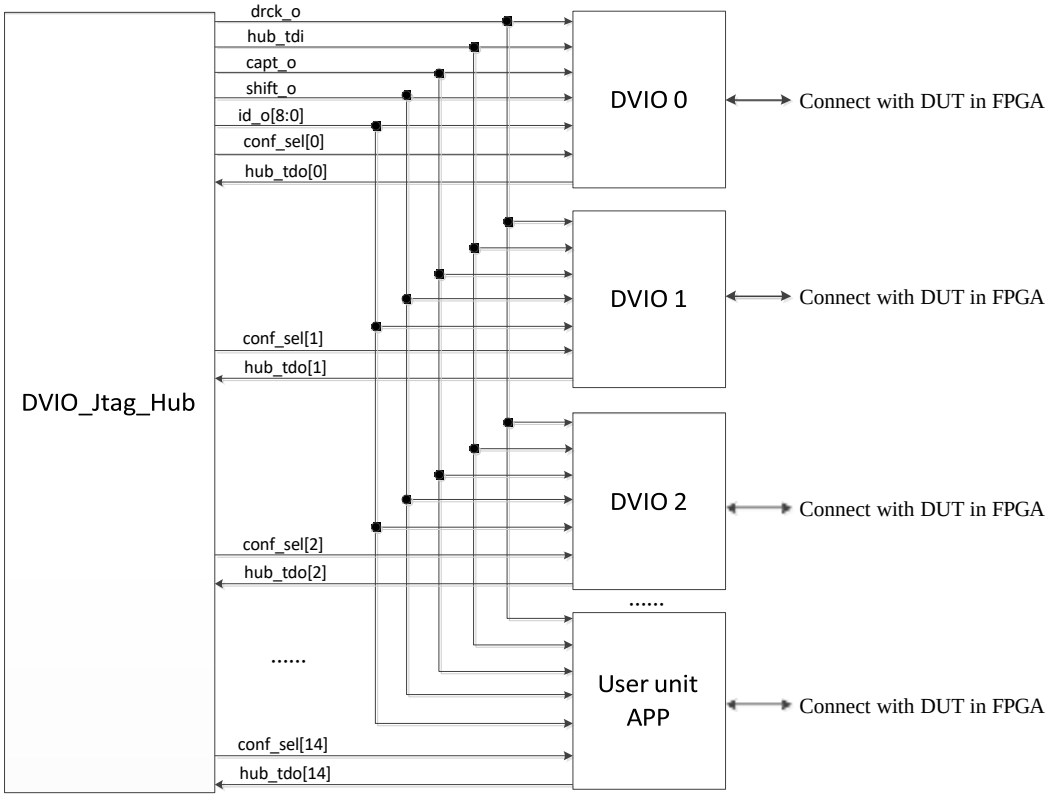

FIGURE 2-12 SYSTEM CONNECTION DIAGRAM

2.3.2 Interface Description

1. Interface diagram

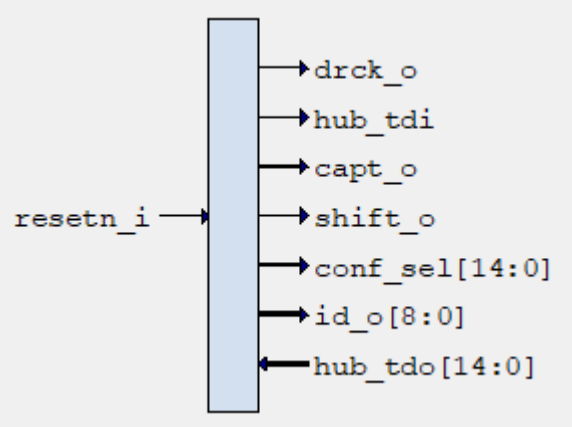

FIGURE 2-13 DVIO_JTAG_HUB IP INTERFACE DIAGRAM

2. Interface list

Table 2-6 DVIO_Jtag_Hub interface list

PORT NAME	INPUT/ OUTPUT	DESCRIPTION
resetn_i	input	Global reset signal, ' 0 ' is active.
drck_o	output	Jtag Hub IP outputs a clock to the user side, with the same frequency as jtag tck.
hub_tdi	output	Jtag Hub IP outputs Jtag tdi data to the user side.
capt_o	output	Capture signal output by Jtag Hub IP.
shift_o	output	The shift signal output by Jtag Hub IP.
conf_sel[14:0]	output	Jtag Hub IP output enable selection signal. Supports 15 enable selections.
id_o[8:0]	output	The hub id selection signal output by Jtag Hub IP.
hub_tdo[14:0]	output	The tdo data input to JtagHub IP comes from 15 User APP modules.

2.3.3 Timing model

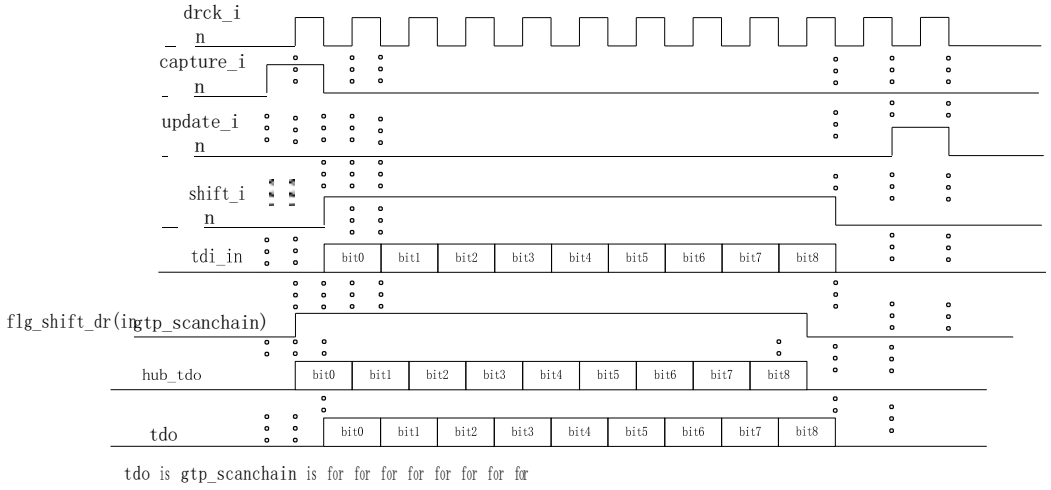

FIGURE 2-14 DVIO_JTAG_HUB WITH SCANCHAIN INTERFACE TIMING

2.3.4 Module instantiation

The customized configuration of DVIO_Jtag_Hub IP can be completed through the IPC tool, and the required IP module can be instantiated and generated. For specific usage of IPC tools, please refer to IP_Compiler_User_Guide[3].

The main steps for instantiating the DVIO_Jtag_Hub IP module are described below.

1. Select IP

Open the IPC software, enter the IP selection interface, and select the corresponding

version of DVIO_Jtag_Hub in the System/Tools/Debug directory. The IP selection path is shown in Figure 2-15. Then set the Pathname and Instance Name on the right page. The project instantiation interface is shown in Figure 2-16.

Notice:

The software must be:

- 2022.2-SP2 SP and above Version;
- 2023.1 and above versions.

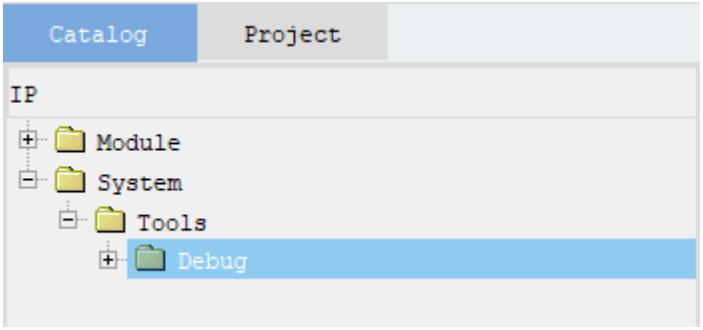

FIGURE 2-15 DVIO_JTAG_HUB IP SELECT PATH

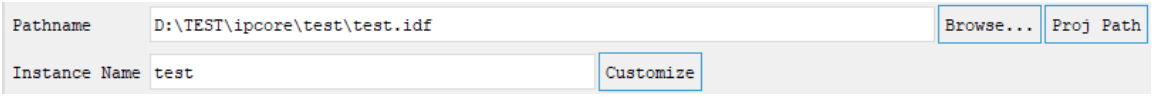

FIGURE 2-16 PROJECT INSTANTIATION INTERFACE

2. Configure IP parameter

After IP selection is completed, click <Customize> to enter the DVIO_Jtag_Hub IP parameter configuration interface, as shown in Figure 2-17.

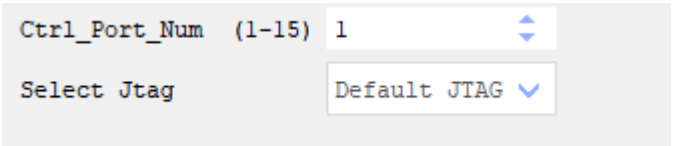

FIGURE 2-17 CONFIGURE DVIO_JTAG_HUB IP PARAMETER INTERFACE

Table 2-7 DVIO_Jtag_Hub IP Configuration parameter description

PARAMETERS / CONFIGURATION OPTIONS	PARAMETER DESCRIPTION	IP CONFIGURATION INTERFACE DEFAULT VALUE
Ctrl_Port_Num (1-15)	Optional number of User APP modules connected to DVIO_Jtag_Hub IP: 1~15	1
Select Jtag	JTAG port type selection, optional types: 1) Default JTAG, the default JTAG port, is provided by the development board; 2) USER JTAG, user JTAG port, provided by the user.	Default JTAG

3. Generate IP

After the parameter configuration is completed, click the <Generate> button in the upper left corner to generate the DVIO_Jtag_Hub IP code corresponding to the user-specific settings. The information report interface for generating IP is shown in Figure 2-18.

FIGURE 2-18 DVIO_JTAG_HUB IP GENERATE REPORT INTERFACE

After the IP is successfully generated, the file shown in Table 2-8 will be output under the Project path specified in Figure 2-16.

Table 2-8 DVIO_Jtag_Hub IP Generated output file

OUTPUT FILE[6]	DESCRIPTION
$instname.v	Generated IP top level.v document.
$instname.idf	Generated IP configuration file.
/rtl/*	Generated IP RTL code file.
/rev_1	The default output path of comprehensive reports. (This folder will only be generated after specifying the synthesis tool)
readme.txt	readme file, describing the structure of the generated directory after IP generation.

[6] $instname is the instantiated name entered by the user; "*" is a wildcard character, replacing files of the same type.

Chapter 3 Appendix

3.1 Reference documentation

[1] Pango_Design_Suite_Quick_Start_Tutorial

[2] Pango_Design_Suite_User_Guide

[3] IP_Compiler_User_Guide

[4] Simulation_User_Guide

3.2 Glossary

J

JTAG	Joint Test Action Group

3.3 Abbreviation list

D

DVIO	Debugger Virtual Input/Output
DVIO_Jtag_Hub	Debug Virtual Input/Output Jtag Hub

I

IPC	IP Compiler

P

PDS	Pango Design Suite

3.4 Statement

3.4.1 Copyright Notice

3.4.2 Disclaimer

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