Application Note 132

Voice Video and Data Communications using a 2-Port Switch and Generic Bus Interface

KSZ8842-16MQL/MVL

Introduction

The IP-Telephony market is booming, due to the ease of use of the technology and the low cost it promises consumers for making voice and video calls using the technology. Conveniently, it runs on the ever popular Ethernet LAN technology, which currently supports over 95 percent of all companies' networks, and works like computer data on the LAN. Using VoIP (Voice over Internet Protocol), voice signals can be packetized like computer data packets and transmitted worldwide over the Internet. This is why VoIP is a win-win solution for everyone.

Packet-switched VoIP converts voice signals into packets and each VoIP packet includes both the sender's/receiver's network addresses. The VoIP packets can traverse any IP network and choose alternate paths because the destination address is included in the packet, so the VoIP is flexible, interoperable and portable.

IP telephone has a NID (Network Interface Device) built into it just like a computer must have a NIC (Network Interface Card) inside of it to connect to the LAN. The NID is the single most important component for VoIP applications and LAN connections because it provides its physical address on the LAN.

Micrel's KSZ8842-16MQL, a network interface device, is the industry's first 2-port Ethernet Layer-2 Managed switch and 8/16 bit generic host bus interface as well as:

- A KSZ8842-32MQL, 32-bit Generic Bus (synchronous or asynchronous) for different host processor interfaces
- 1K Dynamic and 8 Static MAC addresses, 16 VLAN entries and 34 MIB Counters per port
- Supports programmable rate limiting on the ingress/egress ports and 4 priority queues
- Dynamic Packet Memory scheme which fully utilizes 8KB buffer memory in 4B increments
- LinkMD cable diagnostic capabilities. Determines distance to fault and also cable length measurement
- Prevents congestion in the switch with a MAC filtering function to filter or forward unknown unicast packets (useful for VoIP applications)
- HP Auto-MDIX crossover with disable and enable option
- Separate Link and Activity pins on all ports
- Alternative LQFP packaging available in the KSZ8842-16MVL and -32MVL devices

Figure 1 below shows a system level block diagram of the KSZ8842-16M being used in a VoIP application.

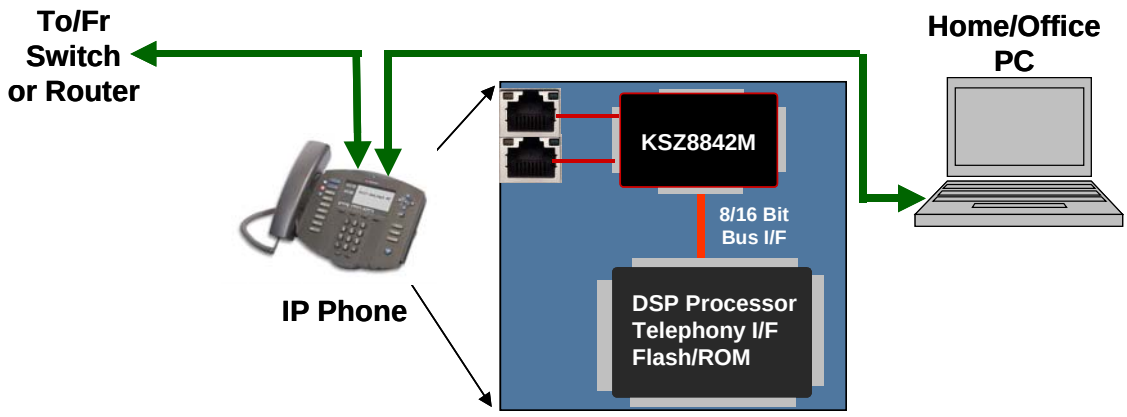

Figure 1: KSZ8842-16MQL Embedded Two-port Ethernet Switch for VoIP Applications

A detailed VoIP phone block diagram is shown in Figure 2 below. The KSZ8842M is designed to handle voice, video and data packets between the LAN connection and Host CPU interface. The following sections focus on how to connect the KSZ8842-16MQL 16-bit generic bus interface to a DSP Host processor.

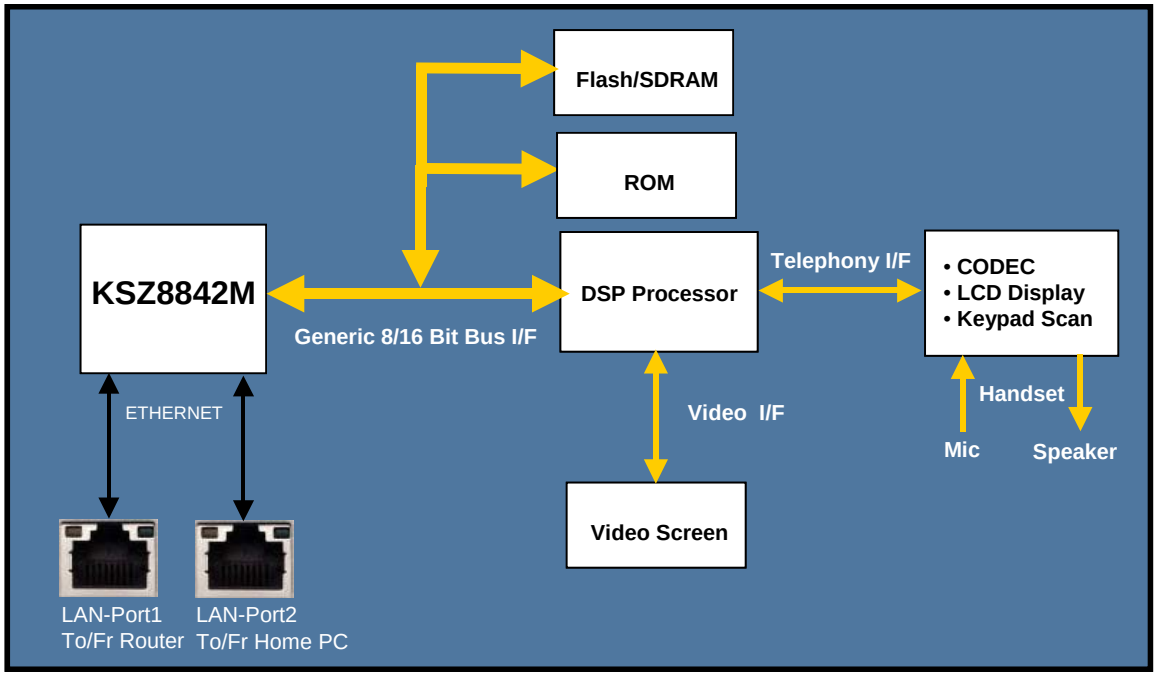

Figure 2: VoIP Phone system level Block Diagram

General Description the Bus Interface between KSZ8842-16M and Processor

The KSZ8842-16MQL/MVL is 2-Port Ethernet Switch with non-PCI interface, and is designed to connect to an 8 or 16-bit bus interface. This application note provides a basic overview of system level signal connections based on 8 or 16-bit bus interfaces, in combination with or without EEPROM.

The KSZ8842-16MQL/MVL supports two transfer modes in the BIU (Bus Interface Unit):

- Asynchronous mode
- Synchronous mode

Both asynchronous and synchronous signals are independent of each other.

In order to handshake in the different bus interfaces (ISA-like, EISA-like or VLBus-like), the following sections will describe all bus interface signal connections using these two transfer modes.

8 or 16-Bit Bus Interface Signal Connections for the KSZ8842-16MQL/MVL

8 or 16-Bit Asynchronous Bus Interface Mode

In the asynchronous bus interface mode, the KSZ8842-16MQL/MVL host bus read/write operation is as an 8 or 16-bit peripheral. All signals are listed in Table 1 and connections are shown in Figures 3, 4, and 5 respectively for 8-bit configurations, and in Figures 6, and 7 for 16-bit operations. The timing waveform is shown in Figure 8.

Table 1: KSZ8842-16MQL/MVL Bus Interface Signals for 8 or 16-Bit Asynchronous Mode

Signal	Type	Asynchronous	
		ADSN = 0 (ISA-like)	Using ADSN (EISA-like)
A[15:1]	I	Address	Address
D[15:0]	I/O	Data (8 or 16-bit)	Data (8 or 16-bit)
AEN	I	Address Enable (active low)	Address Enable (active low)
BE1N,BE0N	I	Byte Enable (active low)	Byte Enable (active low)
ADSN	I	Always enabled Address Strobe (Tied low)	Address Strobe is used to latch A[15:1], AEN,BE1N/BE0N
LDEVN	O	Local Device (asserted low when right address decoded)	Local Device (asserted low when right address decoded)
INTRN	O	Interrupt (asserted low when interrupt status bit set)	Interrupt (asserted low when interrupt status bit set)
RDN	I	Asynchronous Read (active low)	Asynchronous Read (active low)
WRN	I	Asynchronous Write (active low)	Asynchronous Write (active low)
ARDY	O	Asynchronous Ready (active high)	Asynchronous Ready (active high)
VLBUSN	I	Tied high for non-VLBus	Tied high for non-VLBus
CYCLEN	I	Not used (Tied high)	Not used (Tied high)
SWR	I	Not used (Tied high)	Not used (Tied high)
RDYRTNN	I	Not used (Tied high)	Not used (Tied high)
BCLK	I	Not used (Tied low)	Not used (Tied low)
SRDYN	O	Not used (No connect)	Not used (No connect)

Note: These signals BE3N, BE2N, DATACSN are not available (No Connect) in KSZ8842-16MQL/MVL device

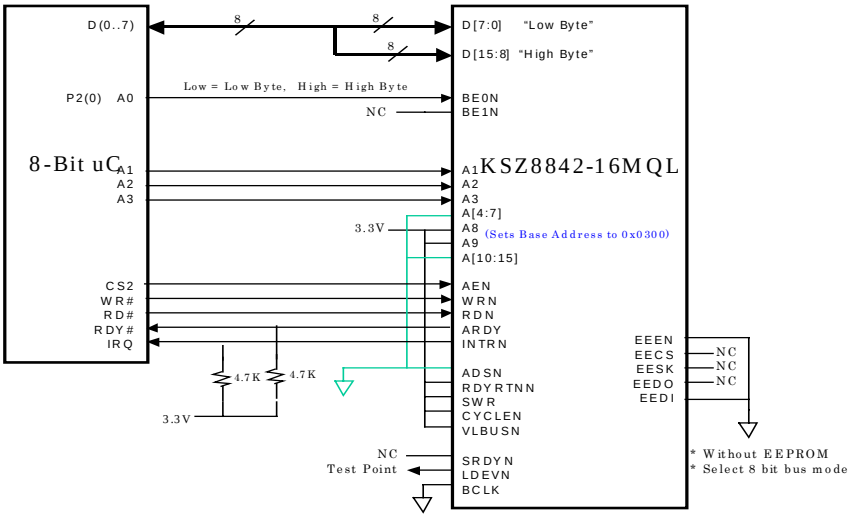

Figure 3: 8-Bit Asynchronous ISA-like Bus Connections with A[3:1]

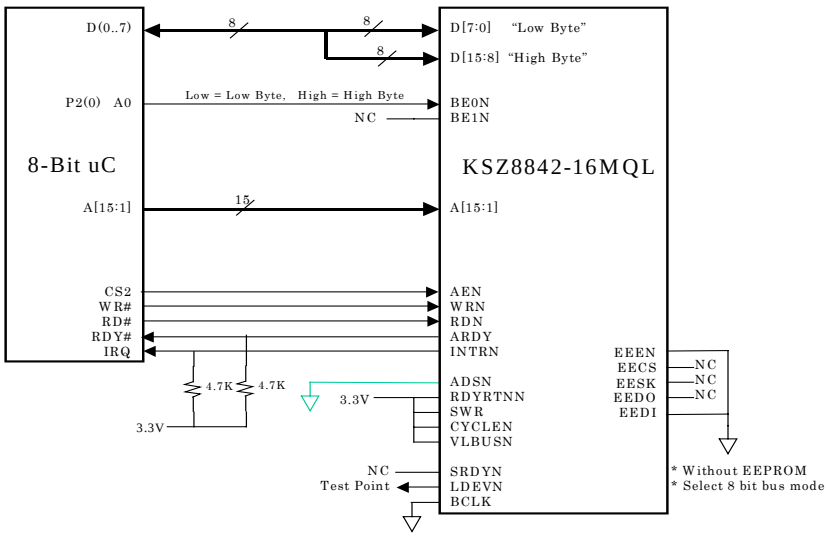

Figure 4: 8-Bit Asynchronous ISA-like Bus Connections with A[15:1]

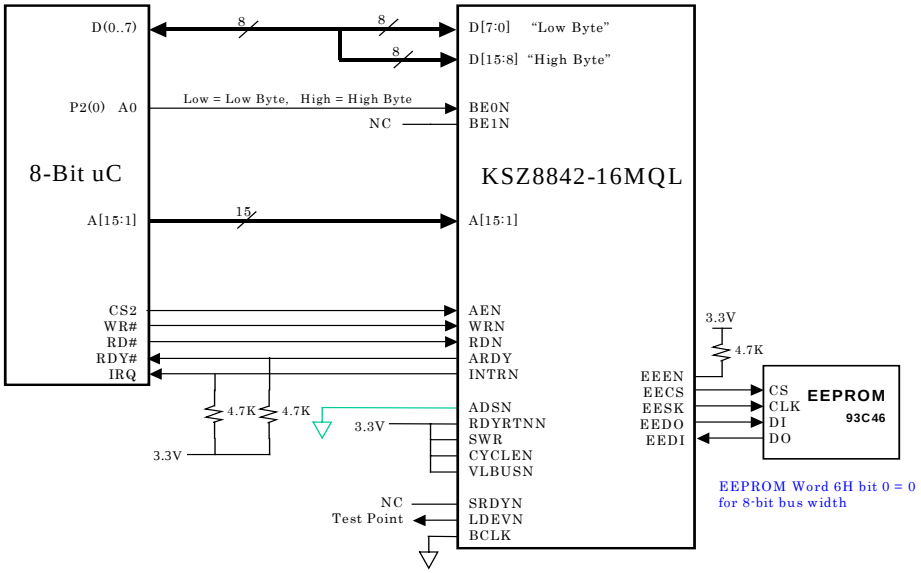

Figure 5: 8-Bit Asynchronous ISA-like Bus Connections with EEPROM

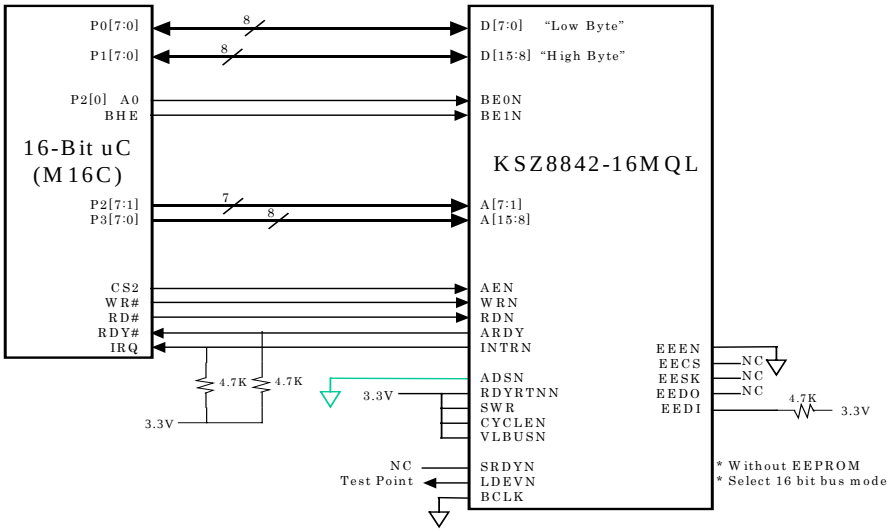

Figure 6: 16-Bit Asynchronous ISA-like Bus Connections without EEPROM

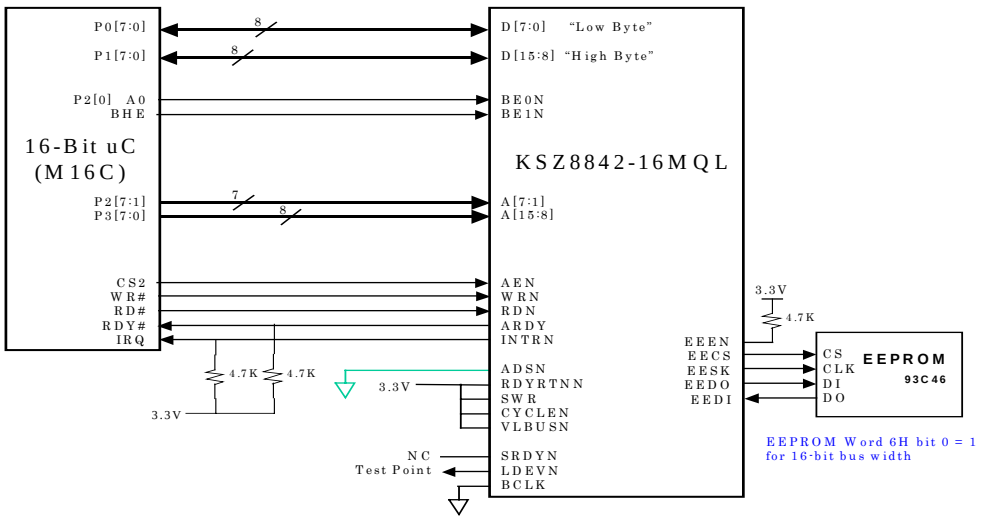

Figure 7: 16-Bit Asynchronous ISA-like Bus Connections with EEPROM

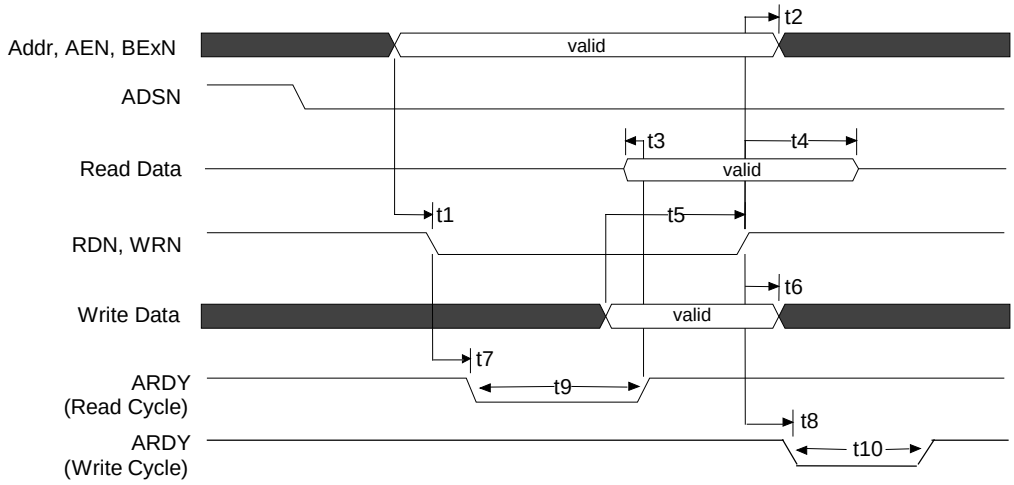

Figure 8: Asynchronous Read & Write Cycles Timing Waveform – ADSN = 0

Symbol	Parameter	Min	Typ	Max	Unit
t1	A1-A15, AEN, BExN[3:0] valid to RDN, WRN active	2			ns
t2	A1-A15, AEN, BExN[3:0] hold after RDN, WRN inactive (assume ADSN tied Low)	1			ns
t3	Read data valid to ARDY rising			0.8	ns
t4	Read data to hold RDN inactive	4			ns
t5	Write data setup to WRN inactive	4			ns
t6	Write data hold after WRN inactive	2			ns
t7	Read active to ARDY Low			8	ns
t8	Write inactive to ARDY Low			8	ns
t9	ARDY low (wait time) in read cycle (Note1) (It is 0ns to read bank select register) (It is 110ns to read QMU data register)	0	110		ns
t10	ARDY low (wait time) in write cycle (Note1) (It is 0ns to write bank select register) (It is 85ns to write QMU data register)	0	85		ns

Note1: When CPU finished current Read or Write operation, it can do next Read or Write operation even the ARDY is low. During Read or Write operation if the ADRY is low, the CPU has to keep the RDN/WRN low until the ARDY returns to high.

16-Bit Synchronous Bus Interface Mode

In the synchronous bus interface mode, the KSZ8842-16MQL/MVL host bus read/write operation is as a 16-bit peripheral. All signals are listed in the Table 2 and connections are shown in Figures 9 and 10. The timing waveform is shown in Figures 11 and 12.

Table 2: KSZ8842-16MQL/MVL Bus Interface Signals for 16-Bit Synchronous Mode

Signal	Type	Synchronous
		VLBUSN = 0 (VLBus-like)
A[15:1]	I	Address
D[15:0]	I/O	Data (8 or 16-bit)
AEN	I	Address Enable (active low)
BE1N, BE0N	I	Byte Enable (active low)
ADSN	I	Address Strobe is used to latch A[15:1], AEN,BE1N/BE0N
LDEVN	O	Local Device (asserted low when right address decoded)
INTRN	O	Interrupt (asserted low when interrupt status bit set)
RDN	I	Not used (Tied high)
WRN	I	Not used (Tied high)
ARDY	O	Not used
VLBUSN	I	Tied low for VLBus-like cycle
CYCLEN	I	CYCLEN is used to sample SWR when it is asserted
SWR	I	Synchronous write cycles when high and read cycles when low
RDYRTNN	I	Ready Return is used by the Host to indicate the end of Read or Write in VLBus-like cycle
BCLK	I	Bus Clock is used for Synchronous transfer
SRDYN	O	Synchronous Ready is used to indicate that data is ready to Read/Write

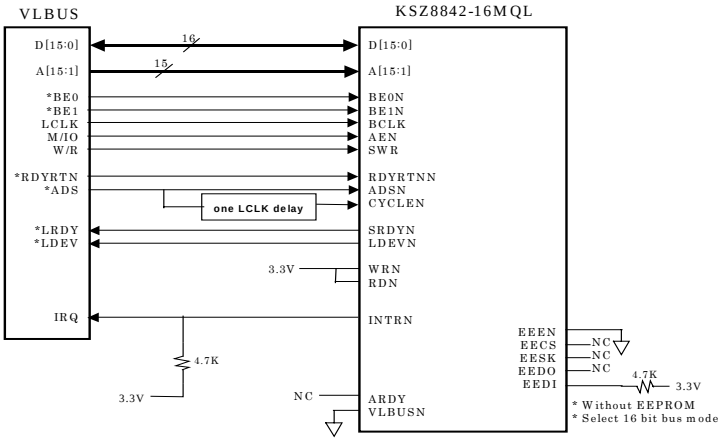

Figure 9: 16-Bit Synchronous VLBUS-like Bus Connections without EEPROM

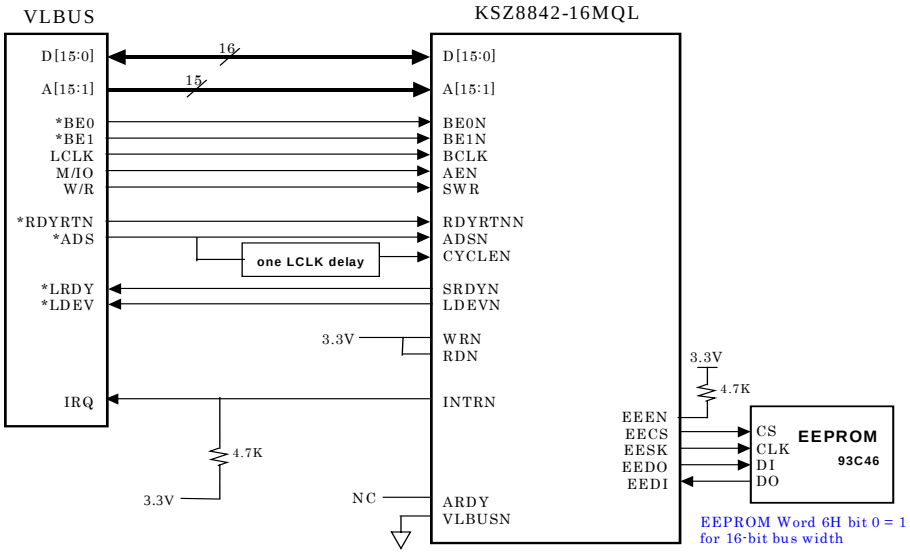

Figure 10: 16-Bit Synchronous VLBUS-like Bus Connections with EEPROM

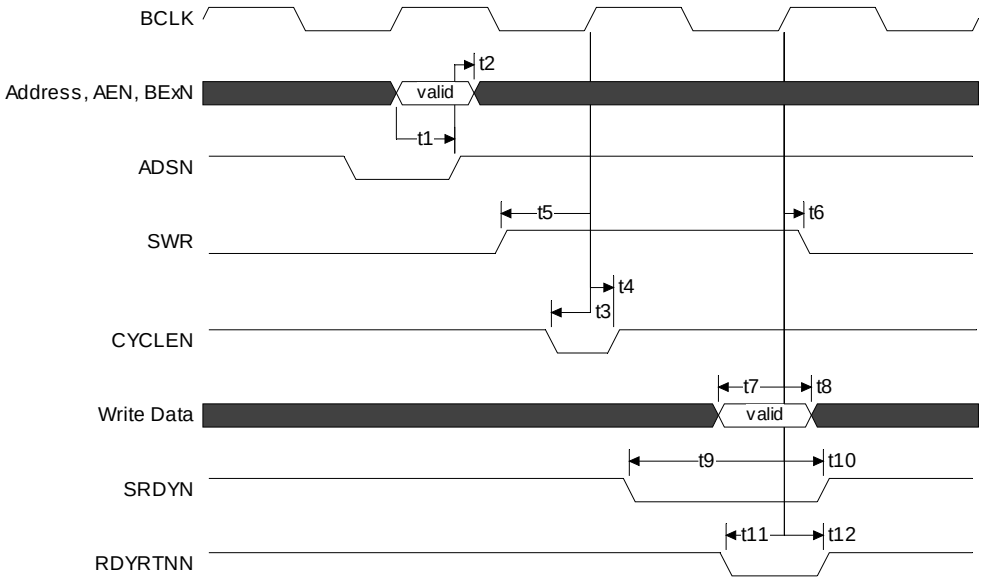

Figure 11: Synchronous Write Cycle Timing Waveform – VLBUS = 0

Symbol	Parameter	Min	Typ	Max	Unit
t1	A1-A15, AEN, BExN[3:0] setup to ADSN rising	4			ns
t2	A1-A15, AEN, BExN[3:0] hold after ADSN rising	2			ns
t3	CYCLEN setup to BCLK rising	4			ns
t4	CYCLEN hold after BCLK rising (non-burst mode)	2			ns
t5	SWR setup to BCLK	4			ns
t6	SWR hold after BCLK rising with SRDYN active	0			ns
t7	Write data setup to BCLK rising	5			ns
t8	Write data hold from BCLK rising	1			ns
t9	SRDYN setup to BCLK	8			ns
t10	SRDYN hold to BCLK	1			ns
t11	RDYRTNN setup to BCLK	4			ns
t12	RDYRTNN hold to BCLK	1			ns

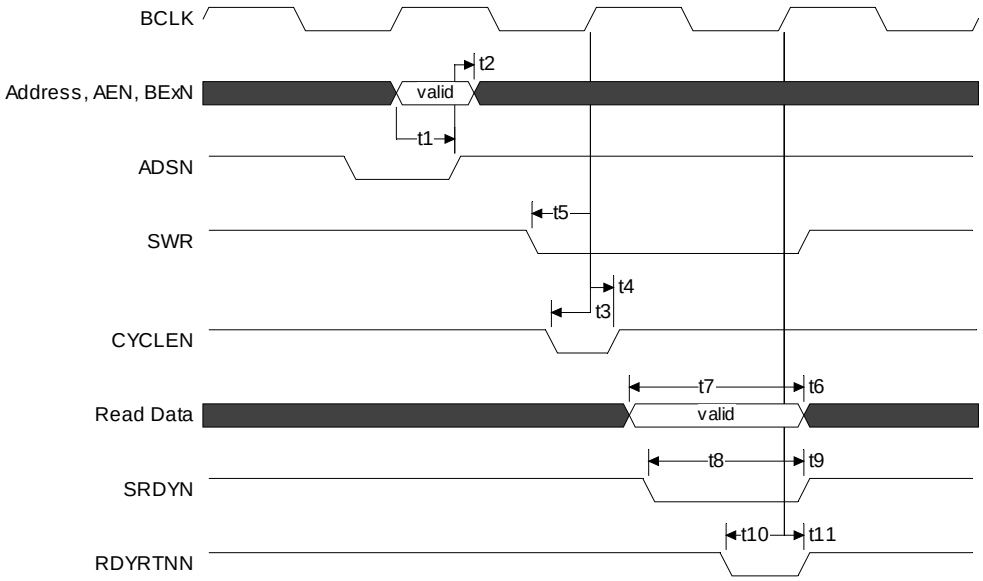

Figure 12: Synchronous Read Cycle Timing Waveform – VLBUS = 0

Symbol	Parameter	Min	Typ	Max	Unit
t1	A1-A15, AEN, BExN[3:0] setup to ADSN rising	4			ns
t2	A1-A15, AEN, BExN[3:0] hold after ADSN rising	2			ns
t3	CYCLEN setup to BCLK rising	4			ns
t4	CYCLEN hold after BCLK rising (non-burst mode)	2			ns
t5	SWR setup to BCLK	4			ns
t6	Read data hold from BCLK rising	1			ns
t7	Read data setup to BCLK	8			ns
t8	SRDYN setup to BCLK	8			ns
t9	SRDYN hold to BCLK	1			ns
t10	RDYRTNN setup to BCLK rising	4			ns
t11	RDYRTNN hold after BCLK rising	1			ns

Conclusion

By using this Application Note, customers are able to design a VoIP phone system with the KSZ8842-16MQL/MVL to easily connect to their FPGAs or processors as well as any other application requiring a two-port switch and generic bus interface for Embedded and Industrial Ethernet applications.

In addition, Micrel provides the flexibility of offering a single port KSZ8841-16MQL/MVL MAC/PHY plus generic bus interface part that is 100% footprint compatible for single port applications. This provides engineers with the flexibility to design two products using a single print circuit board and software driver, thereby saving time, money and efforts in the development cycle.

All of the development collateral including data sheet, schematics, gerber file, IBIS module and software driver can be downloaded from Micrel website. Evaluation boards and user's guide are also available.

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