Path Summary

	Property	Value
1	From Node	rx_8b_10b:loop_ser[7].rx_8b_10b_0|rx_8b_10b_4x:rx_8b_10b_4x_0|rx_ddr:rx_ddr_0|altddio_in:RXDDR|ddio_in_s6f:auto_generated|dataout_l[0]
2	To Node	rx_8b_10b:loop_ser[7].rx_8b_10b_0|rx_8b_10b_4x:rx_8b_10b_4x_0|ser_in_2x_reg_0[1]
3	Launch Clock	SYS_PLL0|pll0_inst|altera_pll_i|general[5].gpll~PLL_OUTPUT_COUNTER|divclk (INVERTED)
4	Latch Clock	SYS_PLL0|pll0_inst|altera_pll_i|general[5].gpll~PLL_OUTPUT_COUNTER|divclk (INVERTED)
5	Data Arrival Time	14.016
6	Data Required Time	11.646
7	Slack	-2.370 (VIOLATED)

Statistics

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	3.333					
2	Clock Skew	-0.861					
3	Data Delay	4.772					
4	Number of Logic Levels		1				
5	Physical Delays						
1	Arrival Path						
1	Clock						
1	IC		6	3.568	47	0.000	2.045
2	Cell		6	4.010	53	0.179	1.528
2	Data						
1	IC		2	4.316	90	0.000	4.316
2	Cell		3	0.456	10	0.078	0.260
3	uTco		1	0.000	0	0.000	0.000
2	Required Path						
1	Clock						
1	IC		6	2.698	45	0.000	1.376
2	Cell		5	3.306	55	0.309	1.272
3	PLL Compensation		1	-0.149	0	-0.149	-0.149

Data Path

Data Arrival

	Total	Incr	RF	Type	Fanout	Location	Element
1	1.666	1.666					launch edge time
2	9.244	7.578					clock path
1	1.666	0.000					source latency

	Total	Incr	RF	Type	Fanout	Location	Element
2	1.666	0.000			1	PIN_G15	ref_clk125
3	1.666	0.000	RR	IC	1	IOIBUF_X46_Y61_N1	ref_clk125~input|i
4	2.570	0.904	RR	CELL	2	IOIBUF_X46_Y61_N1	ref_clk125~input|o
5	3.316	0.746	RR	IC	1	PLLREFCLKSELECT_X68_Y60_N0	SYS_PLL0|pll0_inst|altera_pll_i|general[0].gpll~PLL_REFCLK_SELECT|clkin[1]
6	3.649	0.333	RR	CELL	1	PLLREFCLKSELECT_X68_Y60_N0	SYS_PLL0|pll0_inst|altera_pll_i|general[0].gpll~PLL_REFCLK_SELECT|clkout
7	3.649	0.000	RR	IC	10	FRACTIONALPLL_X68_Y54_N0	SYS_PLL0|pll0_inst|altera_pll_i|general[0].gpll~FRACTIONAL_PLL|refclkin
8	3.828	0.179	RR	CELL	6	FRACTIONALPLL_X68_Y54_N0	SYS_PLL0|pll0_inst|altera_pll_i|general[0].gpll~FRACTIONAL_PLL|vcoph[0]
9	3.828	0.000	RR	IC	1	PLLOUTPUTCOUNTER_X68_Y58_N1	SYS_PLL0|pll0_inst|altera_pll_i|general[5].gpll~PLL_OUTPUT_COUNTER|vco0ph[0]
10	5.356	1.528	RR	CELL	1	PLLOUTPUTCOUNTER_X68_Y58_N1	SYS_PLL0|pll0_inst|altera_pll_i|general[5].gpll~PLL_OUTPUT_COUNTER|divclk
11	6.133	0.777	FF	IC	1	CLKCTRL_G9	GCLKE5_0|GCLKE_altclkctrl_vch_component|sd1|inclk
12	6.480	0.347	FF	CELL	61	CLKCTRL_G9	GCLKE5_0|GCLKE_altclkctrl_vch_component|sd1|outclk
13	8.525	2.045	FF	IC	3	DDIOINCELL_X59_Y0_N31	loop_ser[7].rx_8b_10b_0|rx_8b_10b_4x_0|rx_ddr_0|RXDDR|auto_generated|ddio_ina[0]|clk
14	9.244	0.719	FR	CELL	1	DDIOINCELL_X59_Y0_N31	rx_8b_10b:loop_ser[7].rx_8b_10b_0|rx_8b_10b_4x:rx_8b_10b_4x_0|rx_ddr:rx_ddr_0|altddio_in:RXDDR|ddio_in_s6f:auto_generated|dataout_l[0]
3	14.016	4.772					data path
1	9.244	0.000		uTco	1	DDIOINCELL_X59_Y0_N31	rx_8b_10b:loop_ser[7].rx_8b_10b_0|rx_8b_10b_4x:rx_8b_10b_4x_0|rx_ddr:rx_ddr_0|altddio_in:RXDDR|

	Total	Incr	RF	Type	Fanout	Location	Element
							ddio_in_s6f:auto_generated|dataout_l[0]
2	9.362	0.118	FF	CELL	1	DDIOINCELL_X59_Y0_N31	loop_ser[7].rx_8b_10b_0|rx_8b_10b_4x_0|rx_ddr_0|RXDDR|auto_generated|ddio_ina[0]|regoutlo
3	13.678	4.316	FF	IC	1	LABCELL_X49_Y4_N18	loop_ser[7].rx_8b_10b_0|rx_8b_10b_4x_0|ser_in_2x_reg_0[1]~feeder|dataf
4	13.756	0.078	FF	CELL	1	LABCELL_X49_Y4_N18	loop_ser[7].rx_8b_10b_0|rx_8b_10b_4x_0|ser_in_2x_reg_0[1]~feeder|combout
5	13.756	0.000	FF	IC	1	FF_X49_Y4_N19	loop_ser[7].rx_8b_10b_0|rx_8b_10b_4x_0|ser_in_2x_reg_0[1]|d
6	14.016	0.260	FF	CELL	1	FF_X49_Y4_N19	rx_8b_10b:loop_ser[7].rx_8b_10b_0|rx_8b_10b_4x:rx_8b_10b_4x_0|ser_in_2x_reg_0[1]

Data Required

	Total	Incr	RF	Type	Fanout	Location	Element
1	4.999	4.999					latch edge time
2	11.716	6.717					clock path
1	4.999	0.000					source latency
2	4.999	0.000			1	PIN_G15	ref_clk125
3	4.999	0.000	RR	IC	1	IOIBUF_X46_Y61_N1	ref_clk125~input|i
4	5.903	0.904	RR	CELL	2	IOIBUF_X46_Y61_N1	ref_clk125~input|o
5	6.610	0.707	RR	IC	1	PLLREFCLKSELECT_X68_Y60_N0	SYS_PLL0|pll0_inst|altera_pll_i|general[0].gpll~PLL_REFCLK_SELECT|clkin[1]
6	6.919	0.309	RR	CELL	1	PLLREFCLKSELECT_X68_Y60_N0	SYS_PLL0|pll0_inst|altera_pll_i|general[0].gpll~PLL_REFCLK_SELECT|clkout
7	6.919	0.000	RR	IC	10	FRACTIONALPLL_X68_Y54_N0	SYS_PLL0|pll0_inst|altera_pll_i|general[0].gpll~FRACTIONAL_PLL|refclkin
8	6.770	-0.149	RR	COMP	6	FRACTIONALPLL_X68_Y54_N0	SYS_PLL0|pll0_inst|altera_pll_i|general[0].gpll~FRACTIONAL_PLL|vcoph[0]
9	6.770	0.000	RR	IC	1	PLLOUTPUTCOUNTER_X68_Y58_N1	SYS_PLL0|pll0_inst|altera_pll_i|general[5].gpll~PLL_OUTPUT_COUNTER|vco0ph[0]

	Total	Incr	RF	Type	Fanout	Location	Element
10	8.042	1.272	RR	CELL	1	PLLOUTPUTCOUNTER_X68_Y58_N1	SYS_PLL0|pll0_inst|altera_pll_i|general[5].gpll~PLL_OUTPUT_COUNTER|divclk
11	8.657	0.615	FF	IC	1	CLKCTRL_G9	GCLKE5_0|GCLKE_altclkctrl_vch_component|sd1|inclk
12	8.978	0.321	FF	CELL	61	CLKCTRL_G9	GCLKE5_0|GCLKE_altclkctrl_vch_component|sd1|outclk
13	10.354	1.376	FF	IC	1	FF_X49_Y4_N19	loop_ser[7].rx_8b_10b_0|rx_8b_10b_4x_0|ser_in_2x_reg_0[1]|clk
14	10.854	0.500	FR	CELL	1	FF_X49_Y4_N19	rx_8b_10b:loop_ser[7].rx_8b_10b_0|rx_8b_10b_4x:rx_8b_10b_4x_0|ser_in_2x_reg_0[1]
15	11.716	0.862					clock pessimism removed
3	11.646	-0.070					clock uncertainty
4	11.646	0.000		uTsu	1	FF_X49_Y4_N19	rx_8b_10b:loop_ser[7].rx_8b_10b_0|rx_8b_10b_4x:rx_8b_10b_4x_0|ser_in_2x_reg_0[1]