Path Summary

	Property	Value
1	From Node	rx_8b_10b:loop_ser[0].rx_8b_10b_0|rx_8b_10b_4x:rx_8b_10b_4x_0| rx_ddr:rx_ddr_0|altddio_in:RXDDR|ddio_in_s6f:auto_generated|dataout_h[0]
2	To Node	rx_8b_10b:loop_ser[0].rx_8b_10b_0|rx_8b_10b_4x:rx_8b_10b_4x_0| ser_in_2x_reg[0]
3	Launch Clock	SYS_PLL0|pll0_inst|altera_pll_i|general[5].gpll~PLL_OUTPUT_COUNTER| divclk (INVERTED)
4	Latch Clock	SYS_PLL0|pll0_inst|altera_pll_i|general[5].gpll~PLL_OUTPUT_COUNTER| divclk (INVERTED)
5	Multicycle - Setup End	2
6	Data Arrival Time	14.452
7	Data Required Time	14.889
8	Slack	0.437

Statistics

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	6.666					
2	Clock Skew	-0.921					
3	Data Delay	5.238					
4	Number of Logic Levels		1				
5	Physical Delays						
1	Arrival Path						
1	Clock						
1	IC		6	3.534	47	0.000	2.011
2	Cell		6	4.014	53	0.179	1.528
2	Data						
1	IC		2	4.800	92	0.000	4.800
2	Cell		3	0.438	8	0.076	0.262
3	uTco		1	0.000	0	0.000	0.000
2	Required Path						
1	Clock						
1	IC		6	2.634	44	0.000	1.312
2	Cell		5	3.307	56	0.309	1.272
3	PLL Compensation		1	-0.149	0	-0.149	-0.149

Data Path

Data Arrival

	Total	Incr	RF	Type	Fanout	Location	Element
1	1.666	1.666					launch edge time
2	9.214	7.548					clock path

	Total	Incr	RF	Type	Fanout	Location	Element
1	1.666	0.000					source latency
2	1.666	0.000			1	PIN_G15	ref_clk125
3	1.666	0.000	RR	IC	1	IOIBUF_X46_Y61_N1	ref_clk125~input|i
4	2.570	0.904	RR	CELL	2	IOIBUF_X46_Y61_N1	ref_clk125~input|o
5	3.316	0.746	RR	IC	1	PLLREFCLKSELECT_X68_Y60_N0	SYS_PLL0|pll0_inst|altera_pll_i|general[0].gpll~PLL_REFCLK_SELECT|clkin[1]
6	3.649	0.333	RR	CELL	1	PLLREFCLKSELECT_X68_Y60_N0	SYS_PLL0|pll0_inst|altera_pll_i|general[0].gpll~PLL_REFCLK_SELECT|clkout
7	3.649	0.000	RR	IC	10	FRACTIONALPLL_X68_Y54_N0	SYS_PLL0|pll0_inst|altera_pll_i|general[0].gpll~FRACTIONAL_PLL|refclkin
8	3.828	0.179	RR	CELL	6	FRACTIONALPLL_X68_Y54_N0	SYS_PLL0|pll0_inst|altera_pll_i|general[0].gpll~FRACTIONAL_PLL|vcoph[0]
9	3.828	0.000	RR	IC	1	PLLOUTPUTCOUNTER_X68_Y58_N1	SYS_PLL0|pll0_inst|altera_pll_i|general[5].gpll~PLL_OUTPUT_COUNTER|vco0ph[0]
10	5.356	1.528	RR	CELL	1	PLLOUTPUTCOUNTER_X68_Y58_N1	SYS_PLL0|pll0_inst|altera_pll_i|general[5].gpll~PLL_OUTPUT_COUNTER|divclk
11	6.133	0.777	FF	IC	1	CLKCTRL_G9	GCLKE5_0|GCLKE_altclkctrl_vch_component|sd1|inclk
12	6.480	0.347	FF	CELL	24	CLKCTRL_G9	GCLKE5_0|GCLKE_altclkctrl_vch_component|sd1|outclk
13	8.491	2.011	FF	IC	3	DDIOINCELL_X53_Y0_N65	loop_ser[0].rx_8b_10b_0|rx_8b_10b_4x_0|rx_ddr_0|RXDDR|auto_generated|ddio_ina[0]|clk
14	9.214	0.723	FR	CELL	1	DDIOINCELL_X53_Y0_N65	rx_8b_10b:loop_ser[0].rx_8b_10b_0|rx_8b_10b_4x:rx_8b_10b_4x_0|rx_ddr:rx_ddr_0|altddio_in:RXDDR|ddio_in_s6f:auto_generated|dataout_h[0]
3	14.452	5.238					data path
1	9.214	0.000		uTco	1	DDIOINCELL_X53_Y0_N65	rx_8b_10b:loop_ser[0].rx_8b_10b_0|rx_8b_10b_4x:rx_8b_10b_4x_0|rx_ddr:rx_ddr_0|

	Total	Incr	RF	Type	Fanout	Location	Element
							altddio_in:RXDDR| ddio_in_s6f:auto_generated| dataout_h[0]
2	9.314	0.100	FF	CELL	1	DDIOINCELL_X53_Y0_N65	loop_ser[0].rx_8b_10b_0| rx_8b_10b_4x_0|rx_ddr_0| RXDDR|auto_generated| ddio_ina[0]|regouthi
3	14.114	4.800	FF	IC	1	LABCELL_X23_Y3_N33	loop_ser[0].rx_8b_10b_0| rx_8b_10b_4x_0| ser_in_2x_reg[0]~feeder|dataf
4	14.190	0.076	FF	CELL	1	LABCELL_X23_Y3_N33	loop_ser[0].rx_8b_10b_0| rx_8b_10b_4x_0| ser_in_2x_reg[0]~feeder| combout
5	14.190	0.000	FF	IC	1	FF_X23_Y3_N35	loop_ser[0].rx_8b_10b_0| rx_8b_10b_4x_0| ser_in_2x_reg[0]|d
6	14.452	0.262	FF	CELL	1	FF_X23_Y3_N35	rx_8b_10b:loop_ser[0].rx_8b_10 b_0| rx_8b_10b_4x:rx_8b_10b_4x_0| ser_in_2x_reg[0]

Data Required

	Total	Incr	RF	Type	Fanout	Location	Element
1	8.332	8.332					latch edge time
2	14.959	6.627					clock path
1	8.332	0.000					source latency
2	8.332	0.000			1	PIN_G15	ref_clk125
3	8.332	0.000	RR	IC	1	IOIBUF_X46_Y61_N1	ref_clk125~input|i
4	9.236	0.904	RR	CELL	2	IOIBUF_X46_Y61_N1	ref_clk125~input|o
5	9.943	0.707	RR	IC	1	PLLREFCLKSELECT_X68_Y60_N 0	SYS_PLL0|pll0_inst|altera_pll_i| general[0].gpll~PLL_REFCLK_SE LECT|clkin[1]
6	10.252	0.309	RR	CELL	1	PLLREFCLKSELECT_X68_Y60_N 0	SYS_PLL0|pll0_inst|altera_pll_i| general[0].gpll~PLL_REFCLK_SE LECT|clkout
7	10.252	0.000	RR	IC	10	FRACTIONALPLL_X68_Y54_N0	SYS_PLL0|pll0_inst|altera_pll_i| general[0].gpll~FRACTIONAL_P LL|refclkin
8	10.103	-0.149	RR	COMP	6	FRACTIONALPLL_X68_Y54_N0	SYS_PLL0|pll0_inst|altera_pll_i| general[0].gpll~FRACTIONAL_P LL|vcoph[0]
9	10.103	0.000	RR	IC	1	PLLOUTPUTCOUNTER_X68_Y5 8_N1	SYS_PLL0|pll0_inst|altera_pll_i| general[5].gpll~PLL_OUTPUT_C

	Total	Incr	RF	Type	Fanout	Location	Element
							OUNTER|vco0ph[0]
10	11.375	1.272	RR	CELL	1	PLLOUTPUTCOUNTER_X68_Y58_N1	SYS_PLL0|pll0_inst|altera_pll_i|general[5].gpll~PLL_OUTPUT_COUNTER|divclk
11	11.990	0.615	FF	IC	1	CLKCTRL_G9	GCLKE5_0|GCLKE_altclkctrl_vch_component|sd1|inclk
12	12.311	0.321	FF	CELL	24	CLKCTRL_G9	GCLKE5_0|GCLKE_altclkctrl_vch_component|sd1|outclk
13	13.623	1.312	FF	IC	1	FF_X23_Y3_N35	loop_ser[0].rx_8b_10b_0|rx_8b_10b_4x_0|ser_in_2x_reg[0]|clk
14	14.124	0.501	FR	CELL	1	FF_X23_Y3_N35	rx_8b_10b:loop_ser[0].rx_8b_10b_0|rx_8b_10b_4x:rx_8b_10b_4x_0|ser_in_2x_reg[0]
15	14.959	0.835					clock pessimism removed
3	14.889	-0.070					clock uncertainty
4	14.889	0.000		uTsu	1	FF_X23_Y3_N35	rx_8b_10b:loop_ser[0].rx_8b_10b_0|rx_8b_10b_4x:rx_8b_10b_4x_0|ser_in_2x_reg[0]