Designing Stable Control Loops

By Dan Mitchell and Bob Mammano

ABSTRACT

The objective of this topic is to provide the designer with a practical review of loop compensation techniques applied to switching power supply feedback control. A top-down system approach is taken starting with basic feedback control concepts and leading to step-by-step design procedures, initially applied to a simple buck regulator and then expanded to other topologies and control algorithms. Sample designs are demonstrated with Mathcad simulations to illustrate gain and phase margins and their impact on performance analysis.

I. INTRODUCTION

Insuring stability of a proposed power supply solution is often one of the more challenging aspects of the design process. Nothing is more disconcerting than to have your lovingly crafted breadboard break into wild oscillations just as it is being demonstrated to the boss or customer, but insuring against this unfortunate event takes some analysis which many designers view as formidable. Paths taken by design engineers often emphasize either cut-and-try empirical testing in the laboratory or computer simulations looking for numerical solutions based on complex mathematical models. While both of these approaches have a place in circuit design, a basic understanding of feedback theory will usually allow the definition of an acceptable compensation network with a minimum of computational effort.

II. STABILITY DEFINED

Fig. 1 gives a quick illustration of at least one definition of stability. In its simplest terms, a system is stable if, when subjected to a perturbation from some source, its response to that perturbation eventually dies out. Note that in any practical system, instability cannot result in a completely unbounded response as the system will either reach a saturation level – or fail. Oscillation in a switching regulator can, at most, vary the duty cycle between zero and 100% and while that may not prevent failure, it will ultimate limit the response of an unstable system.

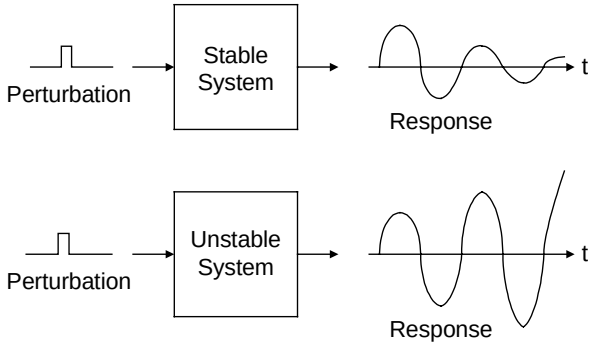


Fig. 1. Definition of stability.

Another way of visualizing stability is shown in Fig. 2. While this graphically illustrates the concept of system stability, it also points out that we must make a further distinction between large-signal and small-signal stability. While small-signal stability is an important and necessary criterion, a system could satisfy this requirement and yet still become unstable with a large-signal perturbation. It is important that designers remember that all the gain and phase calculations we might perform are only to insure small-signal stability. These calculations are based upon – and only applicable to - linear systems, and a switching regulator is – by definition – a non-linear system. We solve this conundrum by performing our analysis using small-signal perturbations around a large-signal operating point, a distinction which will be further clarified in our design procedure discussion.

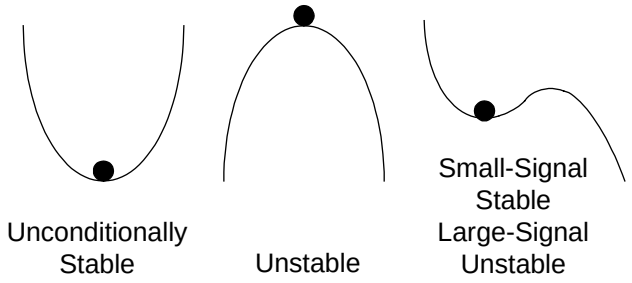


Fig. 2. Large-signal vs. small-signal stability.

III. Feedback Control Principles

The basic regulator is shown in Fig. 3 where an uncontrolled source of voltage (or current, or power) is applied to the input of our system with the expectation that the voltage (or current, or power) at the output will be very well controlled. The basis of our control is some form of reference, and any deviation between the output and the reference becomes an error. In a feedback-controlled system, negative feedback is used to reduce this error to an acceptable value – as close to zero as we want to spend the effort to achieve. Typically, however, we also want to reduce the error quickly, but inherent with feedback control is the tradeoff between system response and system stability. The more responsive the feedback network is, the greater becomes the risk of instability.

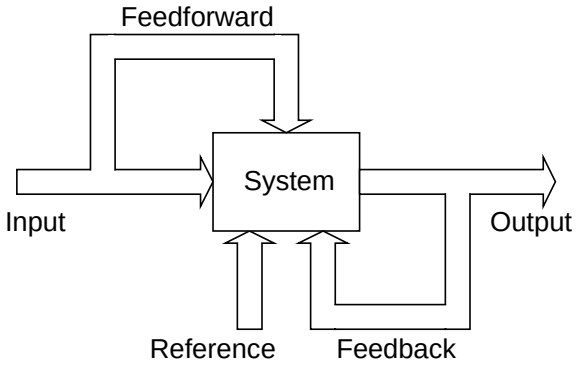


Fig. 3. The basic regulator.

At this point we should also mention that there is another method of control – feedforward. With feedforward control, a control signal is developed directly in response to an input variation or perturbation. Feedforward is less accurate than feedback since output sensing is not involved, however, there is no delay waiting for an output error signal to be developed, and feedforward control cannot cause instability. It should be clear that feedforward control will typically not be adequate as the only control method for a voltage regulator, but it is often used together with feedback to improve a regulator's response to dynamic input variations.

The basis for feedback control is illustrated with the flow diagram of Fig. 4 where the goal is for the output to follow the reference predictably and for the effects of external perturbations, such as input voltage variations, to be reduced to tolerable levels at the output.

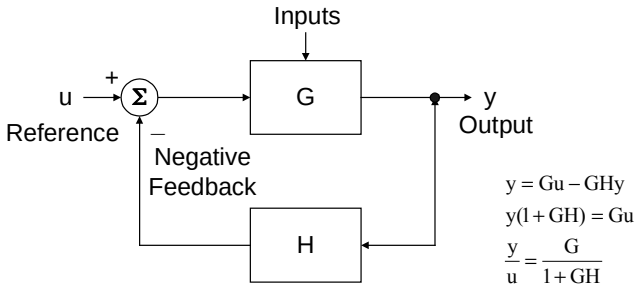


Fig. 4. Flow graph of feedback control.

Without feedback, the reference-to-output transfer function y/u is equal to G, and we can express the output as

$$y = Gu$$

With the addition of feedback (actually the subtraction of the feedback signal)

$$y = Gu - yHG$$

and the reference-to-output transfer function becomes

$$\frac{y}{u} = \frac{G}{1 + GH}$$

If we assume that $GH \rangle\rangle 1$, then the overall transfer function simplifies to

$$\frac{y}{u} = \frac{1}{H}$$

Not only is this result now independent of G, it is also independent of all the parameters of the system which might impact G (supply voltage, temperature, component tolerances, etc.) and is determined instead solely by the feedback network H (and, of course, by the reference). Note that the accuracy of H (usually resistor tolerances) and in the summing circuit (error amplifier offset voltage) will still contribute to an output error. In practice, the feedback control system, as modeled in Fig. 4, is designed so that $G \rangle\rangle H$ and $GH \rangle\rangle 1$ over as wide a frequency range as possible without incurring instability.

We can make a further refinement to our generalized power regulator with the block diagram shown in Fig. 5. Here we have separated the power system into two blocks – the power section and the control circuitry. The power section handles the load current and is typically large, heavy, and subject to wide temperature fluctuations. Its switching functions are by definition, large-signal phenomenon, normally simulated in most stability analyses as just a two-state switch with a duty cycle. The output filter is also considered as a part of the power section but can be considered as a linear block. The control circuitry will normally be made up of a gain block – the error amplifier – and the pulse-width modulator, used to define the duty cycle for the power switches.

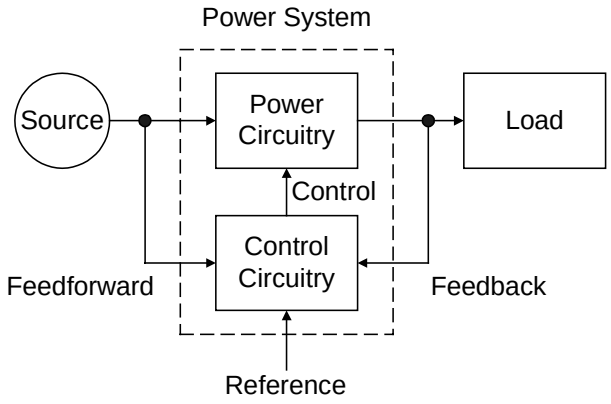


Fig. 5. The general power regulator.

IV. THE BUCK CONVERTER

The simplest form of the above general power regulator is the buck – or stepdown – topology whose power stage is shown in Fig. 6. In this configuration, a DC input voltage is switched at some repetitive rate as it is applied to an output filter. The filter averages the duty cycle modulation of the input voltage to establish an output DC voltage lower than the input value. The transfer function for this stage is defined by

$$V_O = \left(\frac{t_{ON}}{T}\right) \cdot V_i = V_i d, \text{ where :}$$

t_{ON} = switch on – time

T = repetitive period (1/fs)

d = duty cycle

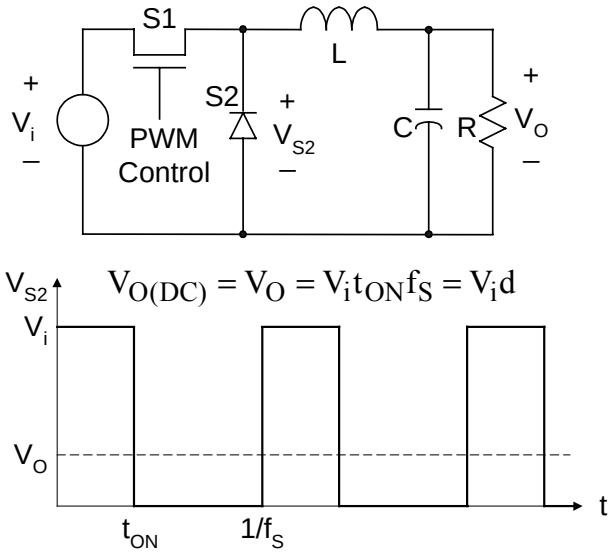


Fig. 6. The buck converter.

Since we assume that the switch and the filter components are lossless, the ideal efficiency of this conversion process is 100%, and regulation of the output voltage level is achieved by controlling the duty cycle. The waveforms of Fig. 6 assume a continuous conduction mode (CCM) meaning that current is always flowing through the inductor – from the switch when it is closed, and from the diode when the switch is open. The analysis presented in this topic will emphasize CCM operation because it is in this mode that small-signal stability is generally more difficult to achieve. In the discontinuous conduction mode (DCM), there is a third switch condition in which the inductor, switch, and diode currents are all

zero. Each switching period starts from the same state (with zero inductor current), thus effectively reducing the system order by one and making small-signal stable performance much easier to achieve. Although beyond the scope of this topic, there may be specialized instances where the large-signal stability of a DCM system is of greater concern than small-signal stability.

There are several forms of PWM control for the buck regulator including,

- Fixed frequency (f_S) with variable t_{ON} and variable t_{OFF}
- Fixed t_{ON} with variable t_{OFF} and variable f_S
- Fixed t_{OFF} with variable t_{ON} and variable f_S
- Hysteretic (or "bang-bang") with t_{ON}, t_{OFF}, and f_S all variable

Each of these forms have their own set of advantages and limitations and all have been successfully used, but since all switch mode regulators generate a switching frequency component and its associated harmonics as well as the intended DC output, electromagnetic interference and noise considerations have made fixed frequency operation by far the most popular.

With the exception of hysteretic, all other forms of PWM control have essentially the same small-signal behavior. Thus, without much loss in generality, fixed f_S will be the basis for our discussion of classical, small-signal stability.

Hysteretic control is fundamentally different in that the duty factor is not controlled, per se. Switch turn-off occurs when the output ripple voltage reaches an upper trip point and turn-on occurs at a lower threshold. By definition, this is a large-signal controller to which small-signal stability considerations do not apply. In a small-signal sense, it is already unstable and, in a mathematical sense, its fast response is due more to feedforward than feedback.

V. Controlling Pulse-Width Modulation

A typical implementation for PWM control (in a form which we now call "voltage-mode control") is illustrated in Fig. 7. From the block diagram it can be seen that the "width" of the PWM signal is determined by the point in time where the sawtooth, or ramp waveform (V_R) crosses the voltage level at the output of the error amplifier (V_E). Since V_R traverses from zero to V_P within a switching period, it follows that when V_E = zero, the width of the output pulse will be zero, and it will increase linearly reaching 100% when $V_E = V_P$. Therefore the duty cycle of the modulator will be V_E / V_P and since, in a buck converter, the duty cycle has already been determined to be V_O/V_i, the control gain of the modulator is:

$$\frac{V_O}{V_E} = \frac{V_i}{V_P}$$

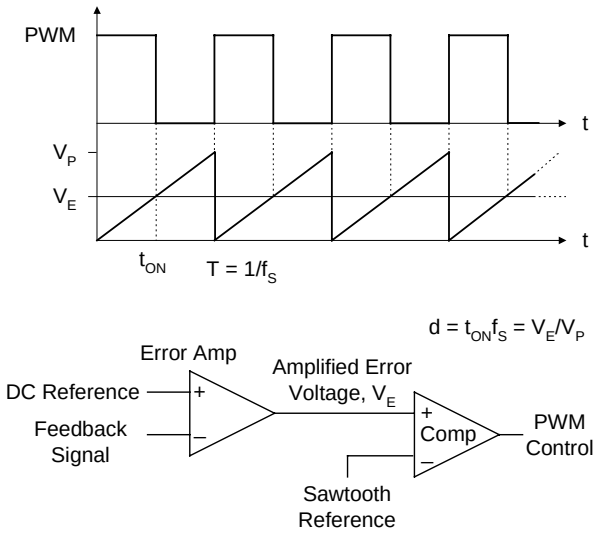


Fig. 7. Typical PWM control implementation.

Note that if V_P is made proportional to V_I, a feature which can be accomplished with feedforward, then the duty cycle will vary inversely proportional to the input voltage and input-to-output voltage regulation can ideally be achieved with no change in V_E.

In this analysis we have assumed complete linearity and that the output of the error amplifier, V_E, is a DC voltage. If, in addition to the intended DC component, V_E contains excessive "ripple", due to error amplifier gain at the switching frequency, then those switching frequency components can mix with the sawtooth frequency components causing the regulator to exhibit large-signal "switching instability", even if it has excellent small-signal stability. This type of instability can cause the regulator to produce even more ripple, usually at a subharmonic of the switching frequency, although it may still regulate at the proper output voltage.

VI. Characteristics of a Loaded L-C Filter

The schematic of Fig. 8 shows an L-C filter with a load, R, where the components have been converted to impedances in the frequency domain through the use of Laplace transforms. The overall transfer function of this network is described by the use of Kirchhoff's law as

$$\frac{V_O(s)}{V_i(s)} = \frac{R \left\| \frac{1}{Cs} \right.}{R \left\| \left(\frac{1}{Cs + Ls} \right) \right.} = \frac{\frac{1}{LC}}{s^2 + \frac{s}{RC} + \frac{1}{LC}}$$

$$= \frac{\frac{1}{LC}}{(s - p_1)(s - p_2)}$$

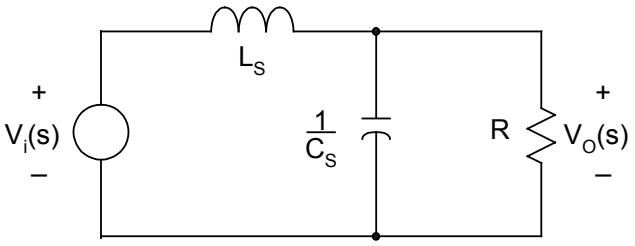


Fig. 8. Frequency response of a loaded LC filter.

By setting the transfer function numerator and denominator each equal to zero, we can derive the roots of both the numerator, which are the zeros of the system (none in this equation), and the denominator which gives us the poles. This second-order expression contains two poles, $p_1 = -\alpha + j\omega_d$ and $p_2 = -\alpha - j\omega_d$ where:

$$\alpha = \frac{1}{2RC}, \quad \omega_d = \sqrt{\frac{1}{LC} - \alpha^2}, \text{ and } j = \sqrt{-1}$$

For lightly damped filters (typical of switching regulators), we can often use the approximation of:

$$\omega_d \approx \omega = \sqrt{\frac{1}{LC}}$$

With $s = j\omega$, we see that transfer functions are complex numbers containing a real part and an imaginary part. The amplitude of a complex number is the square root of the sum of the squares of the real and imaginary parts. The phase is the inverse tangent (arctan) of the ratio of the imaginary part to the real part. By evaluating the transfer functions as a function of frequency, we can determine the point where both the magnitude and the phase make transitions. The most common way of doing this is to plot the gain in dB (20 times the log of gain), and the phase in degrees, against the log of frequency. These are called Bode plots and allow easy visualization of the characteristics that we will use to help define system stability. From the transfer function equations for Fig. 8, we can determine that:

- The gain = 1 and the phase = 0 for $\omega \ll \sqrt{\frac{1}{LC}}$.
- The gain = $R\sqrt{\frac{C}{L}}$ and the phase = 90° for $\omega = \sqrt{\frac{1}{LC}}$.
- The gain slope = $\frac{-1}{\omega^2 LC}$ and the phase = 180° for $\omega \gg \sqrt{\frac{1}{LC}}$.

For this example of a loaded L-C filter, Mathcad was used to draw the plots shown in Fig. 9, with the assumption of an arbitrarily assigned set of numerical values (which we will later use for our buck converter example):

$L = 16\ \mu H$, $C = 540\ \mu F$, and $R = 0.5\ \Omega$

from which $\alpha = 1.85 \cdot 10^3$ and $\omega = 1.06 \cdot 10^4$.

From Fig. 9 we substantiate that the gain of this filter is unity at low frequencies, experiences a resonant peak (determined by R) at the second-order pole frequency, and then falls with a slope of 12 dB/octive (20 dB/decade) at higher frequencies; while the phase goes through a shift from zero to a 180^{o} lag. This higher frequency slope is sometimes called a –2 slope since, in this region, the function is proportional to $1/\omega^2$, or ω^{-2}.

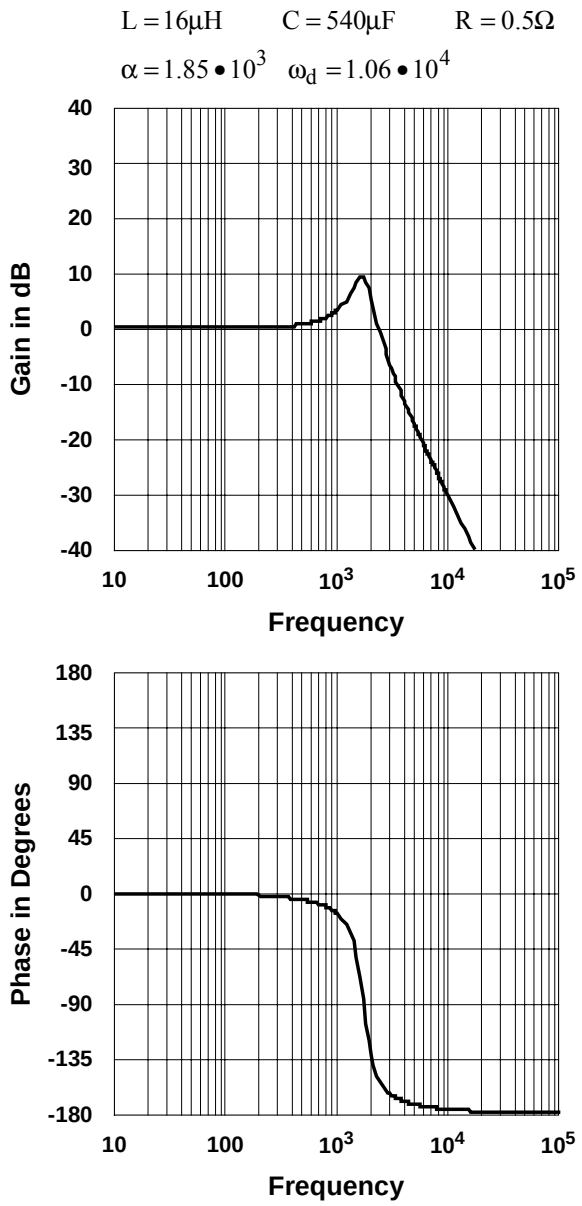


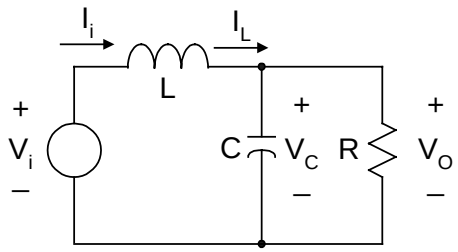
Fig. 9. Bode plot of a sample loaded LC filter.

It is worth reinforcing that a system must be linear before frequency-domain techniques, such as Laplace transforms and Bode plots, apply. A switching regulator is not even continuous, let alone linear. Therefore, approximations will have to be made – first, to average the switching effects so that we have a continuous system, and secondly, to apply a small-signal approximation in order to assume linearity. And, of course, all this is done under the additional assumptions of linear passive components and ideal switches.

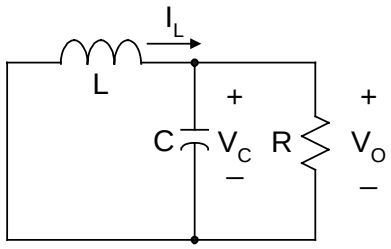
VII. Linearizing the Buck Converter

With ideal components, a switching regulator is a linear circuit for any given switch condition. The concept of averaging can be applied when the switching rate is fast with respect to the rate of change of any other parameters of interest. To quantify this, we can say that the accuracy of the approximations is excellent up to one-tenth the switching frequency, "pretty good" for one-third, and one-half is the theoretical limit based on the Nyquist sampling criterion.

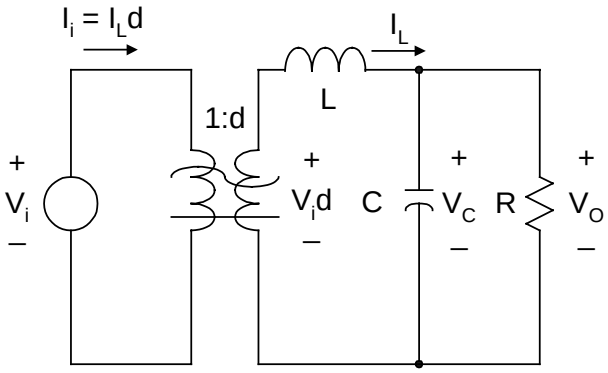
Fig. 10 shows the process of averaging the operation of the circuit by combining the condition when the active switch is closed with that when it is open. The relationship between these two conditions is the duty cycle of the switching and its effect is accounted for through the use of a hypothetical DC transformer with a turns ratio of the duty cycle, d. With this model, the primary current is now $I_L d$ and the secondary voltage is $V_i d$. This DC transformer is an artifact from Dave Middlebrook at Caltech. It is not a real component but it is valid for your Spice library. We now have a continuous system but it is nonlinear because the transformer turns-ratio, d, is a variable - namely the control variable - and not a constant.



Switch Condition I [d th of the time]



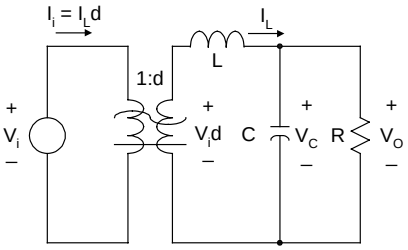
Switch Condition II [(1-d)th of the time]



Circuit Model Using DC Transformer Concept.
$I_L d$ and $V_i d$ are nonlinear terms.

Fig. 10. Averaged buck converter.

With an averaged, continuous model, the next step is to linearize it. We do this exactly the same way we would linearize any nonlinear, continuous system, namely we define the small-signal parameters based on a large-signal operating point. This is shown in Fig. 11. Mathematically, the linearization process involves separating each variable into its DC (in capitals) and signal frequency ac (with a "hat") components, and neglecting the products of two hat terms. For the example calculation shown in Fig. 11, the product $V_i d$ is linearized about the operating point, $V_i D$.



$v_i = V_i + \hat{v}_i \quad i_L = I_L + \hat{i}_L \quad d = D + \hat{d}$ Neglect "hat" products

For example, $v_i d \approx (V_i + \hat{v}_i)(D + \hat{d}) = v_i d + V_i \hat{d}$ where $\hat{V}_i \hat{d} \approx 0$

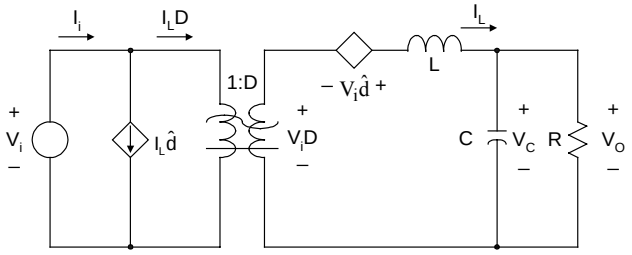


Fig. 11. Linearized buck converter.

The advantage of linearization is that Laplace transforms (i.e. impedance concepts) apply so that closed-form algebraic solutions can be found and plotted (e.g. Bode plots). The range over which the linear approximations are valid depends upon the accuracy desired. In general, as long as the signals are small enough so that the duty factor is not clamped either full on or full off for several switching cycles, the linear approximation works very well. And in any case, small-signal stability as evidenced using Bode plots is still a necessary condition for overall stability.

VIII. Applying the Linearized Model

The flow diagram of the closed-loop linearized buck regulator can be derived by applying the generalized control law to the linearized power circuit described above, as shown in Fig. 12. This control law determines how d(s), the Laplace transformed control variable, varies as a function of key circuit parameters. For a second-order system, such as the buck regulator with one input voltage, it can be expressed as:

$$d(s) = -F_1(s)\hat{I}_L(s) - F_2(s)\hat{V}_C(s) + Q_1(s)\hat{V}_i(s)$$

That is, the inductor current variable, the output voltage variable, and the input voltage variable, can each individually contribute to the system control variable. As it pertains to switching regulators, the expression "voltage-mode control" implies that there is no current feedback, i.e. $F_1(s) = 0$. "Current-mode control" means that there is a current loop as well as a voltage loop. In either case, there may or may not be feedforward control, $Q_1(s)$. And finally, note that in this case, $F_2(s)$ includes the reference and feedback summing components.

This generalized control law can then be made specific to our voltage-mode controlled, buck regulator as shown in Fig. 13, where the feedback summing point is the differential input to the Error Amplifier.

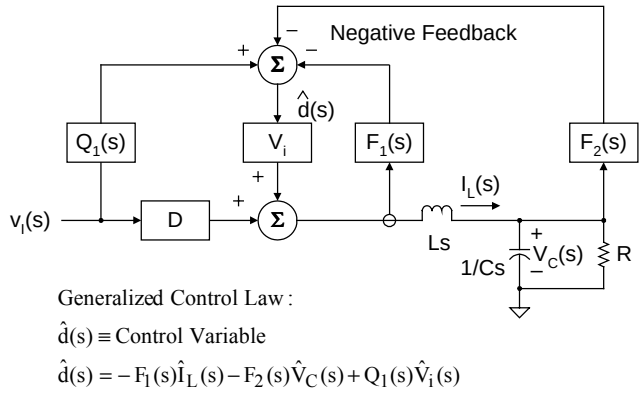


Fig. 12. Flow graph / schematic of linearized buck converter with general control law.

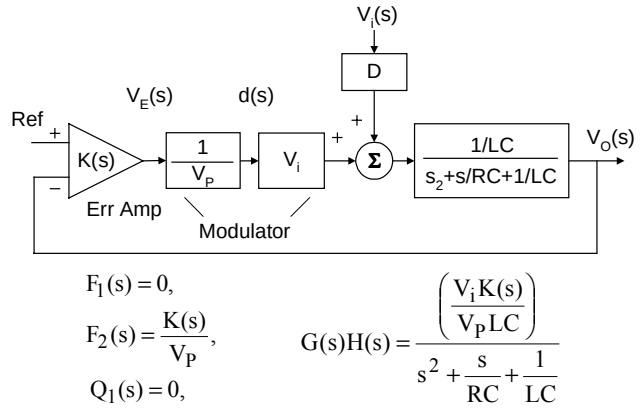


Fig. 13. Flow graph of linearized buck converter with voltage-mode control.

The overall open-loop gain is equal to the product of the individual gains of the error amplifier, the modulator, and the output filter, and is shown as:

$$G(s)H(s) = \frac{\frac{V_i K(s)}{V_P LC}}{s^2 + \frac{s}{RC} + \frac{1}{LC}}$$

There are several points which could be made relative to the above equation: First, note that this expression is independent of the DC duty factor D but is dependent upon the DC input voltage V_i. Hence, as would be expected, the open-loop gain function is dependent upon the DC operating point. Secondly, the second term in the denominator contains the load resistance, R. If R were to go to infinity, this term would go to zero indicating an unstable system, however, the reality is that the circuit would first go to DCM where its small-signal operation becomes essentially first order. Finally, the expression above also assumes that the output voltage level is equal to the reference (H = 1). If this is not the case, the appropriate scale factor would be added to either the reference or the output voltage prior to the error amplifier input.

Note that we have assumed that G(s)H(s) is positive in this expression. This is just a simplification in that we are assuming negative feedback, so the first 180^o is implicit and instability will occur at 180^o rather than the 360^o which some control theory texts describe.

With Mathcad as a simulation tool, and utilizing the parameters of our earlier example, the above general transfer equation can be solved as a function of frequency to yield the Bode plots shown in Fig. 14.

This example again uses:

$L = 16\ \mu H, \quad C = 540\ \mu F, \quad R = 0.5\ \Omega$

and additionally,

$V_i = 12\ V, \quad V_O = 5\ V, \quad V_P = 2\ V$

$f_s = 100\ kHz, \quad K = 5.6,$ and

$s = j2\pi f$

I $\left|G(f)H(f)\right| \approx \frac{V_i K}{V_P}$

II $\left|G(f)H(f)\right| \approx \frac{V_i}{(2\pi f)^2 V_P LC}$

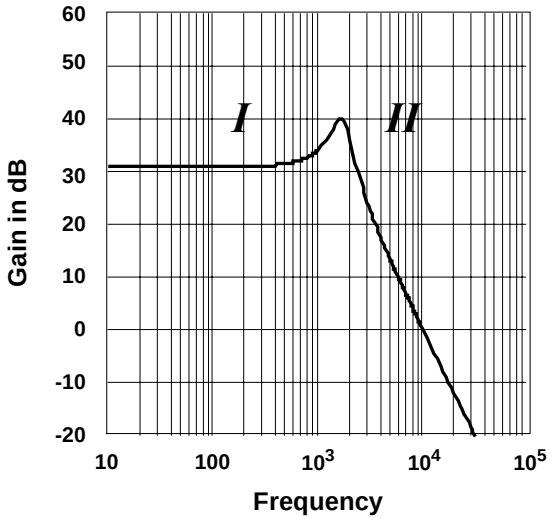
$S = j2\pi f$

$V_i = 12V \quad V_O = 5V$

$R = 0.5\Omega \quad V_P = 2V$

$f_S = 100kHz \quad Ripple < 50mVp-p$

$L = 16\mu H \quad C = 540\mu F$



$Peak = \frac{V_i K}{V_P} \bullet R\sqrt{\frac{C}{L}} = 40dB \text{ at } 1.71kHz$

for $K = 5.6$

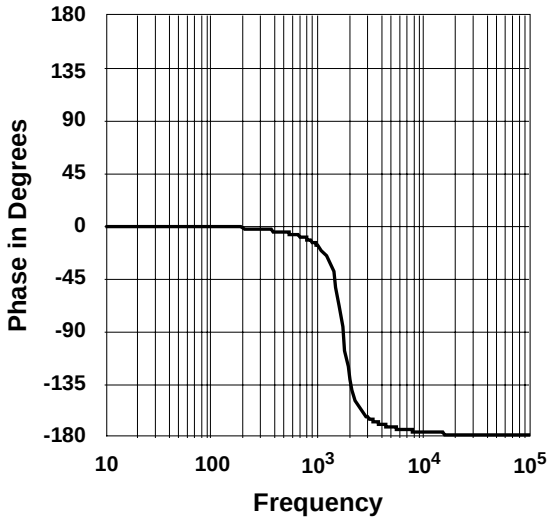


Fig. 14. Bode plot of a 100 W, 12 V-to-5 V, buck converter open loop gain with DC error amp gain [K(s) = K].

From these values, the Bode plots give us the gain and the phase of the open-loop transfer function from which we can see that at low frequencies,

$$\left|G(f)H(f)\right| \approx \frac{V_i K}{V_P} = 30 \text{ dB}$$

and at the higher frequencies,

$$\left|G(f)H(f)\right| \approx \frac{V_i}{(2\pi f)^2 V_P LC}$$

$\Rightarrow$ a negative slope of 12 dB/octave

The peak gain at resonance is:

$$\left|G(f)H(f)\right| \approx \frac{V_i K}{V_P} \cdot R\sqrt{\frac{C}{L}} \approx 40 \text{ dB at } 1.71 \text{ kHz}$$

At this point we should define some terms important to our stability analysis:

A. Gain Margin

The difference between unity gain (zero dB) and the actual gain when the phase reaches 180^o. (In this case it is a positive number.) The recommended value is -6 dB to –12 dB.

B. Phase Margin

The difference between 180^o and the actual phase when the gain reaches unity gain. (In this case it is approaching zero.) The recommended value is 45^o to 60^o.

C. Stability Criteria

A commonly used derivative from the above two definitions is that if the slope of the gain response as it crosses the unity-gain axis is not more than -6 dB / octave, the phase margin will be greater than 45^o and the system will be stable.

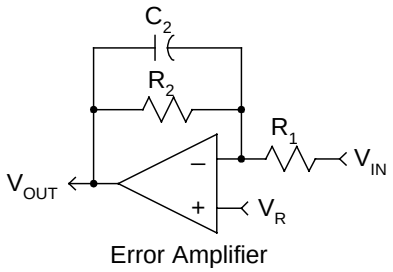
These simulations have made no approximations other than those required for linearizing the system. It should be understood, however, that phase shift is caused not only by reactive components but also by time delay, such as transistor storage time or hold time in a sampling system. Switch delays normally have little effect as long as there is no explicit sample-and-hold function, and the frequencies of interest are well below the switching frequency. For example, the effect of a 1 μs delay in a 100 kHz system is a phase shift of less than 4^o. There will also be potential phase lags due to the op amp and parasitic components. Thus, although technically a second-order system could potentially be stable since 180^o phase lag is only asymptotically approached, we can expect that this system, as currently defined, will be unstable in practice and, in any case, would suffer serious ringing under any external disturbance. In fact, the plots of Fig. 14 show a system with essentially negative gain margin and zero phase margin. We had assumed a value for the amplifier gain of 5.6 only because we will use this value later, but even if it were unity, the gain of the modulator alone could be enough for instability since we already have 180^o phase shift just from the output filter.

IX. Frequency Compensation

Recognizing that we have thus far defined what amounts to an unstable system, we will now consider techniques to shape the open-loop gain function to provide adequate gain and phase margins. Our first approach will be to reduce the gain at a lower frequency such that the unity-gain point will be reached with positive phase margin. This is done by rolling off the gain of the error amplifier with local feedback as shown in Fig. 15. With the addition of C_2 (R_1 and R_2 are what gave us the amplifier gain of 5.6), we now have an amplifier gain of:

$$K(s) = \frac{-V_{OUT}(s)}{V_{IN}(s)} = \frac{R_2}{R_1(1+R_2C_2s)}$$

This amounts to our original DC gain with an added pole at $\omega_p = \frac{1}{R_2C_2}$.



$$K(s) = \frac{-V_{OUT}(s)}{V_{IN}(s)} = \frac{R_2}{R_1(1+R_2C_2s)}$$

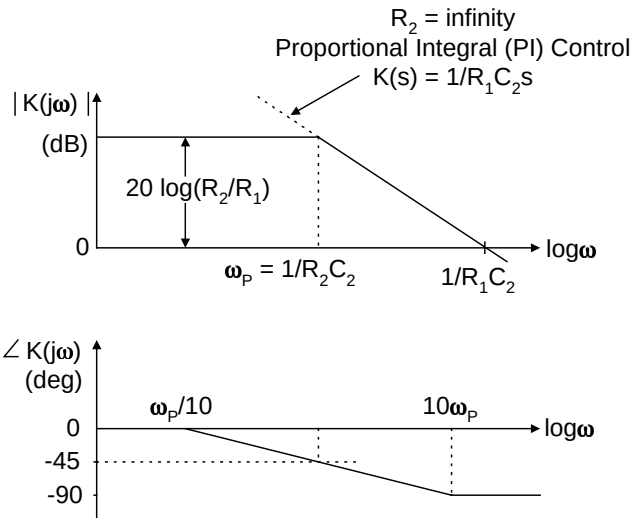


Fig. 15. Lag compensation.

This single-pole compensation is called lag compensation and from the asymptotic approximated plots above, the phase shift changes from zero at 1/10 the corner frequency to 90^o at 10 times the corner frequency. Right at the corner frequency, the phase is 45^o since the denominator is 1 + j , where the real and imaginary parts are equal. Since the amplitude of 1 + j is $\sqrt{2}$, the actual gain amplitude at the corner frequency is reduced by 3 dB (commonly called the half-power point).

Remember: The product/division of two complex numbers is equal to the sum/difference of their amplitudes in dB and the sum/difference of their phase angles.

The amplitude of the compensated error amplifier gain in dB adds directly to the amplitude of the other elements in the control loop, as the amplifier's phase adds to the overall phase lag.

The Bode plots for lag compensation (implemented in this form as a proportional integrator without R_2) are shown in Fig. 16. The asymptotic transfer function equations now become:

At low frequencies,

$$\left|G(f)H(f)\right| \approx \frac{V_I}{2\pi\, fV_P R_1 C_2}$$

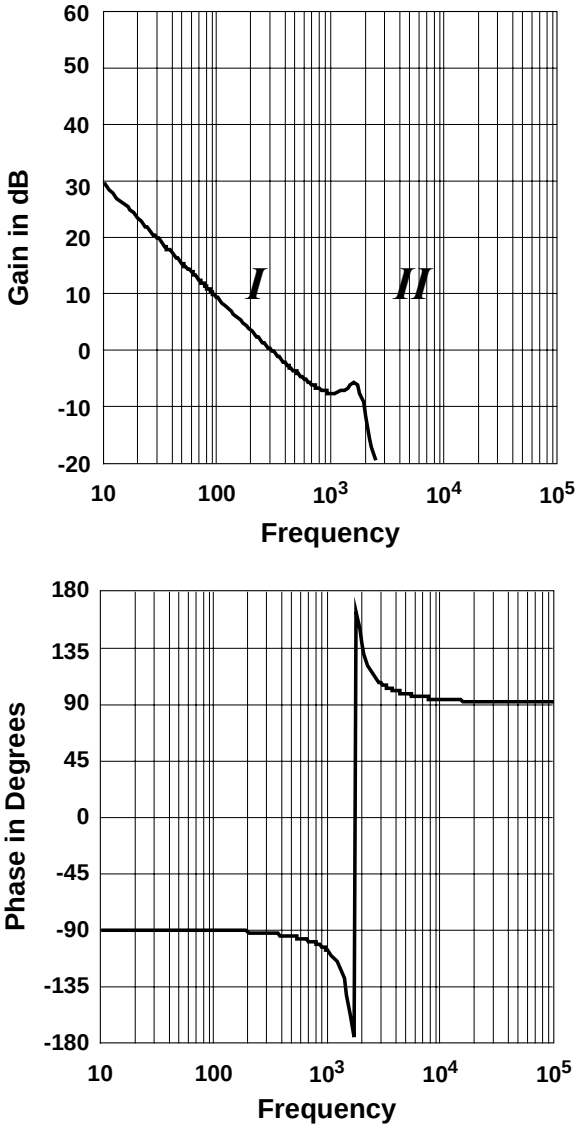
At high frequencies,

$$\left|G(f)H(f)\right| \approx \frac{V_I}{(2\pi\, f)^3 V_P R_1 C_2 LC}$$

$s = j2\pi\, f$

$$\text{The resonant peak} = \frac{V_I}{2\pi\, fV_P R_1 C_2} \cdot R\sqrt{\frac{C}{L}}$$

For a 6 dB gain margin at f = 1.71 kHz, we set the peak gain equal to ½ which yields an R_1C_2 product equal to 299. From this we have set R_1 = 167 kΩ and C_2 = 0.02 µF. Note that the gain-bandwidth (the unity gain crossover frequency) is now less than 300 Hz, an order of magnitude below the resonant frequency. Another point of interest is that the gain margin of 6 dB was based on the resonant peak, which in turn is dependent upon the output loading, R, meaning that decreasing the regulator's load could also decrease the gain margin. In practice, one would use the smallest load (largest R) for which the converter is still in CCM. While the phase margin is now 90°, the dominant pole has reduced the bandwidth to the point where dynamic response will be very poor. (Note that in the complex plane, +90° is the same as –270°. The lag compensator contributes –90° from the DC value, and above resonance, the LC output filter contributes another –180°.)



$$\text{Peak} = \frac{V_i}{2\pi f V_P R_1 C_2} \cdot R\sqrt{\frac{C}{L}}$$

$$\text{for 6 dB gain margin at } f = 1.71\,\text{kHz},$$

$$\frac{V_i}{2\pi f V_P R_1 C_2} \cdot R\sqrt{\frac{C}{L}} = \frac{1}{2} \Rightarrow R_1 C_2 = 299$$

$$\text{Sample values: } R_1 = 167\,\text{k}\Omega,\ C_2 = 0.02\,\mu\text{F}$$

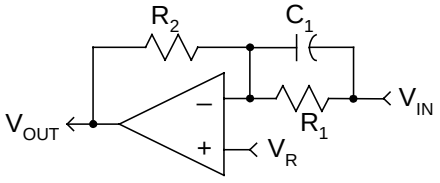
Fig. 16. Bode plot of lag-compensated sample buck converter open-loop gain function.

A second alternative is lead compensation which is described in Fig. 17. Here, instead of decreasing the gain we will increase the phase by adding a lead capacitor, C_1, to the error amplifier, introducing a network zero (the opposite of a pole). Of course, this also increases the gain but if we make the break frequency of this zero, ω_Z, the same as the unity gain frequency of the uncompensated buck regulator, we have provided a phase margin of 45°.

The gain equation for the error amplifier with lead compensation is:

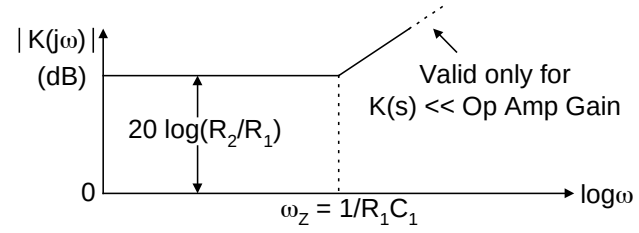
$$K(s) = \frac{-V_{OUT}(s)}{V_{IN}(s)} = \frac{R_2(1+R_1C_1s)}{R_1}$$

This amounts to the original DC gain with an added zero at $\omega_Z = \frac{1}{R_1C_1}$



Error Amplifier

$$K(s) = \frac{-V_{OUT}(s)}{V_{IN}(s)} = \frac{R_2(1+R_1C_1s)}{R_1}$$



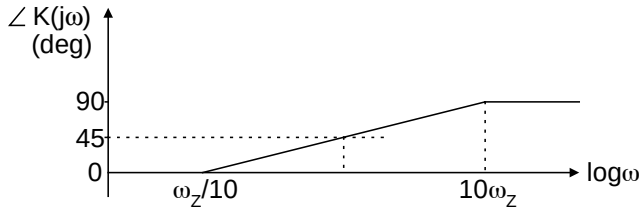


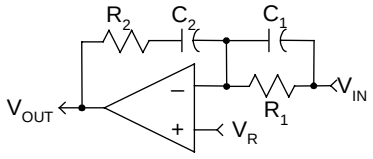
Fig. 17. Lead compensation.

In practice, pure lead compensation is physically unrealizable since the gain cannot continue to rise indefinitely due to limitations in the open loop gain-bandwidth of the amplifier. Naturally, the gain-bandwidth of the operational amplifier used with lead compensation must be much higher than that required for lag compensation.

It should be noted that the error amplifier is not the only place in a switching regulator to experience a compensating zero. The parasitic equivalent series resistance (ESR) inherent in non-ideal capacitors selected for use as an output filter will react with the output capacitance value to introduce a circuit zero to the system. Many designers have relied on this as a "free" (but also relatively uncontrolled) method for achieving some added positive phase margin. (Try to get your favorite capacitor supplier to guarantee a minimum ESR!)

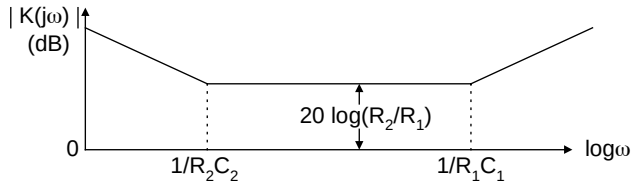
The circuit of Fig. 18 combines both a lead and a lag in an attempt to gain the best features of both – namely low DC error as well as higher bandwidth. In this circuit, a zero capacitor is placed in parallel with the input resistor while a pole capacitor is added in series with the feedback resistor. The intent here is to provide a high gain at low frequencies while still achieving acceptable phase margin at crossover. The gain equation for the error amplifier now becomes:

$$K(s) = \frac{-V_{OUT}(s)}{V_{IN}(s)} = \frac{(1+R_2C_2s)(1+R_1C_1s)}{R_1C_2s}$$



Error Amplifier

$$K(s) = \frac{-V_{OUT}(s)}{V_{IN}(s)} = \frac{(1+R_2C_2s)(1+R_1C_1s)}{R_1C_2s}$$



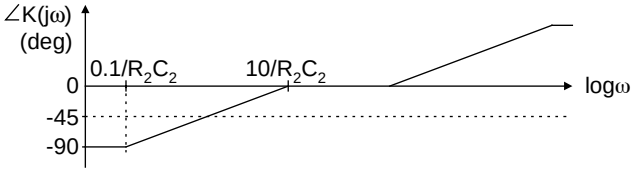


Fig. 18. Achieving "zero" DC error.

The phase lead associated with R_2C_2 cannot completely cancel out the initial 90° phase lag caused by the integrating capacitor until the frequency $\frac{10}{R_2C_2}$ is reached. Therefore, in order to ensure that the phase margin due to the zero associated with R_1C_1 is not degraded, $\frac{1}{R_2C_2}$ must be at least an order of magnitude below the resonant frequency of the system. That is, the phase shift due to the zero caused by R_2C_2 should be "over" before any other phase shift in the system "starts" so that the system is otherwise transparent to the effects of integrating out the DC error.

X. Large-Signal Considerations

We have made several references to the fact that while small-signal stability is a necessary requirement for a stable regulator, large-signal effects cannot be ignored. To illustrate the potential for a large-signal problem, Fig. 19 demonstrates how the amplified output ripple waveform can interfere with the PWM operation. For simplicity, this illustration assumes a constant error amplifier gain. Although this is not very realistic, since we have already demonstrated that a buck converter with constant feedback gain is likely to be small-signal unstable, it will still serve to demonstrate the concept that there is a limit to the amount of gain that the system can have at the switching frequency. Beyond this limit, the system will exhibit large-signal instability, regardless of the margins shown in the Bode plot.

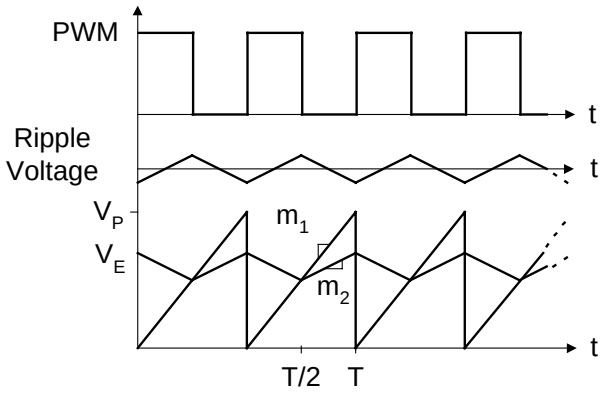


Fig. 19. Large-signal stability considerations for voltage-mode control.

In this example, the output ripple voltage (assumed as being largely caused by the output capacitor ESR) is amplified by the error amplifier gain to appear in inverted form as V_E, the voltage which is compared in the PWM modulator to the ramp waveform. A necessary condition for large-signal stability is that the slope of V_E, designated m_2, must be less that the slope of the ramp, m_1. A sample problem can demonstrate the impact of this requirement. If we assume that the duty cycle D = 0.5, output ripple = 0.05 volts p-to-p, and V_P = 2 volts, then:

$$m_1 = \frac{2}{T} \text{ and } m_2 = \frac{0.05\ K}{T/2} = \frac{0.1\ K}{T}$$

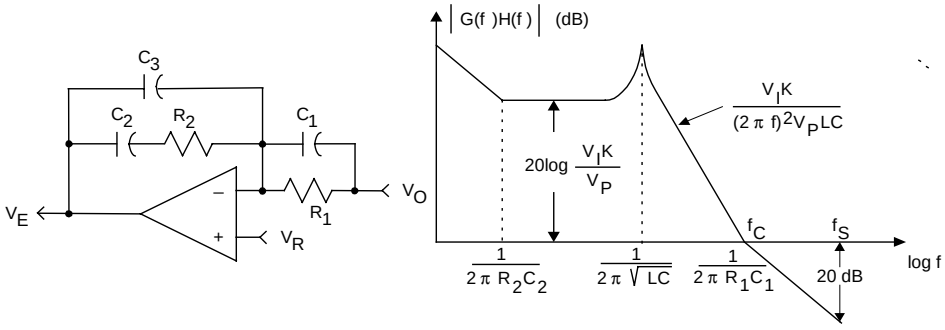
Therefore, K must be less than 20.

In reality, the problem can be more severe if there is an unbounded lead network which would then act as a differentiator at the switching frequency such that the output from the error amplifier might approximate a square wave more than a triangular shape shown in this illustration. While there is no widely accepted design criterion to define a solution, an empirical rule of thumb is to insure that that the total system gain is –20 dB or below at the switching frequency. In any case, this issue is highly application specific and designers should make this determination for each individual system in the course of their evaluation.

XI. DESIGN PROCEDURE

To summarize the design procedure for the lead-compensated, voltage-mode, buck regulator, the step-by-step approach is demonstrated in the accompanying box.

Design Procedure for Lead-Compensated Voltage-Mode Controlled Buck Converter



Step 1: Choose gain - bandwidth $f_C = \frac{f_S}{10}$ for large - signal stability (20 dB attenuation at f_S).

Step 2: Choose zero frequency $\frac{1}{2\pi R_1 C_1} = f_C$ for 45° phase margin.

Step 3: Choose $\frac{R_2}{R_1} = K = \frac{(2\pi f_C)^2 V_P LC}{V_i}$ for unity gain at $f = f_C$.

Step 4: Choose $\frac{1}{R_2 C_2} = 0.1\sqrt{\frac{1}{LC}}$ for increased low - frequency gain and "zero" dc error.

Step 5: Choose $R_2 C_3 = ESR \cdot C$ to cancel lead effect of ESR.

For EXAMPLE, Using the Following Parameter Values:

$V_i = 12$ V $V_O = 5$ V $f_S = 100$ kHz $L = 16\,\mu$H $C = 540\,\mu$F $R = 0.5\,\Omega$ $V_P = 2$V

Step 1: $f_C = \frac{10^5}{10} = 10$ kHz

Step 2: $R_1 C_1 = \frac{1}{2\pi f_C} = 1.59 \cdot 10^{-5}$ $R_1 <<$ input Z of op amp. $R_1 = 10.5$ kΩ, $C_1 = 1500$ pF

Step 3: $R_2 = \frac{(2\pi f_C)^2 V_P LCR_1}{V_i} = 59$ kΩ $K = \frac{R_2}{R_1} = 5.6$

Step 4: $\omega_n = \sqrt{\frac{1}{LC}} = 10{,}758$ $C_2 > \frac{10}{\omega_n R_2} = 1.58 \cdot 10^{-8} \Rightarrow .02\,\mu$F

Step 5: From data sheet, ESR = .022 Ω. $C_3 = \frac{ESR \cdot C}{R_2} = 200$ pF

In this example, we have added C_3 for a high-frequency roll-off, chosen so that the pole frequency, $\frac{1}{R_2C_3}$, cancels the zero frequency at $\frac{1}{(ESR)C}$. This reduction in nominal gain-bandwidth is required to ensure both small-signal stability - with 45° phase margin – and at least 20 dB rejection at the switching frequency in applications where the ESR can vary widely. Our example uses three paralleled 180 μF solid tantalum capacitors where the total capacitance is 3X and the ESR is 1/3 of a single unit. Note that the value of K is much less than the maximum of 20 calculated for large-signal stability.

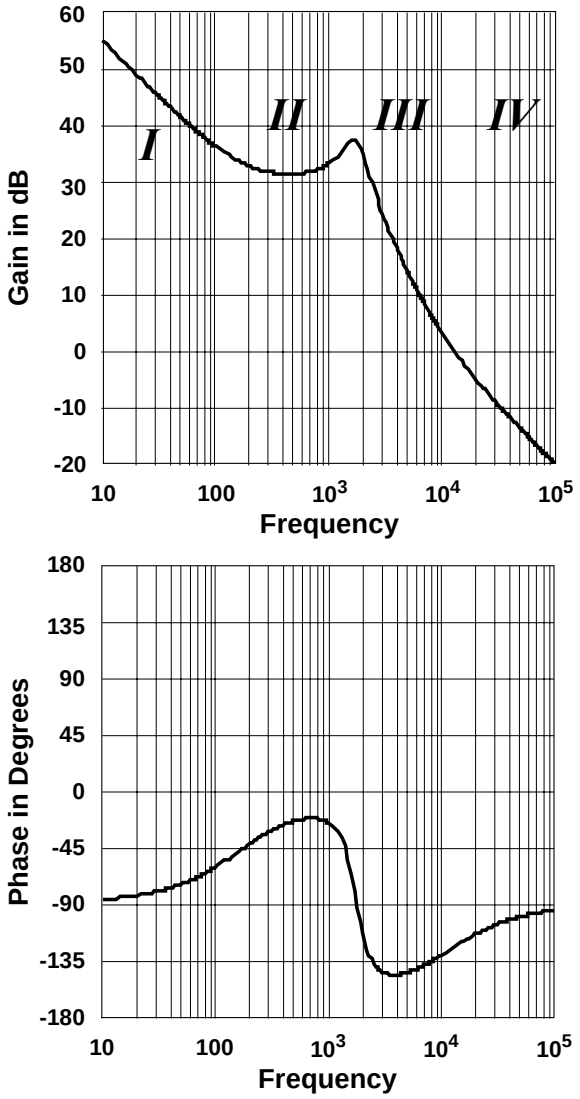
The calculated Bode plots for this example are shown in Fig. 20 from which we can see that the gain bandwidth of this lead-compensated circuit is nearly an order of magnitude greater that the resonant frequency of the uncompensated system. This is particularly significant in remembering that the lag-compensated solution required a gain-bandwidth an order of magnitude lower than resonance. The approximate equations which are active in defining the gain within the various regions of operating frequency are given below:

$$\text{I } \left|G(f)H(f)\right| \approx \frac{V_i}{2\pi f\ V_P R_1 C_2}$$

$$\text{II } \left|G(f)H(f)\right| \approx \frac{V_i R_2}{V_P R_1}$$

$$\text{III } \left|G(f)H(f)\right| \approx \frac{V_i R_2}{(2\pi f)^2\ V_P R_1 LC}$$

$$\text{IV } \left|G(f)H(f)\right| \approx \frac{V_i R_2 C_1}{2\pi f\ V_P LC}$$



The phase margin is greater than 45° for :

$R_1 = 10.5\ k\Omega$

$R_2 = 59\ k\Omega$

$C_1 = 1500\ pF$

$C_2 = 0.02\ \mu F$

The gain – bandwidth is greater than 10 kHz.

Fig. 20. Bode plot of lead-compensated sample buck converter open-loop gain function with "zero" DC error.

The final value for gain-bandwidth is 12.7 kHz while the phase margin is nearly 55°. The gain margin is well over -20 dB and any higher frequency phase lag (as, for example, operational amplifier limitations) would cause the gain to be further reduced.

We can use Mathcad to plot other characteristics of our demonstration example as shown in Fig. 21. These plots show output impedance (a measure of load regulation) and audiosusceptibility (line regulation) as a function of frequency. The benefits of feedback to dynamic performance are graphically illustrated by the comparative curves in these plots.

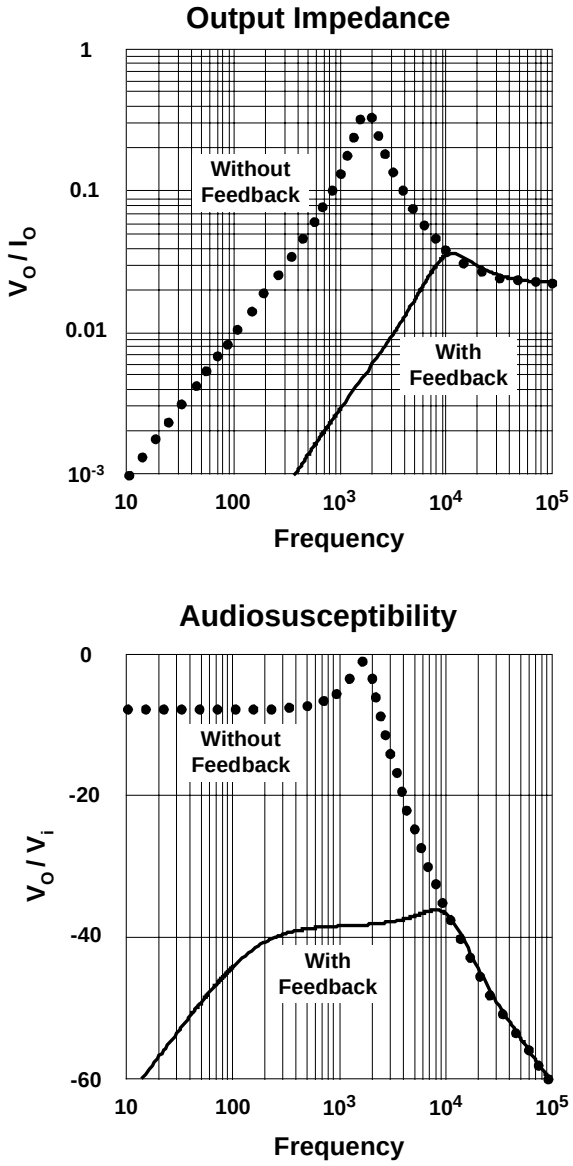


Fig. 21. Output impedance and audiosusceptibility for the lead-compensated sample buck converter.

XII. PEAK CURRENT-MODE CONTROL

The voltage-mode algorithm which we have been using as a model for the preceding analysis achieves its PWM control by comparing the error amplifier command signal with an artificially-generated sawtooth, or ramp waveform. With peak current-mode (C/M) control, this comparison ramp is derived from the output inductor current waveform and thus forms an inner current feedback loop. While there is still an outer voltage loop, its function is to program the output inductor current rather than the duty cycle directly. With the open loop characteristics of a programmable current source, current-mode control effectively hides the inductor within the inner loop, changing the resonant two-pole output filter to a single lower frequency dominant pole, plus a higher frequency pole at or beyond the gain-bandwidth of the system. In so doing, the task of compensation is significantly eased. A simplified block diagram of this topology is shown in Fig. 22 and its operation is described as follows:

A fixed-frequency oscillator initially sets the latch which turns on the power switch, causing inductor current to rise according to:

$$\frac{di}{dt} = \frac{(V_i - V_o)}{L}.$$

This current is sensed and converted to a voltage ramp which is compared to the error signal from the voltage error amplifier.

When the current ramp crosses the error signal, the comparator resets the latch turning off the power switch, allowing the inductor current to decay according to $\frac{di}{dt} = -\frac{V_o}{L}$. While both DCM and CCM operation are possible, this example assumes CCM.

The power switch is held off by the latch until the clock initiates the next cycle.

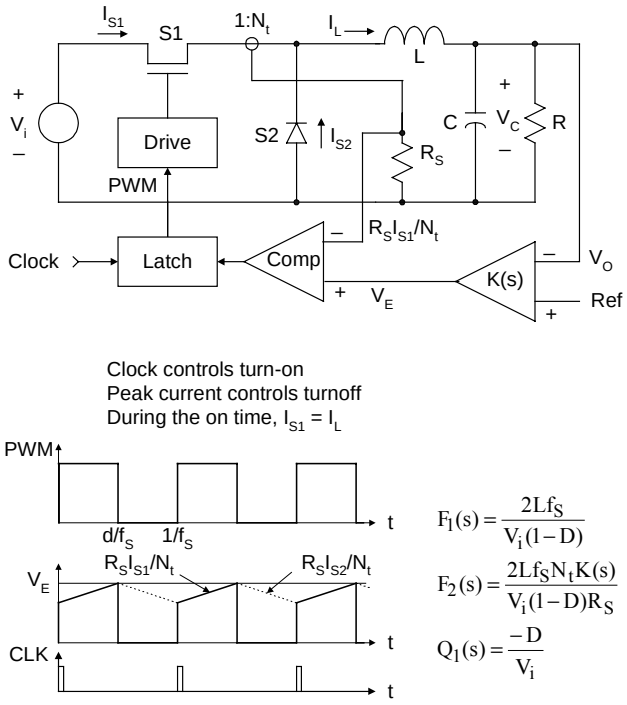


Fig. 22. Peak current-mode control implementation for buck converter.

Current sensing can be accomplished with either a sensing resistor or a current sense transformer (as used in this example) but, in either case, a proportionate voltage waveform is derived for the comparator. One problem with current-mode control is that this waveform often also contains leading-edge noise spikes caused by parasitic capacitance and diode recovery. These spikes need to be controlled by either blanking or filtering or else the comparator may reset the latch right at the beginning of the power pulse.

Note that this example actually measures switch current rather than inductor current since the only information needed for control is the peak value of the inductor current and this is usually more conveniently done in series with the power switch. What happens to the inductor current after the switch opens is, in principle, unimportant.

However, in CCM applications where the duty cycle may extend beyond 50%, a large-signal, sub-harmonic instability can occur which is described in Fig. 23.

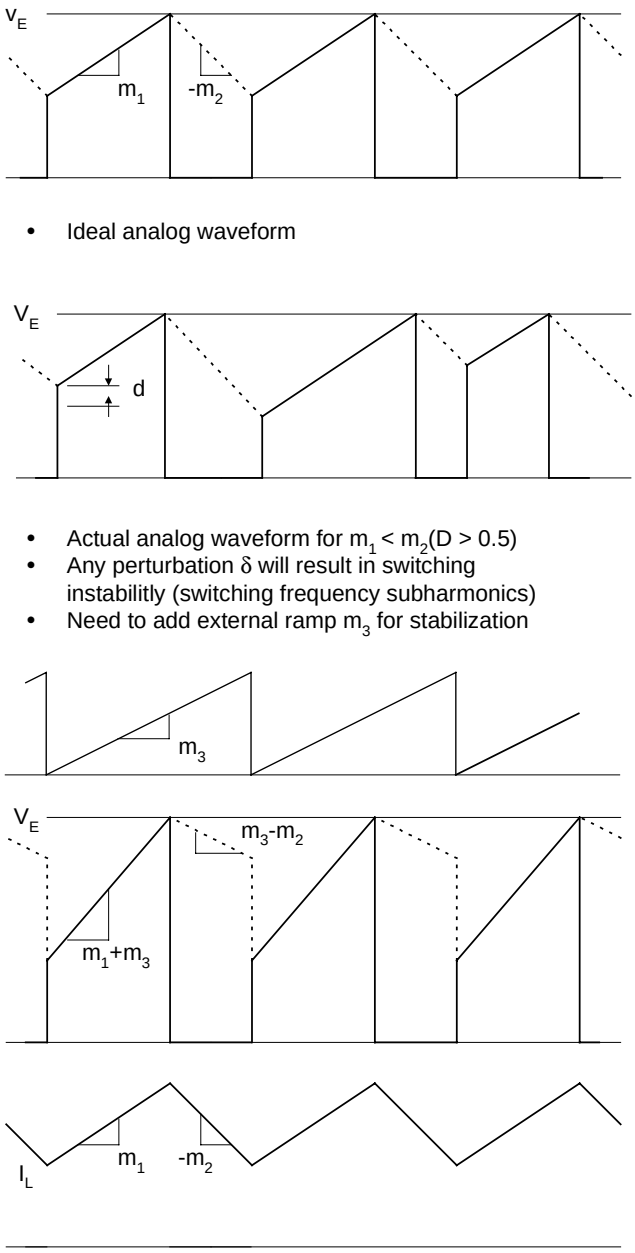


Fig. 23. Peak current-mode switching instability.

The waveforms in the upper portion of this illustration show the switch current in a CCM application with a rising inductor current slope equal to m_1 and a falling slope (when the switch is off) of $-m_2$. Under stable operating conditions, the end of m_2 has to match the beginning of m_1. With less than 50% duty cycle, $|-m_2| < m_1$ and any small perturbation (δ) which might occur during the switch on-time will be reduced by the time the next period starts and eventually die out with successive switching cycles. But with more than 50% duty cycle, $|-m_2| > m_1$ and δ will be

larger at the start of the next period, resulting in regenerative oscillation.

The cure for this is the addition of an additional ramp (m_3) on top of the current waveform so that the controller sees an up-slope of $(m_1 + m_3)$ and a downslope of $(-m_2 + m_3)$. If m_3 is chosen so that $m_3 > \frac{(m_2 - m_1)}{2}$, then $|m_3 - m_2| < m_1 + m_3$ and the system will be stable. The minimum value of m_3 for the buck converter (for the impractical condition of just borderline stability) is then

$$m_3 = \frac{(m_2 - m_1)}{2} = \frac{V_i R_S (2D-1)}{2N_t L}$$

To determine a more practical value for m_3, we first need to determine the overall closed loop gain of the system because this added ramp also has the effect of reducing the gain of both the voltage and current loops by a factor of:

$$\gamma = \frac{m_1}{m_1 + 2m_3}$$

With the constraint that $m_3 > \frac{(m_2 - m_1)}{2}$, then it is also implied that $\gamma < \frac{(1-D)}{D}$. (This expression is true for any of the three basic switching regulator topologies.)

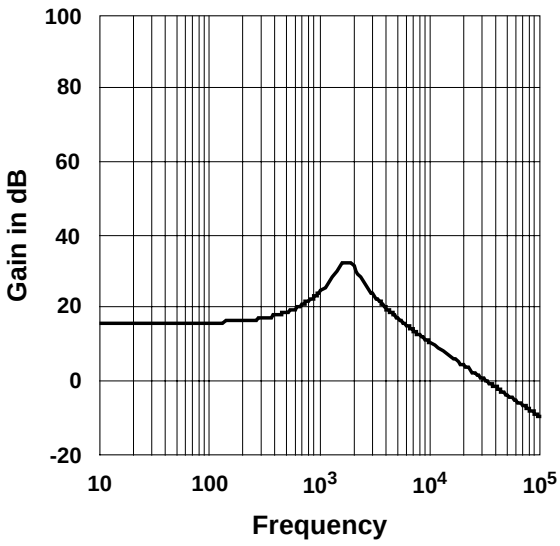
As shown in Fig. 24, the generalized control law first presented back in Fig. 12 can be used to develop individual expressions for the small-signal gains for both the current and voltage loops. This stems from the fact that, in accordance with basic flow graph theory, the total loop gain $G(s)H(s)$ of a system with two touching loops can be expressed as the sum of the individual open-loop gains, namely $G1(s)H1(s) + G2(s)H2(s)$. Note that the s term in the numerator of $G1(s)H1(s)$ provides the opportunity for lead compensation, which is why the inner current loop in current-mode control can be thought to compensate the outer voltage loop.

Any transfer function can be expressed as $\frac{T(s)}{[1 + G(s)H(s)]}$ where T(s) is the transfer function without feedback and $1 + G(s)H(s) = 0$ is the feedback related characteristic equation of the system.

Current Loop:

$$G_1(s)H_1(s) = \frac{\left(\frac{2\gamma f_S}{1-D}\right)\left(s + \frac{1}{RC}\right)}{s^2 + \frac{s}{RC} + \frac{1}{LC}}$$

$s = j2\pi f$



Voltage Loop:

$$G_2(s)H_2(s) = \frac{\left(\frac{2\gamma f_S}{1-D}\right)\left(\frac{NtK(s)}{R_S C}\right)}{s^2 + \frac{s}{RC} + \frac{1}{LC}}$$

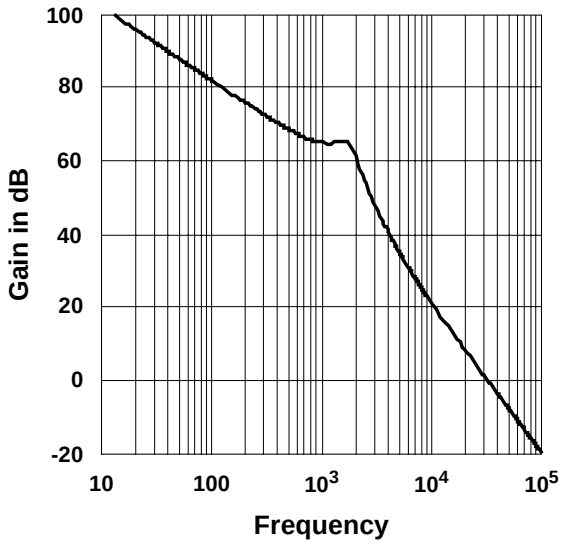


Fig. 24. Individual loop gains for linearized buck converter with peak current-mode control.

For our two-loop system, the feedback related characteristic equation becomes $1+G_1(s)H_1(s)+G_2(s)H_2(s)=0$. However, as long as $G_1(s)H_1(s)$ is never –1 (in this case the current loop phase shift is never greater than 90^o), we can divide both sides of the characteristic equation by $1+G_1(s)H_1(s)$ to form a new "single-loop" characteristic equation $\frac{1+G_2(s)H_2(s)}{\{1+G_1(s)H_1(s)\}}=0$ where the new "single-loop" open-loop gain function is:

$$G(s)H(s)=\frac{G_2(s)H_2(s)}{[1+G_1(s)H_1(s)]}$$

This single-loop representation is illustrated with the flow graph shown in Fig. 25 and results in a new open-loop voltage gain equation:

$$G(s)H(s)=\frac{\left(\frac{2f_S\gamma}{1-D}\right)\left(\frac{N_tK(s)}{R_SC}\right)}{\left(s+\frac{2f_S\gamma}{1-D}\right)\left(s+\frac{1}{RC}\right)}$$

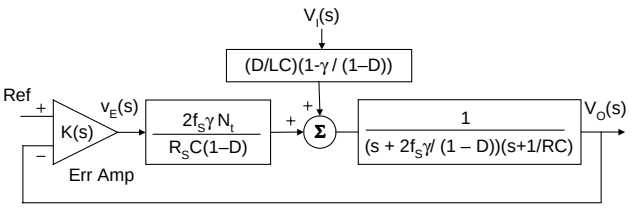


Fig. 25. Single-loop flow graph of linearized buck converter with peak current-mode control.

for the original circuit with the current-loop closed. In other words, instead of a resonant circuit with a double-pole at $\sqrt{\left(\frac{1}{LC}\right)}$, we now have a new power circuit with a dominant low frequency pole at $\frac{1}{RC} \ll \sqrt{\left(\frac{1}{LC}\right)}$, and another higher frequency pole at $\frac{2f_S\gamma}{(1-D)} \gg \sqrt{\left(\frac{1}{LC}\right)}$.

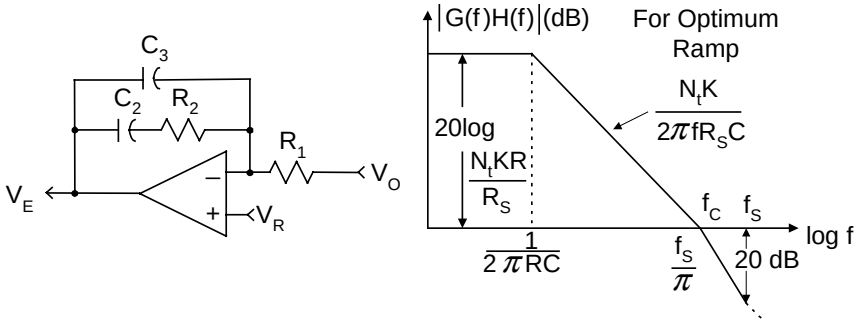
If we make the assumption that $G_1(s)H_1(s) \gg 1$ (which is the case with $f \ll \frac{f_S\gamma}{\pi(1-D)}$) the single-loop gain can now be reduced to simply:

$$G(s)H(s)=\frac{G_2(s)H_2(s)}{G_1(s)H_1(s)} \approx \frac{\frac{N_tK(s)}{R_SC}}{s+\frac{1}{RC}}$$

and the system is essentially first order.

An additional feature achieved with the combination of the voltage and current loops into the single-loop flow graph of Fig. 25, we can see that the gain block associated with the input voltage $V_i(s)$ goes to zero for $\gamma = 1 - D$, corresponding to, theoretically, zero audiosusceptibility. Thus, $\gamma = 1 - D$ implies an "optimum" ramp for $m_3 = (V_O/L)(R_S/2N_t)$, which is independent of D and is greater than the minimum requirement previously discussed. If we assume that we have applied this optimum amount of slope compensation such that $\gamma = 1-D$, then the generalized equation given in the Fig. reverts to the same simplified form that we have calculated earlier for all $f << f_S / \pi$.

Design Procedure for Peak Current-Mode Controlled Buck Converter



Step 1 : Choose R_S/N_t so that the effective peak - to - peak current analog (including ramp) $\frac{R_S D(V_i + V_O/2)}{N_t f_S L}$ is well above the noise level, e.g. 0.5 volts.

Step 2 : Choose second pole f_S/π to correspond to unity gain crossover frequency for 45° phase margin. Attenuation at f_S will automatically be 20 dB.

Step 3 : Choose $K = \frac{R_2}{R_1} = \frac{2f_S R_S C}{N_t}$ for unity gain at $f = f_C = \frac{f_S}{\pi}$.

Step 4 : Choose $\frac{1}{R_2 C_2} = \frac{1}{RC}$ for increased low - frequency gain and "zero" dc error.

Step 5 : Choose $R_2 C_3 = ESR \cdot C$ to cancel lead effect of ESR.

For EXAMPLE, Using the Following Parameter Values:

$V_i = 12\ V \qquad V_O = 5\ V \qquad f_S = 100\ kHz \qquad R = 0.5\ \Omega$

$L = 16\ \mu H \qquad C = 540\ \mu F \qquad D = 5/12 \qquad m_3 = \frac{V_O R_S}{2N_t L}$

Step 1 : $\frac{R_S}{N_t} = \frac{f_S L}{2D(V_i + V_O/2)} = 0.103 \Rightarrow R_S = 10\ \Omega, \quad N_t = 100$ Turns

Step 2 : $f_C = f_S/\pi = 31.8$ kHz (asymptotic approximation estimate)

Step 3 : $K = \frac{R_2}{R_1} = \frac{2f_S R_S C}{N_t} = 10.8$ $R_1 \ll$ input Z of op amp. $R_1 = 10\ k\Omega$, $R_2 = 107\ k\Omega$

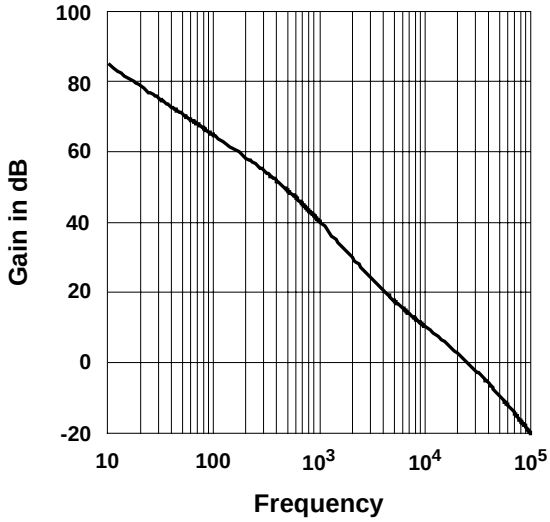
Step 4 : $C_2 = \frac{RC}{R_2} = 2.52 \cdot 10^{-9} \Rightarrow 2700$ pF

Step 5 : From data sheet, ESR = 0.022 Ω, $C_3 = \frac{ESR \cdot C}{R_2} = 1.1 \cdot 10^{-10} \Rightarrow 100$ pF

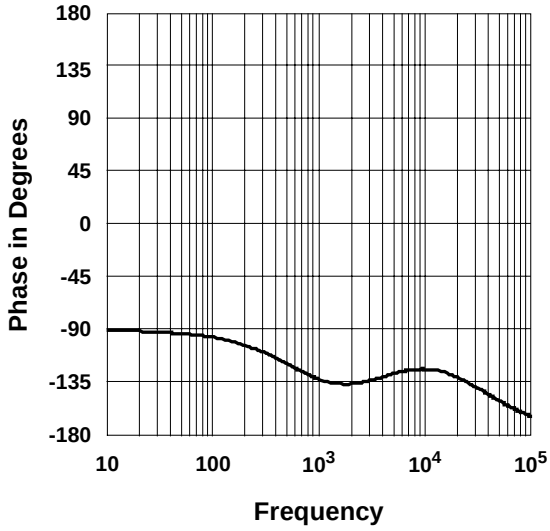
XIII. Design Procedure for Peak Current-Mode Buck Regulator

To illustrate the design procedure for a buck regulator using a single-loop peak current-mode control algorithm, a typical example using a current sense transformer and slope compensation is presented in the accompanying sidebar box and the results are shown in the Bode Plots of Fig. 26.

This example assumes transformer current sensing and slope compensation, the latter because, even though the nominal input-to-output voltage ratio predicts a duty cycle of less that 50%, operating extremes and circuit tolerances could potentially push the duty cycle higher and, of course, we have also seen the benefit of improved audio susceptability. The design criterion here is to achieve at least 45^o of phase margin, which corresponds to setting the higher frequency pole at the unity gain crossover frequency, with a gain of -20 dB at the switching frequency. This corresponds to an asymptotically predicted gain-bandwidth of $f_S/\sqrt{10}$, or approximately f_S/π, as compared to the gain-bandwidth of approximately $f_S/10$ for our lead compensated voltage-mode control example. Note that in push-pull applications, where the possibility of signal reinforcement at $f_S/2$ exists, additional attenuation at the switching frequency may be necessary to prevent subharmonic oscillations. More sophisticated analyses, simulations and/or empirical studies could help to adequately address these large-signal issues for nonlinear systems.



The gain – bandwidth is greater than 25 kHz.



The Phase Margin is 45^o for:

$R_S = 10\ \Omega$	$R_2 = 107\ k\Omega$
$N_t = 100$ turns	$C_2 = 2700$ pF
$R_1 = 10\ k\Omega$	$C_3 = 100$ pF

Fig. 26. Bode plot of peak current-mode controlled sample buck converter open-loop gain function with optimum ramp.

The compensation-related benefits of current-mode control are seen in the plots of Fig. 26, which shows what is essentially a first-order system within the gain-bandwidth. The actual gain-bandwidth of 25 kHz ($f_S/4$) is less than the asymptotic prediction (f_S/π) because the curves are actually rounded at the break points.

XIV. THE BOOST CONVERTER

The basic boost converter topology is shown in Fig. 27 operating in the continuous conduction mode, (CCM). The operation of this circuit is a two-step process where, with the switch on, energy is added to the inductor as current increases according to $\frac{di}{dt} = \frac{V_i}{L}$. When the switch is opened, the current is shunted to the diode and the inductor discharges with a decreasing current according to $\frac{di}{dt} = \frac{-(V_o - V_i)}{L}$. For steady-state operation, the average current in the inductor must equal the DC current in the load and the average dc voltage across the inductor must equal zero. As distinguished from the buck regulator where the filter inductor and capacitor continuously work together as a "team", in a boost (and flyback) topology they essentially alternate in a "bucket-brigade" mode. While energy is being stored in the inductor, the capacitor is working alone to deliver energy to the load, and then with the switch open, the inductor replenishes the delivered energy by recharging the capacitor to prepare it for the next cycle. Since the average (DC) voltage across the inductor must be zero, we can then write (for CCM)

$$v_i d - (V_o - v_i)(1-d) = 0,$$

which gives us $V_o = \frac{v_i}{(1-d)}$

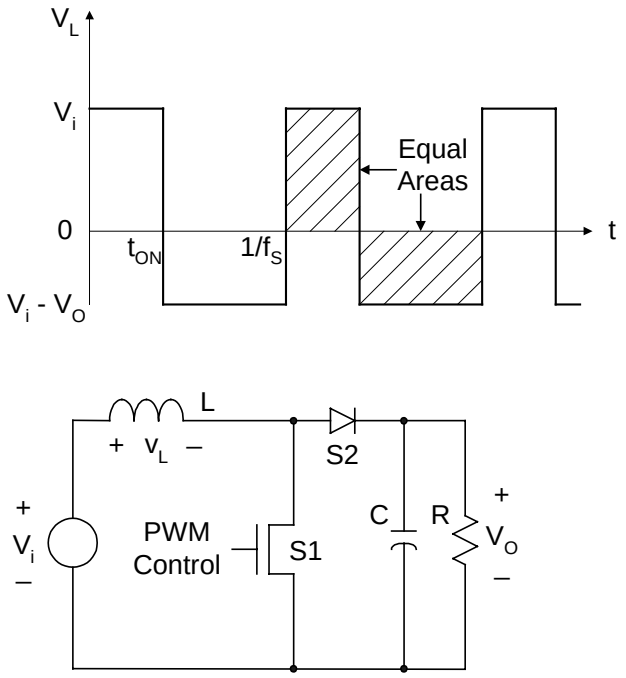
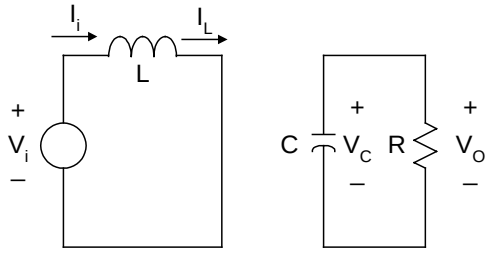


Fig. 27. The boost converter.

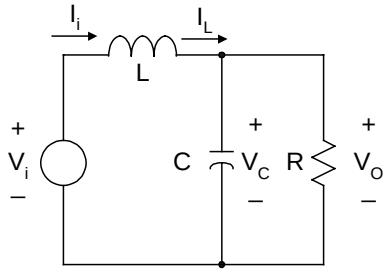
An important characteristic of both the boost and the flyback topologies in CCM is the presence of a "right-half-plane" zero, a characteristic which gives a gain increase but with a phase lag. This RHP zero is caused by the delay between controlling and delivering energy to the load. For example, a sudden increase in load current causes a droop in the output voltage, upon which the controller calls for an increase in the switch duty cycle to store more energy in the inductor. Increasing the switch on-time, however, causes a decrease in the off-time, meaning that less energy is going into the capacitor and the output voltage thus falls further. Eventually a new balance is reached to regulate at the new load but this RHP delay is almost impossible to compensate and usually requires a relatively low frequency system gain rolloff for simple voltage-mode control.

XV. Developing the Small-Signal Boost Model

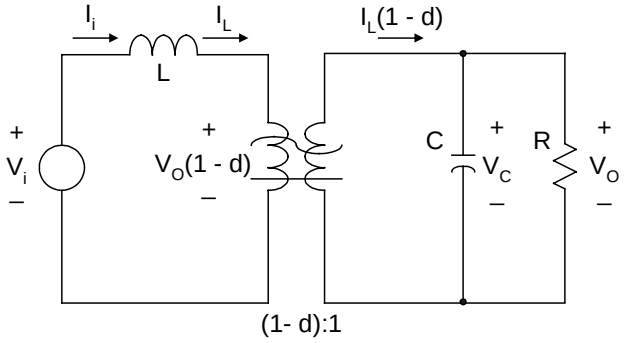
As we did with the buck topology, a small-signal model for analysis needs to be developed from the equivalent circuit by a process of averaging and linearizing. Fig. 28 shows the development of the average model by the process of first deriving an equivalent circuit for each state. Switch condition I corresponds to S_1 on and S_2 off while switch condition II has S_1 off and S_2 on. Then using the duty cycle relationships, one can determine the average voltage across the switch branches of the loops involving inductors, and the average currents through the switch branches into the nodes involving capacitors. These relationships are then connected using a DC transformer with the appropriate turns ratio.



Switch condition I [(d)th of the time]



Switch condition II [(1-d)th of the time]



Circuit model using DC transformer concept

Fig. 28. Averaged boost converter.

Fig. 29 then shows the linearization process which also follows as it did for the buck but, unlike the buck, the open loop gain function is dependent upon the DC duty factor.

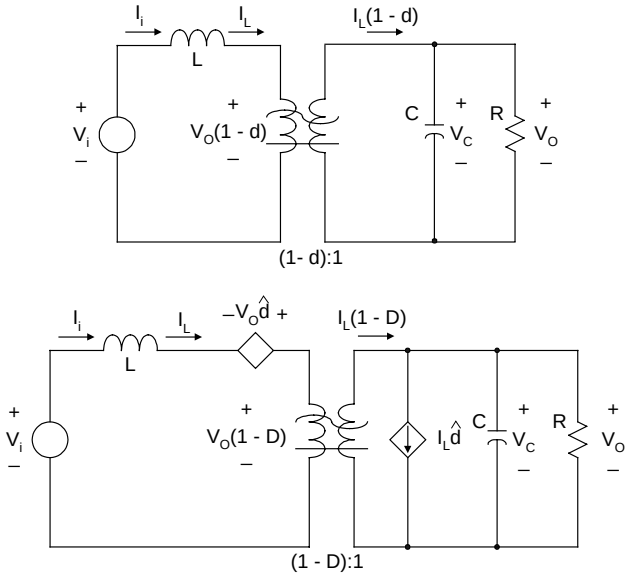


Fig. 29. Linearized boost converter.

The closed loop flow graph for the resultant linearized boost converter, using voltage-mode control, is presented in Fig. 30. From this flow graph, we can derive the overall closed loop gain equation as:

$$G(s)H(s) = \frac{V_i K(s)}{V_P RC(1-D)^2} \cdot \frac{\frac{R(1-D)^2}{L} - s}{s^2 + \frac{s}{RC} + \frac{(1-D)^2}{LC}}$$

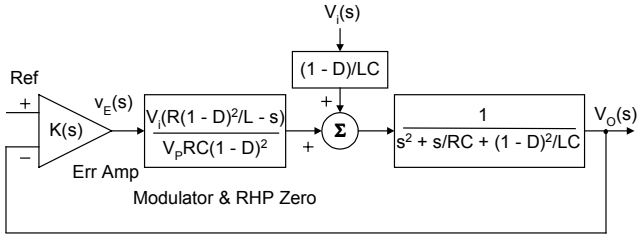


Fig. 30. Flow graph of linearized boost converter with voltage-mode control.

Note that due to the duty factor dependency, the term (1 – D) appears in the terms relating to both the resonant frequency and the RHP zero. The duty factor dependent pole is easy to rationalize as the L and C are only connected during the (1 – d) portion of the period. There is also no question about the circuit's uncompensated instability since the RHP zero contributes an added 90^o of phase shift beyond resonance, for a total of 270^o. As we have already determined, this phase lag is related to the extra time delay (as compared to the buck) in getting energy from the source out to the load, however, it is also a function of the load. The lighter the load (larger R), the further the RHP pole moves out in frequency and the less it will impact circuit behavior.

In stabilizing the voltage-mode controlled boost converter, generally only lag compensation is applicable because a set of fixed-frequency lead networks would work for only a very narrow range of input voltage and output loading. Thus, the typical voltage-mode boost converter exhibits very low gain-bandwidth and a poor dynamic response. In particular, any sudden line or load perturbation will result in a damped oscillation at the effective resonant frequency of the converter. The lag network must be designed for the lowest resonant frequency, corresponding to the maximum D, and at the lightest load for which the circuit is still in CCM operation.

These arguments apply to virtually all non-buck topologies. The similarities are evident in comparing the boost flow diagram above with the flyback shown in Fig. 31. The gain equation for an equivalent flyback topology is:

$$G(s)H(s) = \frac{NDV_i K(s)}{V_P RC(1-D)^2} \cdot \frac{\frac{R(1-D)^2}{N^2 LD} - s}{s^2 + \frac{s}{RC} + \frac{(1-D)^2}{N^2 LC}}$$

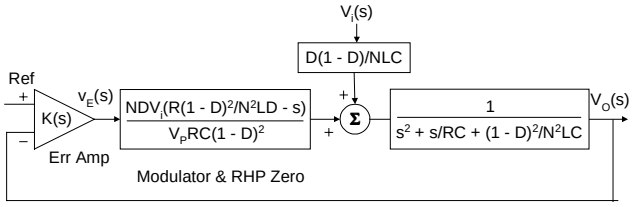


Fig. 31. Flow graph of flyback converter with voltage-mode control.

In this equation, L is the transformer inductance reflected to the primary, and N is the secondary-to-primary turns ratio. With stability issues and closed-loop dynamics virtually the same as the boost converter, the design procedures are effectively the same and, by extension, can also be applied to the Cuk and SEPIC topologies. As we shall see, the use of current-mode control will significantly improve performance, allowing these topologies to operate with a much higher gain-bandwidth.

XVI. Current-Mode Control for the Boost Converter

The boost converter with current/mode control is shown schematically in Fig. 32 and 33 – Fig. 32 with peak C/M, and Fig. 33 with average C/M implementation. As we have already mentioned, these circuits are shown assuming the use of current transformers for current sensing. If a resistor was used for sensing, R_S still applies but N_t in the equations becomes unity. Peak C/M control allows sensing switch current in place of inductor current and the switch off-time allows time for the current sense transformer to reset. With average C/M, we use the entire inductor waveform, which contains a DC component that would saturate a single current transformer. Therefore, two are shown in the schematic, alternating in measuring switch and diode current. These two signals are then summed to reconstruct the total equivalent inductor current. A current sense resistor in the input or return line may be a more practical solution in all except higher power applications but, again, this just means that $N_t = 1$ and we have kept the equations consistent.

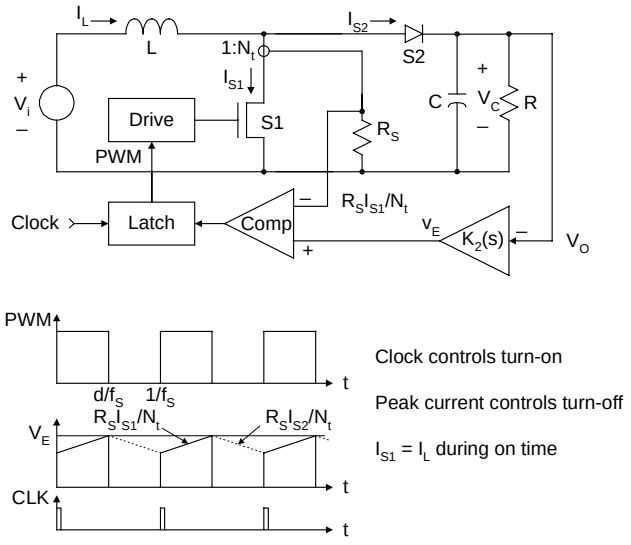


Fig. 32. Peak current-mode control for boost converter.

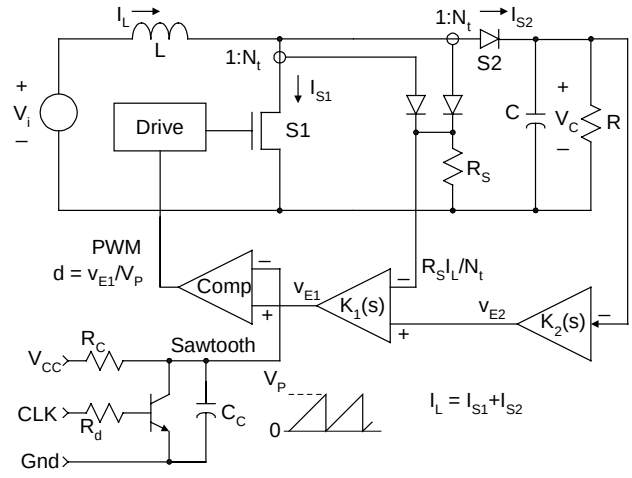


Fig. 33. Average current-mode control for boost converter.

While there are distinct differences between peak and average current-mode control, they are primarily large-signal characteristics, such as:

- Peak C/M often requires slope compensation where average C/M does not.
- Average C/M requires an additional error amplifier.
- Peak C/M offers some input voltage feed forward (but not generally as effective as in the buck).
- There is a peak-to-average control error with peak C/M.
- Average C/M often allows painless crossing of the CCM / DCM mode boundary.
- Peak C/M is highly subject to noise triggering.

Naturally, these differences cause some applications to be inherently better suited to one or the other and, in practice, different applications may impose significantly different design criteria (e.g., a slow voltage loop in a PFC application vs. a high-speed voltage regulator). However, while these distinctions between peak and average control can influence individual large-signal design criteria, their small-signal performance and closed-loop requirements can be virtually identical for the same application.

Fig. 34 illustrates the large-signal differences between peak and average C/M control for the boost converter. With average C/M, the inductor current ripple creates an opposite-phased signal at the output of the added current error amplifier (K1), amplified by its closed-loop gain. Again, large-signal criterion demands that $m_2 < m_1$ but dynamic current loop response is improved as m_2 approaches m_1. With average C/M control, slope compensation is unnecessary so the slope equations are:

$$m_1 = \frac{V_P}{T} = V_P f_S$$

$$m_2 = \frac{K_1 R_S (V_O - V_i)}{N_t L} = \frac{K_1 R_S V_O D}{N_t L}$$

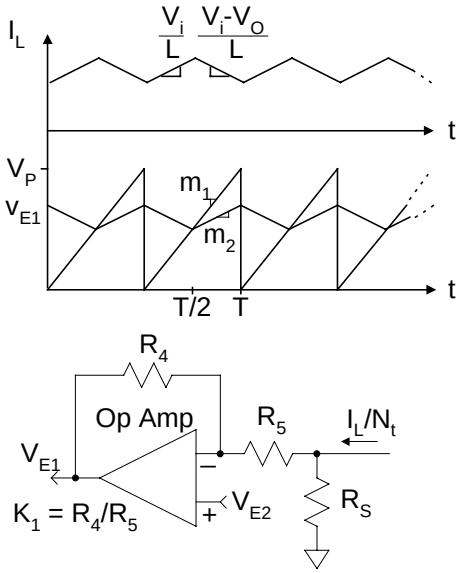
$$K_1 < \frac{V_P f_S N_t L}{R_S V_O D}$$

With peak C/M control, we need to consider slope compensation in the same manner as with the buck converter. Here the external ramp criterion is:

$$m_3 > \frac{V_O R_S (2D-1)}{2L}$$

which corresponds to $\gamma < (1\text{-}D)/D$ where gamma is the gain reduction factor introduced earlier. Although adding an external compensating ramp improves line regulation for the boost topology, it is not possible to null out input voltage sensitivity completely as it was with the buck regulator. Therefore, there is no "optimum" ramp slope for the boost converter but setting $\gamma = (1 - D)$ as we did for the buck is still a reasonable decision since $(1\text{-}D) < (1\text{-}D)/D$.

Average:



$m_2 < m_1$ for large-signal stability

$$m_1 = \frac{V_P}{T} = V_P f_s$$

$$m_2 = \frac{K_1 R_S (V_o - V_i)}{N_t L} = \frac{K_1 R_S V_o D}{N_t L}$$

$$K_1 < \frac{V_P f_s N_t L}{R_S V_o D}$$

Peak:

In the case of the boost converter, the external ramp criterion is :

$$m_3 > \frac{V_O R_S (2D-1)}{2L},$$

corresponding to $\gamma < \frac{1-D}{D}$,

where γ is the gain reduction factor.

Fig. 34. Large-signal stability considerations for current-mode boost converter.

The overall closed-loop gain equation for the linearized, C/M controlled, boost converter is derived from the flow graph in Fig. 35 as:

$$G(s)H(s) = \frac{\left(\frac{V_O F_2(s)}{RC(1-D)}\right)\left(\frac{R(1-D)^2}{L} - s\right)}{\left(s + \frac{2}{RC}\right)\left(s + \frac{V_2 F_1}{L}\right)}$$

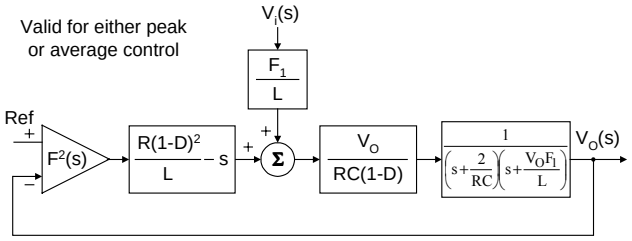


Fig. 35. Flow graph of single-loop linearized c/m controlled boost converter.

The generalized control terms, F_1 and $F_2(s)$, allow this equation to be used for either peak or average current-mode control by defining them as:

Peak:

$$F_1 = \frac{2\gamma f_S L}{V_I} \qquad F_2(s) = \frac{K_2(s) F_1}{R_S}$$

Average:

$$F_1 + \frac{R_S K_1}{V_P N_t} \qquad F_2(s) = \frac{K_2(s)(1+K_1)}{V_P}$$

Remember that F_1 represents the dependency of the control variable, d, upon the inductor current while $F_2(s)$ relates d to the output voltage. Note that the conditions for equal gain between peak and average control can be determined from the values of the terms that make F_1 and $F_2(s)$ (peak) equal to F_1 and $F_2(s)$ (average). As it did with the buck topology, the two resonant poles of the output filter have been transformed into two first-order poles: a dominate low-frequency pole and a second pole at a much higher frequency. Note that the RHP zero is included in the numerator.

XVII. COMPENSATING THE BOOST CONVERTER

The basic boost circuit gain equations and their effect are shown in Fig. 36. Note that the gain amplitude characteristic appears to be a first-order system which, in theory, should not need compensation of the voltage error amplifier to achieve stability. One could say either that the current loop compensates the voltage loop or that C/M control reduces the second-order system to a first-order, at least up to the cutoff frequency, f_C. Nevertheless, we still do have a second-order power system with a right-half-plane zero, so there is still the potential for a total of 270° of phase shift. Remember that the pole or zero phase shift shows up an order of magnitude lower in frequency than a change in amplitude.

$$G(s)H(s) = \frac{\left(\frac{V_O F_2}{RC(1-D)}\right)(2\pi f_Z - s)}{\left(s + \frac{2}{RC}\right)(s + 2\pi f_P)};$$

$$f_Z = \frac{R(1-D)^2}{2\pi L},$$

$$f_P = \frac{V_O F_1}{2\pi L},$$

$$K_2(s) = K_2$$

Valid for either peak or average control

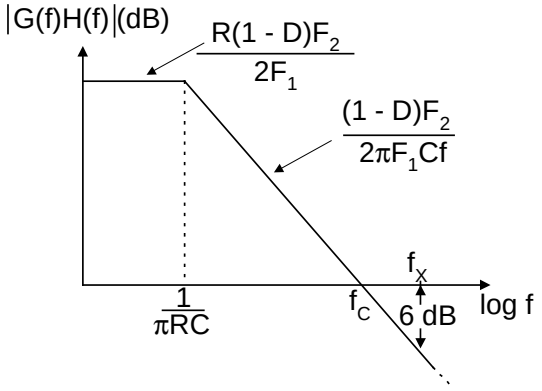


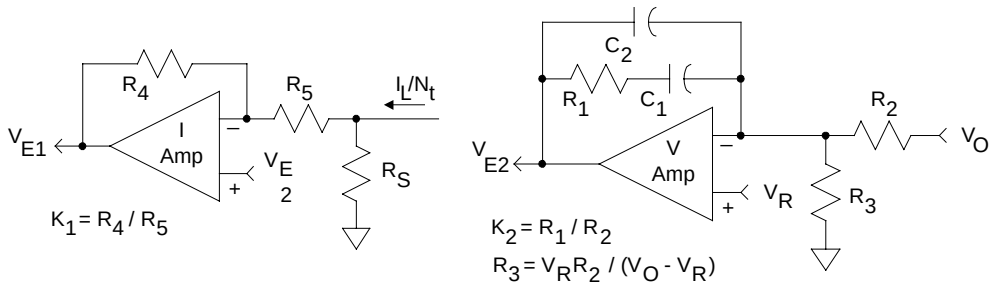
Fig. 36. Open-loop gain considerations for C/M controlled boost converter.

Since F_1 is limited by the large-signal stability criterion, one should avoid the temptation to assume that the high-frequency pole is beyond the frequency range of interest. While that pole and the RHP zero tend to cancel in terms of magnitude, their phase shifts add. However, it can be shown that if $f_Z = f_P = f_X$, and there is a 6 dB gain margin, (i.e., where the phase shift is 180°) then the phase shift at crossover is $90 + 2\left(\frac{180}{\pi}\right)\tan^{-1}\left(\frac{1}{3}\right) = 127°$, corresponding to a 53° phase margin. Thus, meeting a 6 dB gain margin should automatically insure at least a 45° phase margin. With this, a design strategy could be the following:

- If $f_Z < f_P$, then set $f_X = f_Z$
- If $f_P < f_Z$, then set $f_X = f_P$
- Worst case when $f_Z = f_P$
- Set the gain of K_2 for an open-loop gain magnitude < 0.5 at $f = f_X$ for at least 6 dB gain margin.

As an example of this overall procedure, the design steps for a hypothetical average C/M boost converter are outlined in the accompanying sidebar box. This example, of course, assumes 100% efficiency with ideal switches. The choice of L = 3.2 times critical inductance for DCM is somewhat arbitrary since increasing L in the boost topology does not result in a corresponding reduction in C as it does with the buck topology, however, it does reduce the peak currents that the switches must accommodate. In this case, the additional motivation is to show that one can go deep into CCM with the boost topology (and, in fact, any non-buck topology) and still achieve a wide-band stable system using current-mode control.

Design Procedure for Average Current-Mode Controlled Boost Converter Control Circuit



Step 1: Choose $I_{L(p-p)}R_S / N_t$ so that it is well above the noise level, e.g. $I_{L(p-p)}R_S / N_t = 0.5$ volts.

Step 2: Choose $K_1 < \dfrac{V_P f_S L N_t}{V_O D R_S}$ for large-signal stability.

Step 3: Calculate $f_Z = \dfrac{R(1-D)^2}{2\pi L}$ and $f_P = \dfrac{V_O R_S K_1}{2\pi V_P N_t L}$.

Step 4: For $f_Z < f_P$, choose $K_2 < \dfrac{R_S R C K_1 (1-D)}{2N_t L(1+K_1)}$. For $f_P < f_Z$, choose $K_2 < \dfrac{V_O C}{2L(1-D)}\left(\dfrac{R_S K_1}{V_P N_t}\right)^2$.

Step 5: Choose $1/R_1C_1 = 2/RC$ for increased low-frequency gain and "zero" dc error.

Step 6: Choose $R_1C_2 = ESR \cdot C$ to cancel lead effect of ESR.

Step 7: Choose R_3 for proper output divider ratio.

For EXAMPLE, Using the Following Parameter Values:

$V_i = 12$ V $V_O = 24$ V $f_S = 100$ kHz $L = 12\,\mu$H $C = 110\,\mu$F $R = 6\,\Omega$

$P = 96$W $V_P = 2$V $V_R = 5$V $D = 0.5$ L is 3.2 times critical inductance at full load.

$i_{L(DC)} = 8$A $i_{L(p-p)} = \dfrac{2i_{L(DC)}}{3.2} = 5$A C is chosen for less than 240 mV p-p ripple (1%).

Step 1: $\dfrac{R_S}{N_t} = \dfrac{0.5}{i_{L(P-P)}} = \dfrac{0.5}{5} = \dfrac{1}{10} \Rightarrow R_S = 10\Omega \quad N_t = 100T$

Step 2: $K_1 < \dfrac{V_P f_S L N_t}{V_O D R_S} = \dfrac{2(10^5)(12\cdot10^{-6})(100)}{24(.5)(10)} = 2 \Rightarrow 1.6$ for margin

$R_5 = 10\text{k}\Omega \qquad R_4 = 16.2\text{k}\Omega$

Step 3: $f_Z = \dfrac{R(1-D)^2}{2\pi L} = \dfrac{6(.5)^2}{2\pi(12\cdot10^{-6})} = 19.9\,\text{kHz}$

$f_P = \dfrac{V_O R_S K_1}{2\pi V_P N_t L} = \dfrac{24(10)(1.6)}{2\pi(12\cdot10^{-6})(2)(100)} = 25.5\,\text{kHz}$

Step 4: Since $f_Z < f_P$, $K_2 < \dfrac{R_S R C K_1(1-D)}{2N_t L(1+K_1)} = \dfrac{10(6)(110\cdot10^{-6})(1.6)(.5)}{2(100)(12\cdot10^{-6})(2.6)} = .845 \Rightarrow .75$

$R_1 = 7.50\,\text{k}\Omega \qquad R_2 = 10\,\text{k}\Omega$

Step 5: $\dfrac{1}{R_1C_1} = \dfrac{2}{RC} = \dfrac{2}{6(110\cdot10^{-6})} = \dfrac{1}{330\cdot10^{-6}} \Rightarrow C_1 = .05\,\mu\text{F}$

Step 6: From data sheet, $ESR = .032\,\Omega \qquad C_2 = ESR \cdot C / R_1 = 470\text{pF}$

Step 7: $R_3 = \dfrac{V_R R_2}{V_O - V_R} = \dfrac{5(16.2\cdot10^3)}{24-5} = 4.2632\cdot10^3 \Rightarrow R_3 = 4.22\text{k}\Omega + 43.2\Omega$

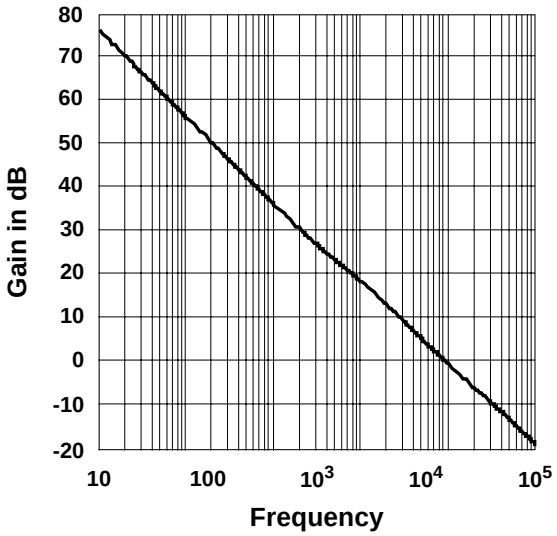
The gain and phase plots for this example are shown in Fig. 37. Note that this circuit behaves as a first-order system until the RHP zero and higher frequency poles take over; and then the phase changes doubly fast. This result shows a gain-bandwidth of > 9 kHz. By comparison, the gain-bandwidth of an equivalent, lag-compensated, voltage-mode control design would be in the range of only 130 Hz.

Again, it should be emphasized that essentially identical small-signal performance can be achieved with either peak or average C/M control, regardless of whether one places the integrating capacitor in the voltage error amplifier (as described above), or in the current amplifier (as it might be in power-factor correction circuits).

Obviously, there is much more which could be included on this subject but it is hoped that with the description and examples presented herein, the reader will be able to extrapolate to applications specific to the design problems at hand. Additional information on other circuit topologies may be found in the references given below.

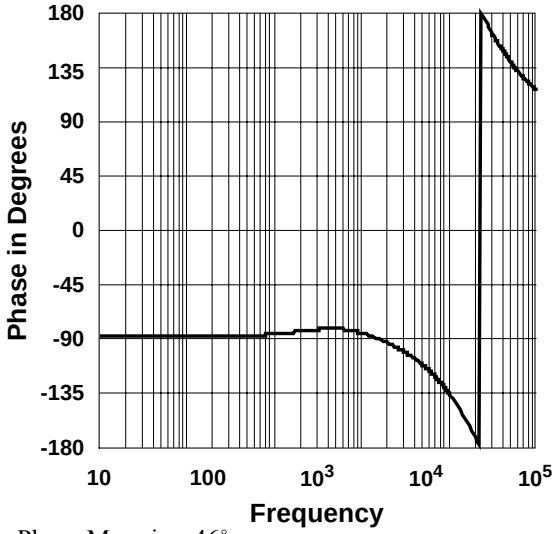
XVIII. For Further Study

Dan Mitchell teaches a two-day course covering an in-depth presentation of design, stability, and performance analyses of DC/DC converters entitled "Switching Regulator Design and Analysis". This course is a part of the Modern Power Conversion Design Techniques program offered by e/j BLOOM associates, Inc. For additional information, Dan may be reached by phone at (319) 363-8066, or by e-mail at dmmitch@home.com



Gain Margin = 7dB

Gain – Bandwidth > 9kHz



Phase Margin = 46°

Fig. 37. Open-loop gain function for average current-controlled sample boost converter.

REFERENCES

[1] D. M. Mitchell, *"DC-DC Switching Regulator Analysis"*, McGraw-Hill, 1988, DMMitchell Consultants, Cedar Rapids, IA, 1992 (reprint version).

[2] D. M. Mitchell, *"Small-Signal Mathcad Design Aids"*, (Windows 95 / 98 version), e/j BLOOM Associates, Inc., 1999.

[3] George Chryssis, *"High-Frequency Switching Power Supplies"*, McGraw-Hill Book Company, 1984.

[4] Ray Ridley, *"A More Accurate Current-Mode Control Model"*, Unitrode Seminar Handbook, SEM-1300, Appendix A2.

[5] Lloyd Dixon, *"Control Loop Design"*, Unitrode Seminar Handbook, SEM-800.

[6] Lloyd Dixon, *"Control Loop Design – SEPIC Preregulator Design"*, Unitrode Seminar Handbook, SEM-900, Topic 7.

[7] Lloyd Dixon, *"Closing the Feedback Loop"*, Unitrode Seminar Handbook, SEM-300, Topic 2.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265