Gowin MIPI D-PHY RX TX

User Guide

IPUG112-2.02E, 07/06/2019

Disclaimer

Revision History

Date	Version	Description
04/24/2017	1.0E	Initial version.
05/16/2018	1.1E	Description of MIPI D-PHY 1:16 added.
03/05/2019	2.0E	Description of MIPI IO added.
06/06/2019	2.01E	● 1:16 Mode device support added; ● LP signal port description updated.
07/12/2019	2.02E	● Description of IP interface signals updated; ● Supported products added; ● Notes for the resistance value in Figure 4-1, Figure 4-2, and Figure 4-3 added.

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1 About This Guide

1.1 Purpose

The purpose of this Gowin MIPI D-PHY RX TX User Guide is to help users to quickly understand how to use the GOWINSEMI MIPI D-PHY RX TX by providing an overview of the functions, features, ports, timing, configuration, and reference design, etc, which helps users to quickly learn Gowin MIPI D-PHY RX TX features and usage.

1.2 Supported Products

The information presented in this guide applies to the following products:

1. GW1N series of FPGA Products
2. GW1NR series of FPGA Products;
3. GW1NS series of FPGA Products;
4. GW1NSR series of FPGA Products;
5. GW2A series of FPGA Products;
6. GW2AR series of FPGA Products.

1.3 Related Documents

The user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. GW1N series of FPGA Products Data Sheet
2. GW1NS series of FPGA Products Data Sheet
3. GW1NR series FPGA Products Data Sheet
4. GW1NSR series of FPGA Products Data Sheet
5. GW2A series FPGA Products Data Sheet
6. GW2AR series FPGA Products Data Sheet
7. Gowin YunYuan Software User Guide

1.4 Terminology and Abbreviation

The terminology and abbreviations used in this manual are as shown in Table 1-1.

Table 1-1 Abbreviations and Terminology

Terminology and Abbreviations	Meaning
IP	Intellectual Property
RAM	Random Access Memory
LUT	Look-up Table
GSR	Global System Reset

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

+Tel: +86 755 8262 0391

2 Overview

2.1 MIPI D-PHY TX RX IP

Gowin MIPI D-PHY TX RX IP applies to the display serial interface (DSI) and the camera serial interface (CSI), which is designed to receive and send pictures or video data. MIPI D-PHY provides a physical layer definition.

Table 2-1 MIPI D-PHY RX/TX IP

MIPI D-PHY RX/TX IP	
IP Core Application	
Supported Devices	● MIPI D-PHY 1:8 mode:GW1N, GW1NR, GW1NS, GW1NSE, GW1NSR, GW2A, and GW2AR series; ● MIPI D-PHY 1:16 mode: GW1N-6, GW1N-9, GW1NR-9, GW1NS, and GW1NSE series; ● MIPI IO is only supported by GW1N-9 and GW1NR-9.
Logic Resource	Please refer to Table 3-2 and Table 3-3.
Delivered Doc.	
Design Files	Verilog (encrypted)
Reference Design	Verilog
TestBench	Verilog
Test and Design Flow	
Synthesis Software	Synplify_Pro
Application Software	GoWinYunYuan

2.2 MIPI D-PHY

The Mobile Industry Processor Interface (MIPI) is an interface standard for mobile devices. MIPI D-PHY provides a physical definition for DSI and CSI and describes the physical layer interface protocols of source synchronous, high speed, and low power. In accordance with application requirements, MIPI D-PHY includes RX and TX, which are used for

receiving or sending the data in line with MIPI D-PHY. Figure 2-1 shows the structure view.

MIPI D-HPY typically incorporates one clock lane and from one to four data lanes. You can configure the number of data lanes using IDE. The clock and data lanes can switch between1.2V LVCMOS signal and SLVS-200 differential signal.

MIPI D-PHY supports the following two data transmission modes:

- High-speed (HS) mode
- Low-power (LP) mode

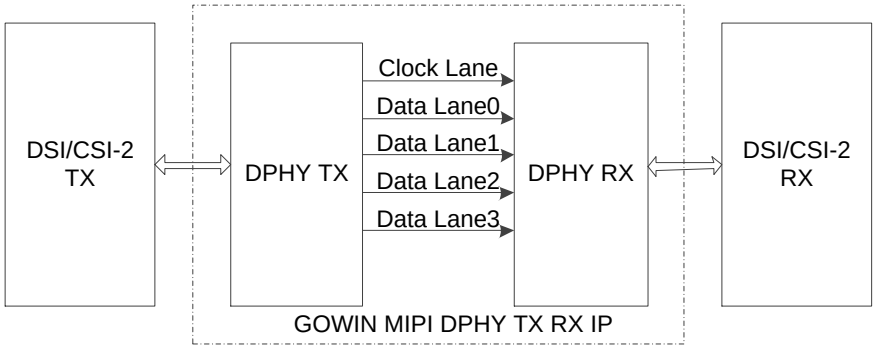
In HS mode, video data is delivered over a differential pair. Depending on the applications, the HS mode can be utilized at all times, or the D-PHY can switch from HS differential lanes to signal ended data.

When D-PHY is sending single ended data, this is referred to as the LP mode.

Note!

- In camera and display applications, the device enters the LP mode, which reduces power during the blanking period.
- In display applications, LP mode is used for screen configuration.

Figure 2-1 MIPI D-PHY Structure View



3 Features and Performance

3.1 Key Features

- In line with *MIPI Alliance Standard for D-PHY Specification*, version 1.1;
- Interfaces to MIPI CSI2 and DSI, RX and TX devices;
- Supports unidirectional High-speed (HS) mode;
- Supports bidirectional Low-power operation mode;
- Deserializes and serializes high-speed data into byte data packets;
- Supports MIPI D-PHY TX 8:1 mode and 16:1 mode;
- Supports MIPI D-PHY RX 1:8 mode and 16:1 mode;

  Note!

  MIPI D-PHY 1:16 mode is currently supported by GW1N-6K, GW1N-9K, GW1NR-9K, GW1N-1S and GW1NS series.
- Supports IO Types of ELVDS, TLVDS, and MIPI IO

  Note!

  MIPI IO is only supported by GW1N-9 and GW1NR-9.
- In HS mode, the line rate of the single channel port supports the range 80Mb/s to 800Mb/s.
- Data transmission is maintained in LP mode at a speed of 10Mb/s.

3.2 Max. Frequency

The maximum frequency of MIPI D-PHY is mainly determined by the line rate and the speed grade of the devices.

3.3 Latency

D-PHY TX Latency is the time delay from inputting the data_in (8-bit/16-bit parallel data) to outputting HS_DATA.

D-PHY RX Latency is the time delay from inputting the HS_DATA SOT (start-of-transmission) to outputting data_out (8-bit/16-bit parallel data).

See Table 3-1 for the detailed Latency.

Table 3-1 D-PHY TX RX Latency

Module	Line Rate（Mb/s）	Lanes	Latency (byteclk Latency [1] Cycle)
D-PHY TX	800	1	3
D-PHY RX	800	1	11

Note!

[1] Frequency of byteclk (MHz) = line rate in Mb/s / 8

3.4 Resource Utilization

The Verilog performance and resource utilization of MIPI D-PHY RX and TX Its performance and resource utilization may vary when the design is employed in a different device, or at a different density, speed, or grade.

Take the GW1N-4 device as an example. See and Table 3-2 and Table 3-3 for the MIPI D-PHY RX and TX resource utilization. For the applications on the other GOWINSEMI devices, please refer to the later release.

Table 3-2 MIPI D-PHY RX Resource Utilization

Device	Speed Grade	Name	Resource Utilization	Remarks
GW1N-4	-5	LUT	318	● 1:8 Mode ● contains four data lanes ● contains word alignment and lane alignment modules ● no clk_cross_fifo
		IODELAY	4	
		REG	300	
		BSRAM	4	
		IDES8	5	
		CLKDIV	1	
		DHCEN	1	

Table 3-3 MIPI D-PHY TX Resource Utilization

Device	Speed Grade	Name	Resource Utilization	Remarks
GW1N-4	-5	LUT	16	● 8:1 Mode ● Internal PLL is not configured.
		REG	4	
		CLKDIV	1	
		OSER8	4	

4 Functional Description

MIPI D-PHY contains the following two D-PHY IP modules:

- D-PHY RX
- D-PHY TX

In D-PHY RX and D-PHY TX modules, HS data is deserialized/serialized to and from single data rate byte packets respectively. The data in LP mode can be transmitted bi-directionally on any data channel or clock channel.

Note!

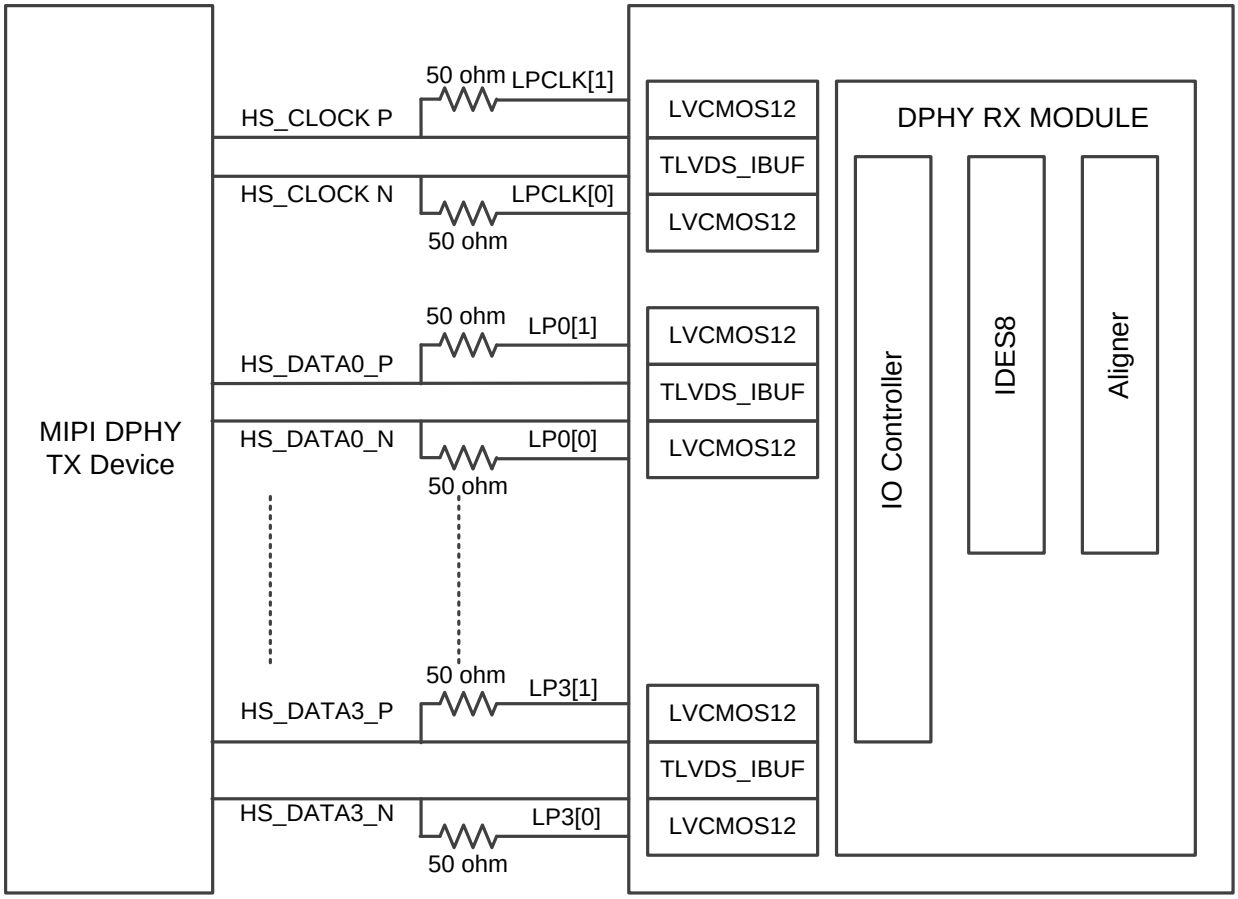
D-PHY RX and D-PHY TX have different resister networks; however, both modules support bi-directional LP communication and unidirectional HS communication.

4.1 MIPI D-PHY RX Structure and Function

HS data can be received on one clock lane and four clock data lanes using D-PHY RX.

Each clock and data lane uses four I/Os. Two I/O pins are used to receive HS data with TLVDS differential I/O. TLVDS I/O is used to handle the common 200mV mode voltage. The other two I/Os are used as serial termination in HS mode, and can be used to transmit or receive 1.2V CMOS data in LP mode, as shown in Figure 4-1.

Figure 4-1 HS Mode and LP Mode Interface Implementation



Note!

The resistance value in Figure 4-1 is only for reference.

In D-PHY RX module, HS data is deserialized using IDES8/IDES16. FPGA drives a divide-by-4/divide-by-8 clock and 8 bits/16 bits byte data directly using IDES8/IDES16.

Note!

The number of data lanes can be configured. Options are 1, 2, 3, or 4 data lanes.

When the data is deserialized to 8 bits/16 bits byte data, and the lane is aligned, MIPI byte data is available on each byte clock cycle.

Note!

- The alignment is done based on the recognition of MIPI HS_Ready sequence.
- MIPI HS_Ready sequence is transimitted on all data lanes one clock cycle before the packet header.

hs_en is used to reset the alignment module:

1. When hs_en is low, the word alignment module is reset;
2. When hs_en is high, the word alignment module looks for the next HS_Ready sequence;

3. When HS_Ready sequence is detected, the sync signal will increase, and the byte data at the output of the aligner will be properly aligned.

The aligner module consists of two subsidiary modules as below:

- The first module aligns the 8-bit data from the deserializer.
- The second module aligns each of the data lanes to each other.

Note!

- In some cases, lane alignment or lane and word alignment is not needed;
- Macro compiling commands can be used to turn the word and lane alignment on and off.

HS termination is designed to be implemented by controlling IO_Ctrol_RX module with term_en signal. Although there is no direction detection mechanism, the following two ways can be used to enable HS termination:

1. The HS clock can be used to observe LP to HS data transition on one data lane.
2. In comparison to the data lane, the clock lane will enter the HS mode sooner and exit the HS mode later. Initialize the LP signals as input at startup, and then observe the clock and data lanes of LP and HS. Once the sequence is detected, term_en can be set to "low" by enabling HS_termination.

The IO_Ctrol_RX module also controls LP signal.

Each data lane has a lp*_dir signal, which controls LP data direction between the FPGA and the transmitting device.

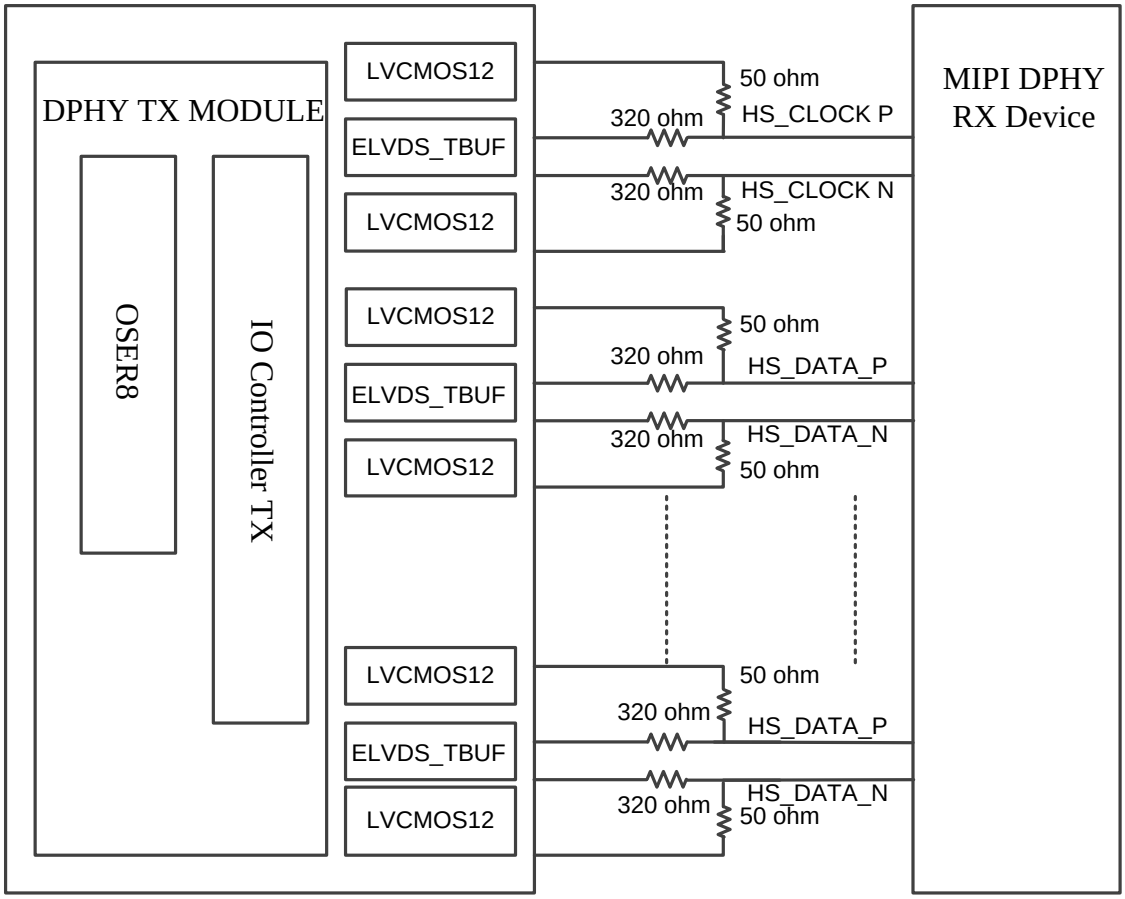
You can turn on/off LP IP for each clock and data lane individually by using Macro complier directives. This can be convenient if the user requires the LP mode for one or two MIPI D-PHY data lanes.

The LP signals are defined as two bit buses. Signal 1 is usually connected to the P wire side, and 0 to the N wire side. This maintains the consistency with the LP transition identification scheme.

4.2 MIPI D-PHY TX Structure and Function

D-PHY TX IP gives users the ability to utilize one clock lane and up to four data lanes. Each lane has four I/Os. Two I/O pins transmit HS data with ELVDS type or TLVDS type I/O. The other two I/O pins are used to provide voltage dividing circuit in HS mode and to transmit or receive 1.2V CMOS data in LP mode. For the circuit structure of HS data adopting ELVDS type I/O, please refer to Figure 4-2; for the circuit structure of adopting TLVDS type I/O, please refer to Figure 4-3.

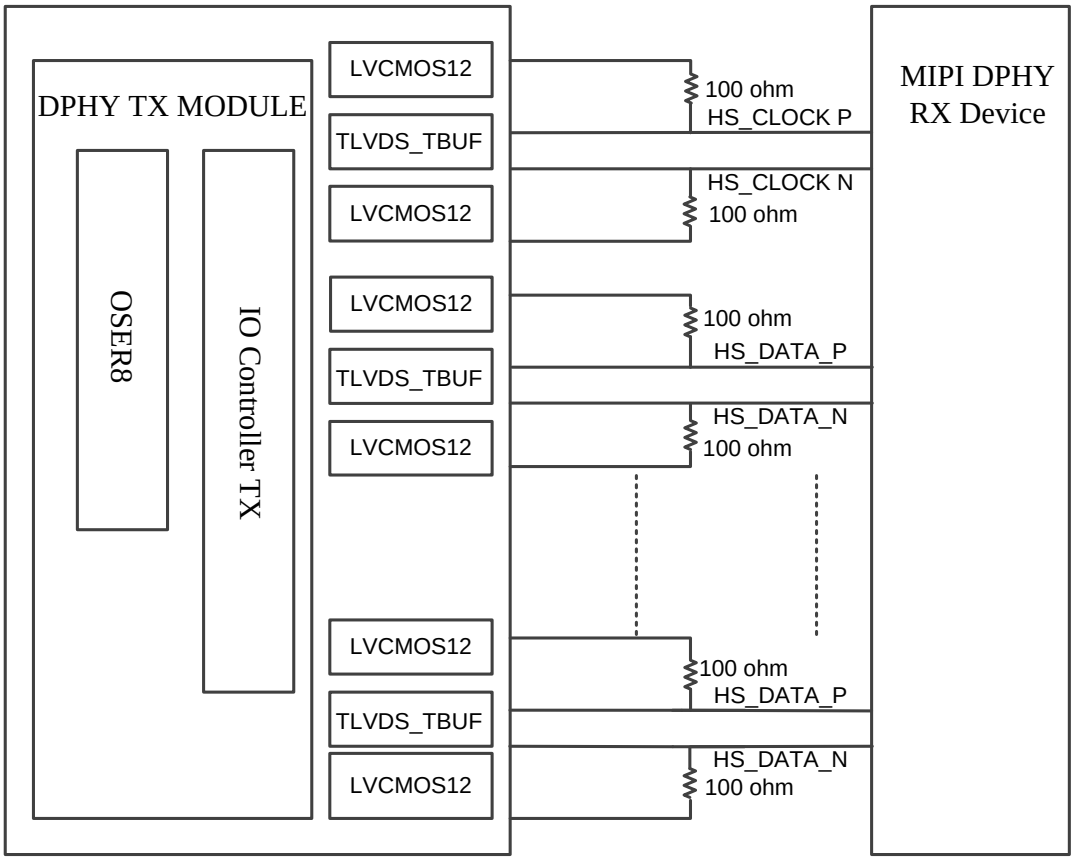
Figure 4-2 HS Mode and LP Mode Interface Implementation, HS Adopting ELVDS



Note!

The resistance value in Figure 4-2 is only for reference.

Figure 4-3 HS Mode and LP Mode Interface Implementation, HS Adopting TLVDS



Note!

The resistance value in Figure 4-3 is only for reference.

In the D-PHY TX module, HS data is serialized using OSER8/OSER16. D-PHY TX data is center aligned, so HS data lane and clock lane adopt the clock output signal with a phase shifting 0 and 90 degrees generated by the PLL respectively. Users can select to use the external PLL or internal PLL to provide clock. It should be noted that it takes some time for the internal PLL in FPGA to lock.

IO_Ctrol_TX module controls HS and LP data traffic:

- When hs_clk_en and hs_data_en signals are high, clock and data lanes are enabled in HS mode. In HS mode, IO_Ctrol_TX sets CMOS signals low to create a voltage divider network on LVDS output signals to achieve a 200mV common mode voltage;
- When hs_clk_en or hs_data_en is low, ELVDS I/O is set to high impedance, so it does not interfere with LP data transmissions. As MIPI specification defines clock lane going in to or out of HS mode before or after the data lanes, there is an hs_clk_en control signal and an hs_data_en signal;

lp_data_dir signal controls the LP mode direction:

- When hs_*_en='1', the lp*_dir control signal is overwritten;
- While in LP mode, IO_Ctrol_TX module also controls the LP data traffic.
  The lp*_dir signal controls LP mode data traffic direction. The LP signals are defined as two bit buses. Signal 1 is usually connected to the P wire side, and 0 to the N wire side, which maintains consistency with LP transition identification scheme.

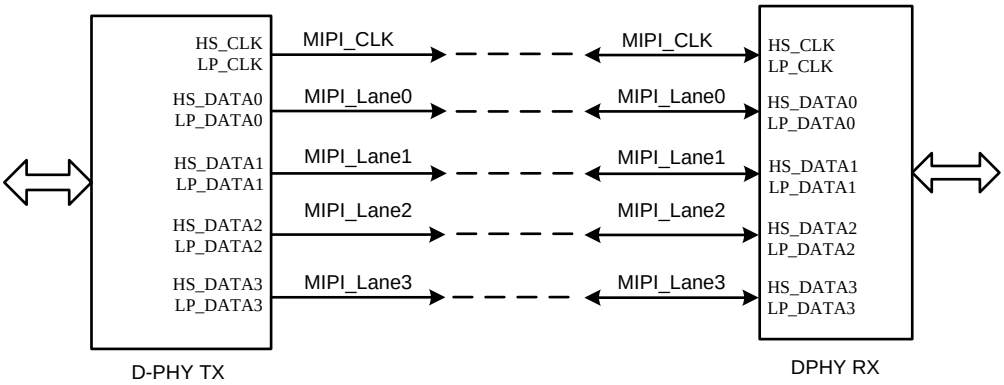
4.3 MIPI IO

MIPI D-PHY TX RX IP ports support MIPI IO. As shown in Figure 4-4, when you select MIPI IO TYPE, HS clock lane and LP clock lane share IOs, and HS data lane and LP data lane share IOs too.

Note!

It is currently supported by GW1N-9K and GW1NR-9K.

Figure 4-4 MIPI IP Ports in MIPI IO Mode



5 Ports Description

5.1 MIPI D-PHY RX Ports

For the MIPI D-PHY RX I/O ports description, please refer to Table 5-1.

Table 5-1 D-PHY RX I/O Ports

Signal	I/O	Description
reset_n	Input	Reset signal, active low
HS_CLK	Input	● HCLK ● When IO TYPE is TLVDS or ELVDS
HS_DATA<*N*>	Input	● High-speed data lane<N> ● When IO TYPE is TLVDS or ELVDS
hs_en	Input	Initialize the word alignment module at the next HS-Ready sequence
clk_byte	Input	The read clock of clk_cross_fifo.
clk_byte_out	Output	Clock Byte Out = HS_CLK/4
data_out<*n*>	Output	● Parallel data output, data lane <*n*> ● When MIPI D-PHY is 1:8, the width is 8 bits; ● When MIPI D-PHY is 1:16, the width is 16 bits;
ready	Output	Active "high" when parallel data is aligned
LP_CLK [1:0]	Bidirectional	● LP clock lane; ● LP_CLK[0] = P wire, LP_CLK[1] = N wire； ● When IO TYPE is TLVDS or ELVDS
LP_DATA<*N*> [1:0]	Bidirectional	● LP data lane<N>; ● LP<N> [0] = P wire, LP<N> [1] = N wire； ● When IO TYPE is TLVDS or ELVDS
term_en	Input	Terminal resistor control signal; ● In MIPI IO mode, 1: turn on resistor, 0: turn off resistor; ● In other IO Type modes, 1: control LP signal output 0, 0: lp_data_dir<n> control LP signal output.

Signal	I/O	Description
lp_clk_dir	Input	Control the direction of LP clock ● '0': LP clock receive ● '1': LP clock transmit
lp_data<*n*>_dir	Input	Controls the direction of LP data ● '0': LP data receive ● '1': LP data transmit
lp_clk_out [1:0]	Output	● LP receives clock ● Available when lp_clk_dir = '0' and term_en = '0'
lp_data<*n*>_out [1:0]	Output	● LP receive data ● Available when lp_ data<*n*>_dir = '0' and term_en = '0'
lp_clk_in [1:0]	Input	● LP transmits clock ● Available when lp_clk_dir = '1' and term_en = '0'
lp_data<*n*>_in [1:0]	Input	● LP transmits data ● Available when lp_ data<*n*>_dir = '1' and term_en = '0'
MIPI_CLK	Bidirectional	When IO TYPE is MIPI IO, HS and LP share the same clock lane.
MIPI_LANE<*N*>	Bidirectional	When IO TYPE is MIPI IO, HS and LP share the same data lane.

Note!

The high and low of lp_clk_in and lp_clk_out is corresponded to the high and low of LP_CLK.

The high and low of lp_data<n>_in and lp_data<n>_out is corresponded to the high and low of lp_data<n>.

5.2 MIPI D-PHY RX Ports

For the MIPI D-PHY TX I/O ports description, please refer to Table 5-2.

Table 5-2 D-PHY TX I/O

Signal	I/O	Description
reset_n	Input	Reset signal, active low
HS_CLK	Output	● HCLK ● When IO TYPE is TLVDS or ELVDS
HS_DATA<*N*>	Output	● High-speed data lane<N> ● When IO TYPE is TLVDS or ELVDS
clk_byte	Input	The input clock when using internal PLL
CLKOP	Input	The input clock while adopting external PLL. The phase difference between CLKOP and CLKOS is 90°, and they have the same frequency with HS_CLK;
CLKOS	Input	
sclk	Output	TX internal clock output, generally used for sampling data_in;

Signal	I/O	Description
data_in<*n*>	Input	● Parallel data input, data lane <*n*> ● When MIPI D-PHY is 8:1, the width is 8 bits; ● When MIPI D-PHY is 16:1, the width is 16 bits;
LP_CLK [1:0]	Bidirectional	● LP clock lane; ● LPCLK[0] = P wire, LP_CLK[1] = N wire； ● When IO TYPE is TLVDS or ELVDS
LP_DATA<*N*> [1:0]	Bidirectional	● LP data lane<*N*>; ● LP<*N*> [0] = P wire, LP<N> [1] = N wire ● When IO TYPE is TLVDS or ELVDS
hs_clk_en	Input	Enables HS clock on output, set LP_CLK signals as 0, and overwrite lp_clk_dir signal
hs_data_en	Input	Enables HS clock on output, set LP_DATA<*N*> signals as 0, and overwrite lp_data<*n*>_dir signal
lp_clk_dir	Input	Control the direction of LP clock ● '0': LP clock receive ● '1': LP clock transmit
lp_data<*n*>_dir	Input	Controls the direction of LP data ● '0': LP data receive ● '1': LP data transmit
lp_clk_out [1:0]	Input	● LP transmits clock ● Available when lp_clk_dir = '1' and hs_clk_en = '0', no terminal resistance in TX
lp_data<*n*>_out [1:0]	Input	● LP transmits data ● Available when lp_ data<*n*>_dir = '1' and hs_data_en = '0'
lp_clk_in [1:0]	Output	● LP receives clock ● Available when lp_clk_dir = '0' and hs_clk_en = '0', no terminal resistance in TX
lp_data<*n*>_in [1:0]	Output	● LP receive data ● Available when lp_ data<*n*>_dir = '0' and hs_clk_en = '0'
MIPI_CLK	Output	When IO TYPE is MIPI IO, HS and LP share the same clock lane.
MIPI_LANE<*N*>	Output	When IO TYPE is MIPI IO, HS and LP share the same data lane.

Note！

The high and low of lp_clk_in and lp_clk_out is corresponded to the high and low of LP_CLK.

The high and low of lp_data<n>_in and lp_data<n>_out is corresponded to the high and low of lp_data<n>.

6 Timing Description

This chapter mainly describes the input signals timing of MIPI D-PHY RX and TX in HS mode.

In practical applications, RX and TX can be connected; i.e., RX output can be TX input, and TX output can be RX input. Therefore, only the timing for RX and TX input signals is described as below.

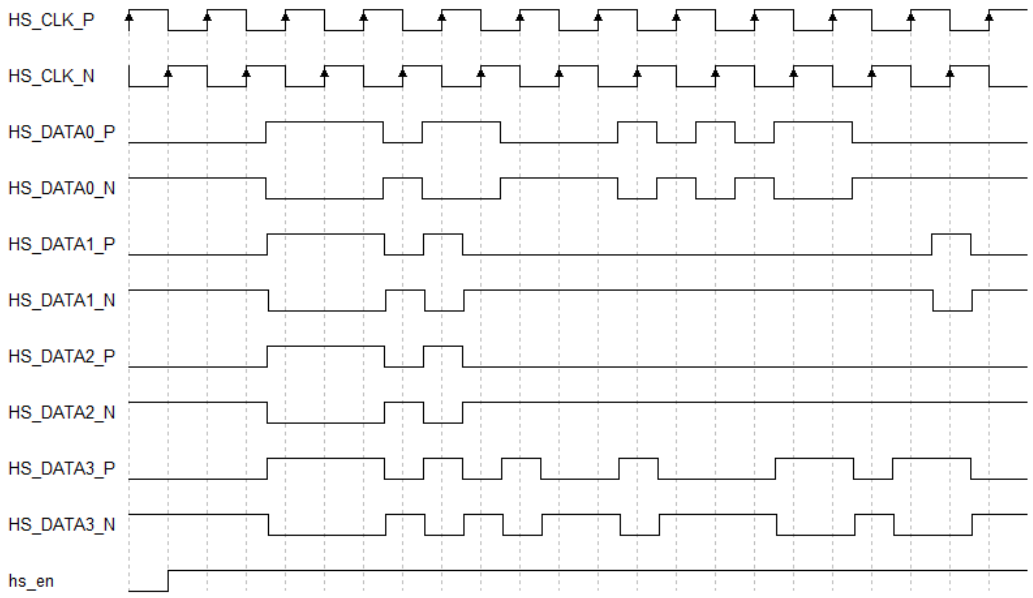
6.1 RX Input Signal Timing

The clock and data lane signal timing of MIPI D-PHY RX in HS 1:8 mode is as shown in Figure 5-1.

One clock lane (HS_CLK) and four data lanes (HS_DATA0, HS_DATA1, HS_DATA2, andHS_DATA3) are used in the diagram. Clock lane and data lane are all differential signal input. In HS mode, clock and data center is aligned when transmitting image data. The signal hs_en needs to be set to high before receiving HS_DATA data.

The signal timing of MIPI D-PHY RX in HS 1:16 mode is similar to that of 1:8 mode. Note that the data width is 16 bits (2byte) after RX conversion. RX will put the first received data to the low 8 bits.

Figure 6-1 Input Signal Timing of MIPI D-PHY RX in HS 1:8 Mode



6.2 TX Input Signal Timing

The clock and data lane signal timing of MIPI D-PHY TX in HS mode is as shown in Figure 6-2.

When using TX:

- If internal PLL is set to use, clk_byte needs to be provided (the frequency is 1/4 of HS_CLK);
- If internal PLL is not set to use, CLKOP and CLKOS with 90-degree phase difference need to be provided. (CLKOP, CLKOS, and HS_CLK have same frequency)

In Figure 6-2, 8:1 mode is adopted and one clock lane (HS_CLK) and four data lanes (data_in0, data_in1, data_in2, and data_in3) are used. The hs_clk_en and hs_data_en signals need to be set as high before receiving data_in data.

In Figure 6-3 16:1 mode is adopted. The timing is similar to that of 8:1 mode. In 16:1 mode, 16 bits (2 bytes) data is converted in each cycle. The low 8 bits (low byte) data will be sent first, so the packet header of B8 locates in the low 8 bits of the first data.

Figure 6-2 Input Signal Timing of MIPI D-PHY TX in HS 1:8 Mode

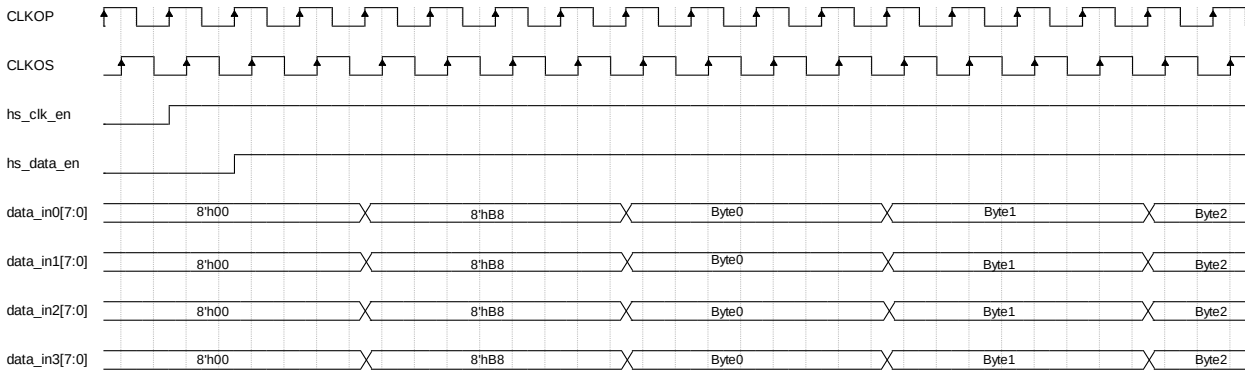
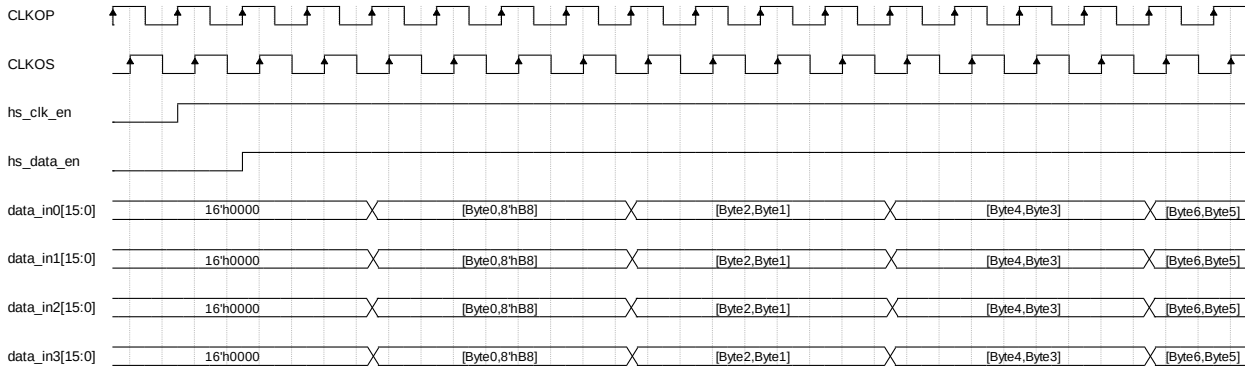


Figure 6-3 Input Signal Timing of MIPI D-PHY TX in HS 1:16 Mode



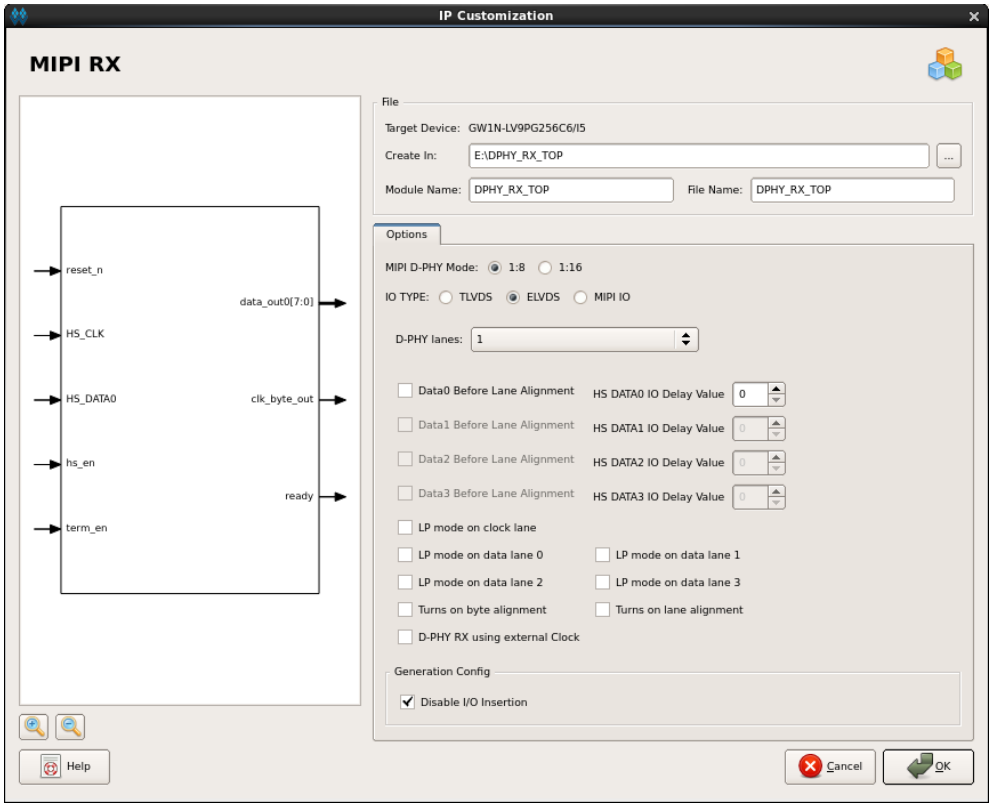
7 MIPI D-PHY RX/TX Configuration and Generation

Start "IP Core Generator" from the "Tools" menu in the Gowin YunYuan software and then configure and generate the MIPI D-PHY RX and MIPI D-PHY TX.

7.1 MIPI D-PHY RX Configuration

The configuration options for MIPI D-PHY RX are shown in Figure 7-1.

Figure 7-1 MIPI D-PHY RX Configuration



1. Name the MIPI D-PHY RX by modifying the "File Name";
2. Create the top module name of MIPI D-PHY RX by modifying "Module Name";
3. Adjust the "Options" to configure the number of HS data lane, the clock and data lane in LP mode, and the byte alignment or lane alignment, etc. Table 7-1 lists the detailed options configuration.
4. Only one HS clock lane and one HS clock lane are used by default.

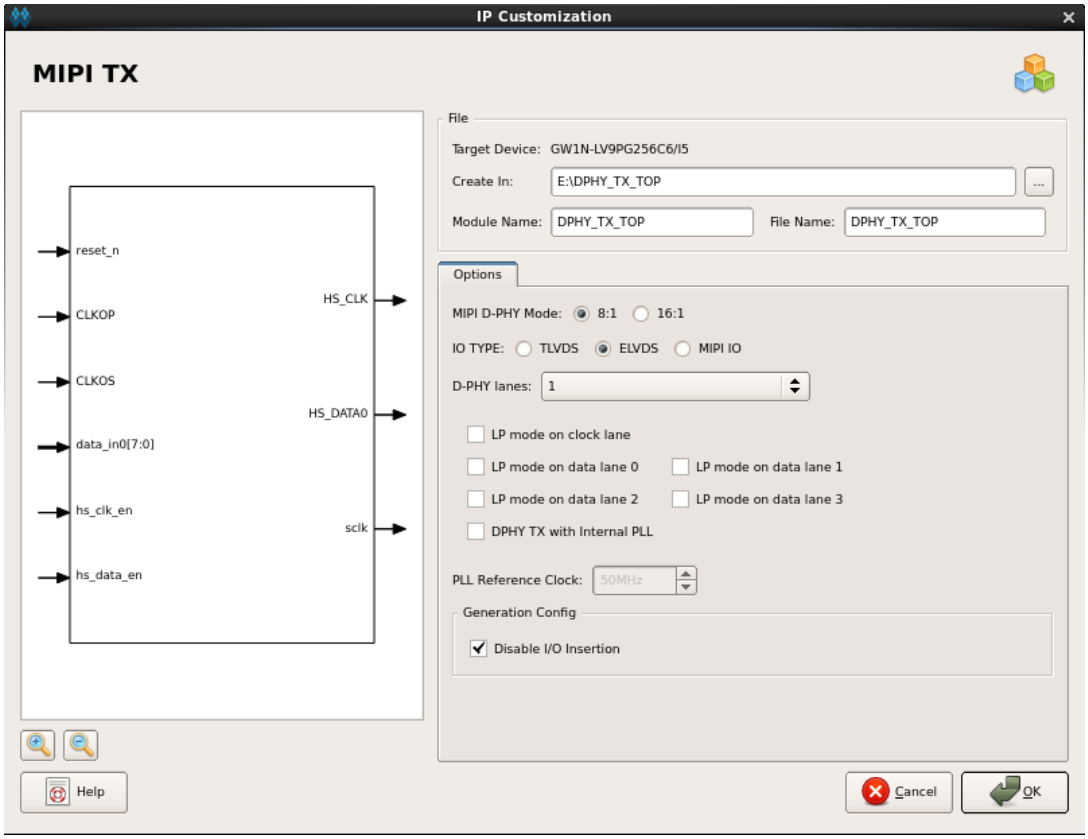
Table 7-1 MIPI D-PHY RX Options

Options	Description
D-PHY lanes	1: Generates one data lane HS_DATA0;
	2: Generates two data lanes HS_DATA0 and HS_DATA1;
	3: Generates three data lanes HS_DATA0, HS_DATA1, and HS_DATA2;
	4: Generates four data lanes HS_DATA0, HS_DATA1, HS_DATA2, and HS_DATA3.
MIPI D-PHY Mode	Set the data transmission mode as 1:8 or 1:16
IO TYPE	Set HS Lane port as ELVDS, TLVDS, or MIPI IO
Data3/2/1/0 Before Lane Alignment	Set whether to generate data port, output data before entering the lane alignment module HS Lanes can be set independently
HS Data3/2/1/0 IO Delay Value	Set the IO Delay value of HS Lane ports HS Lanes can be set independently
LP mode on clock lane	Generates LP_CLK[1:0] and the other I/O ports for LP mode on clock lane.
LP mode on data lane0	Generates LP_DATA0[0:1] and the other I/O ports for LP mode on data lane0.
LP mode on data lane1	Generates LP_DATA1[1:1] and the other I/O ports for LP mode on data lane0.
LP mode on data lane2	Generates LP_DATA2[2:1] and the other I/O ports for LP mode on data lane0.
LP mode on data lane3	Generates LP_DATA3[3:1] and the other I/O ports for LP mode on data lane0.
Turns on byte alignment	Check this option to enable byte alignment, which is used to align the bytes after deserializing on one lane.
Turns on lane alignment	Check this option to enable lane alignment, which is used to align different data lanes;
D-PHY RX using external Clock	Check this option for RX module to use an external clock (clk_byte), and data_out0/1/2/3 will align at clk_byte.

7.2 MIPI D-PHY TX Configuration

The configuration options for MIPI D-PHY RX are shown in Figure 7-2.

Figure 7-2 MIPI D-PHY TX Configuration



1. Name the MIPI D-PHY TX file by modifying the "File Name";
2. Create the top module name of MIPI D-PHY TX by modifying "Module Name";
3. Adjust the "Options" to configure the number of HS data lane, whether the clock and data lane in LP mode use the internal PLL or not, etc. Table 7-2 lists the detailed configuration options that are available.
4. Only one HS clock lane and one HS clock lane are used by default.

Table 7-2 MIPI D-PHY TX Options

Options	Description
D-PHY lanes	1: Generates one data lane HS_DATA0;
	2: Generates two data lanes HS_DATA0 and HS_DATA1;
	3: Generates three data lanes HS_DATA0, HS_DATA1, and HS_DATA2;
	4: Generates four data lanes HS_DATA0, HS_DATA1, HS_DATA2, and HS_DATA3.
MIPI D-PHY Mode	Set the data transmission mode as 1:8 or 1:16
IO TYPE	Set HS Lane port as ELVDS, TLVDS, or MIPI IO
LP mode on clock lane	Generates LP_CLK[1:0] and the other I/O ports for LP mode on clock lane.
LP mode on data lane0	Generates LP_DATA0[0:1] and the other I/O ports for LP mode on data

Options	Description
	lane0.
LP mode on data lane1	Generates LP_DATA1[1:1] and the other I/O ports for LP mode on data lane0.
LP mode on data lane2	Generates LP_DATA2[2:1] and the other I/O ports for LP mode on data lane0.
LP mode on data lane3	Generates LP_DATA3[3:1] and the other I/O ports for LP mode on data lane0.
D-PHY TX with Internal PLL	In this mode, TX module will use an internal PLL. The internal PLL will generate a pair of clock with 90-degree phase difference.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