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HyperLynx®
Release Notes

Software Version VX.2.7

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Chapter 1

HyperLynx® SI/PI/Thermal

HyperLynx SI/PI/Thermal Problems Fixed

- **dts0100933393** – SDF file created by Generic Batch mode needs to be documented
- **dts0101347618** – True differential IBIS [Model] Input_diff generates errors without Vinh and Vinl
- **dts0101372484** – IBIS AMI eye mask adjustment - eye should be passing
- **dts0101373170** – Some vias look shorted in board viewer and Via Visualizer shows clearances using the auto antipad clearance when actual padstack has antipad defined.
- **dts0101377646** – ODB++ import gives strange results
- **dts0101382585** – Tcl File Viewer reports 'can't use non-numeric string as operand of "*"' during DDRx Wizard run
- **dts0101382765** – Unable to open "ezwave_cmds.txt": no such file or directory when opining EZwave with runEZwave.bat.
- **dts0101383000** – Analyzed 3D EM non-existing shapes appear when creating 3D area and is also visible in advance solver
- **dts0101385268** – Unexpected behavior in LineSim when saving after deleting inner layer in Stackup Editor
- **dts0101385393** – The Set Model Compilation Parameters in DDRx Timing Model Editor causes unexpected behavior
- **dts0101385655** – Different current density with 45/135 degree trace.
- **dts0101386912** – Selection Keep Existing Project in Add or Edit 3D Area dialog does not work
- **dts0101387058** – Component pads are not proper shapes are missing/incomplete.
- **dts0101387314** – Error: Multi-conductor system
- **dts0101387316** – About DSN file translation
- **dts0101388460** – Unexpected behavior in HyperLynx when running an S-parameter simulation
- **dts0101388606** – HyperLynx has unexpected behavior on S-parameter export if Remove Non-Functional Pads enabled
- **dts0101393940** – Encountered an improper argument error in Japanese OS and Japanese menu.
- **dts0101396043** – The FFS file will can't be opened by LineSim next time if we create a 3D EM model for a via

HyperLynx SI/PI/Thermal Workarounds

- **dts0100765638** - New value of thermal conductivity set in CES stackup does not show up in BoardSim when a board is extracted from Expedition PCB through PI interface.

  Workaround: Set the thermal-conductivity values manually inside HyperLynx, in the Stackup Editor.

- **dts0100906430** - Problem during save, EZwave warning message while exiting HyperLynx

  Workaround: Exclude file settings.properties.lock (or this file type) from search indexing

- **dts0100941780** - HyperLynx can't simulate HSPICE 2011.09-SP2 Netlist and fails with error

  Workaround: Run without VPN

Chapter 2

HyperLynx® DRC

HyperLynx DRC Problems Fixed

- **dts0101365748** – HyperLynx DRC component outlines are only partially translated when importing Zuken CR5000 layout with multiple component outlines
- **dts0101376455** – HyperLynx DRC rule displays unexpected behavior on Linux
- **dts0101379419** – Vertical reference plane change misses a violation where Multi-Stitch is required
- **dts0101382488** – Metal Island DRC reports an Isolated Metal on UnconCondShps in the middle of a mounting hole
- **dts0101383785** – HyperLynx DRC event On Open Document is not found in type library
- **dts0101384443** – Silk Screen when enable covers the entire board.
- **dts0101384502** – Stackup Technology does not match what is set in the Xpedition
- **dts0101384637** – Via pads on solder mask layer is not shown in CCE design
- **dts0101385831**– "Mounting Holes appear to be shifted after translation from Allegro Design"
- **dts0101386052** – HyperLynx DRC hangs without a proper error message in conditions with insufficient RAM
- **dts0101387025** – HyperLynx DRC Stackup Editor does not follow the Unit Setting in Options Setting
- **dts0101387054** – Unexpected run time error
- **dts0101387524** – The rule Long Stub should ignore the violating trace stubs overlapped with plane shapes
- **dts0101387677** – Inconsistent names for bridged nets found between HyperLynx DRC projects opened on .pcb and the exported .cce
- **dts0101388231** – Pad offset is not enabled in CIBD format
- **dts0101391466** – Violation Display method doesn't work
- **dts0101392116** – Unexpected behavior with trying to set up user object list/constant nets/electrical nets
- **dts0101394449** – HyperLynx DRC Embedded rule doc link doesn't work properly
- **dts0101397470** – Unexpected behavior when running the rule “Multi-layers Creepage Distance” with option “Generate Passed Results” set to “yes”

HyperLynx DRC Workarounds

- **Design Synchronization**

  To synchronize a design with the data in Constraint Manager, go to Setup > Options > Constraint Manager and change the option for Constraint Manager Data Import to "Every time design is loaded". This ensures that all electrical nets, differential pairs, and model assignments comply with what is set in Constraint Manager. However, this requires that any modifications to these objects be performed in Constraint Manager.

- **dts0100887937** - Promote settings dialog box doesn't display "Unit System" setting

  Workaround: Change the “Units System” setting by loading the *.hldset file into HyperLynx DRC and editing it using Setup/Options dialog.

- **dts0100890261** - HyperLynx DRC Diff Pair DRC compares the wrong pair of vias

  Workaround: HyperLynx DRC may fail to identify the correct via pairs for multiple blind/buried via transitions spaced very close together.

- **dts010934349** - CES First Time versus Every Time

  Workaround: "First time" use, may result in a design that has different electrical nets, diff pairs etc., than the same design with every time sync to CES. The "Every time" mode requires the user to go to CES to change data entered in CES rather than being able to override it in HyperLynx DRC.

- **dts0101041832** - Bad Copper Balancing Graphics

  Workaround: To avoid this problem, run HyperLynx DRC in standalone and not use sCCZ stream.

- **dts0101134127** - XAC/sCCZ PCB designs with Negative Plane layers are missing plane data in HLDRC using sCCZ

  Workaround: First copy the design, switch to Positive Plane with Dynamic Plane Data State, verify the copper area is valid, then run the DRC's as needed.

- **dts0101205724** - pdm.dll appears to be missing for Internet Explorer install directory for Windows 10

  Workaround: Start a CMD window with administrator privilege. In the CMD window, run: regsvr32 C:\Windows\System32\F12\pdm.dll

- **dts0101270765** - Release Switcher will switch the IC Packaging/Enterprise release but HyperLynx DRC still points to the IC Packager release

  Workaround: The Analysis Control will be launched from the tools installed last. So if Xpedition PCB is installed and then Package Designer, the XAC comes from the Package Designer install but will still work.

Chapter 3

HyperLynx® Advanced Solvers

HyperLynx Advanced Solvers Problems Fixed

- **dts0101345597** – Metric units for current density in power scope gets replaced with imperial units
- **dts0101353711** – Could not create proper pin groups as port reference (sink) pins in a specific design
- **dts0101363544** – Lost connection due to licenses lost not reusing the solver buffer when you resume the simulation
- **dts0101376022** – Incorrect Via Model in VX.2.5, model extracted using Full-Wave Solver
- **dts0101379511** – Problem with AFS Options in cluster processing
- **dts0101380428** – 3D Area Manager - Non-passive/Non-causal models
- **dts0101382284** – ACIS Mesh failed when the model is cropped with boundary type ARR
- **dts0101386491** – Adding series ferrite bead in PI decoupling analysis- not affecting results
- **dts0101390678** – DC drop analysis results are not consistent between single board and multiboard
- **dts0101394893** – HyperLynx FWS projects have shorts due to polygon problem

HyperLynx Advanced Solver Workarounds

- **dts0101286080** - JD2 GUI not working on RHEL6

  Workaround: The new GUI for JD2 requires GTK3, which is not included nor available for this RHEL6 platforms. Please use RHEL7.

- **dts0101173933** - Port extension does not work when source and sink are on the same net

  Workaround: Run create valid nets to split nets in case they are broken pieces of metals connected through series components.

- **dts0101360681** - Roughness settings does not correctly translate from BoardSim to HyperLynx Full Wave Solver (FWS)

  Workaround: Set the roughness flag and model parameters in HyperLynx FWS manually.

Chapter 4

HyperLynx® Documentation

HyperLynx Documentation Problems Fixed

None

HyperLynx Documentation Workarounds

Broken Links in PDF Documentation - (MG595892)

Due to enhanced security restrictions with web browser PDF plug-ins, some links do not function. Links in HTML documentation are fully functional.

Clicking a link within a PDF viewed in a web browser may result in no action, or it may load the title page of the current PDF manual (instead of the intended target in the PDF manual). The unresolved link behavior occurs in all web browsers on Windows® and Linux® platforms. Because of this behavior, the navigational experience of PDF manuals is compromised. PDF is ideal for printing because of its page-oriented layout.

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