Si2173-A30

WORLDWIDE HYBRID TV TUNER WITH ANALOG DEMODULATOR

Features

- Worldwide hybrid TV tuner
  - Analog TV: NTSC, PAL/SECAM
  - Digital TV: ATSC/QAM, DVB-T/T2/C, ISDB-T/C, DTMB
  - 42–1002 MHz frequency range
- Compliance with A/74, NorDig, D-Book, C-Book, ARIB, EN55020, OpenCable™ specifications
- Highly-integrated, lowest BOM
  - No SAW filters required
  - Integrated LNA and tracking filters
- No alignment, tuning or calibration
- Best-in-class real-world reception
  - Exceeds MOPLL-based tuners
- Analog TV (ATV) demodulator
  - Superior video SNR performance
- Customizable ATV & DTV filters
- Flexible output interface
  - CVBS + SIF/AF to AV processor
  - DLIF to DTV demodulator
- 3.3 and 1.8 V supply voltage
- Standard CMOS process
- 6 x 6 mm, 40-pin QFN package
- RoHS compliant

Ordering Information:

See page 28.

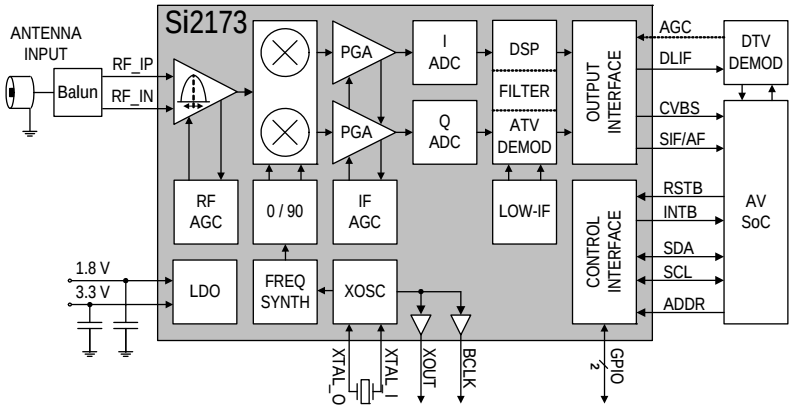
Applications

- Hybrid ½-NIM, ¾-NIM and full-NIM
- iDTV (Integrated Digital TV)
- Digital terrestrial and cable STB
- Hybrid PVR and DVD recorder

Description

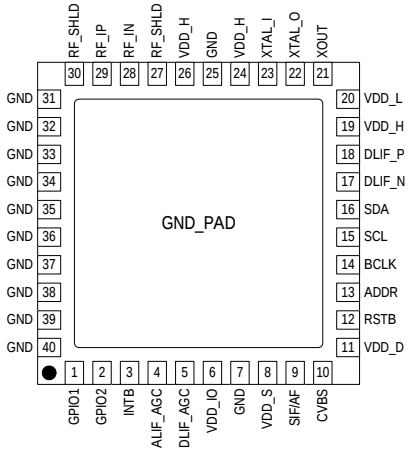
The Si2173 integrates a complete hybrid tuner with analog TV demodulator supporting all worldwide terrestrial and cable TV standards. Leveraging Silicon Labs' proven digital low-IF architecture, the Si2173 extends the unmatched performance and design simplicity of the original Si2170/1/2 while further reducing footprint size. No external LNAs, tracking filters, or SAW filters are used. Compared with competing silicon tuners and discrete MOPLL-based tuners, the Si2173 delivers superior picture quality and a higher number of received stations in real-world conditions due to its very high linearity and low noise. Interfacing the Si2173 seamlessly with the Si2165 DVB-T/C demodulator creates a terrestrial and cable hybrid PAL/SECAM and DVB-T/C receiver.

Functional Block Diagram



Pin Assignments

Si2173
(Top View)



Patents pending

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1. Electrical Specifications

Table 1. Recommended Operating Conditions[1]

Parameter	Symbol	Min	Typ	Max	Unit
Analog High Supply Voltage	V_{DD_H}	3.15	3.3	3.6	V
Analog Low Supply Voltage	V_{DD_L}	1.7	1.8	1.9	V
Digital Supply Voltage	V_{DD_D}	1.7	1.8	1.9	V
I/O Supply Voltage	V_{DD_IO}	1.7	—	3.6	V
Interface Supply Voltage	V_{DD_S}	1.7	1.8 to 5.0	5.5	V
Ambient Temperature[2]	T_A	–20	25	85	°C

Notes:
1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions unless otherwise stated. Typical values apply at $V_{DD\_H} = V_{DD\_IO} = V_{DD\_S} = 3.3$ V, $V_{DD\_L} = V_{DD\_D} = 1.8$ V, and $T_A = 25$ °C. Parameters are tested in production unless otherwise stated.
2. The maximum ambient temperature applies to a PCB having θ_{JA} of 27 °C/W under the maximum power consumption condition specified in Table 3. The Si2173 package has θ_{JC} of 3 °C/W (independent of PCB implementation). Refer to "AN413: Si217x Layout and Design Guidelines" for additional details on thermal considerations.

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Min	Max	Unit
Analog High Supply Voltage	V_{DD_H}	–0.3	3.9	V
Analog Low Supply Voltage	V_{DD_L}	–0.3	2.0	V
Digital Supply Voltage	V_{DD_D}	–0.3	2.0	V
I/O Supply Voltage	V_{DD_IO}	–0.3	3.9	V
Interface Supply Voltage	V_{DD_S}	–0.3	5.8	V
I/O Input Voltage[2,3]	V_{IN_IO}	–0.3	V_{IO} + 0.3	V
Interface Input Voltage[2,4]	V_{IN_S}	–0.3	V_S + 0.3	V
ADDR Pin Input Voltage[2]	V_{IN_A}	–0.3	V_H + 0.3	V
Input Current[3,4]	I_{IN}	–10	10	mA
Operating Temperature	T_{OP}	–25	95	°C
Storage Temperature	T_{STG}	–55	150	°C

Notes:
1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure beyond recommended operating conditions for extended periods may affect device reliability.
2. V_H, V_L, V_D, V_{IO}, and V_S are the concise representations of V_{DD_H}, V_{DD_L}, V_{DD_D}, V_{DD_IO}, and V_{DD_S}, respectively.
3. For input pins GPIO1, GPIO2, DLIF_AGC, RSTB.
4. For input pins SCL, SDA.

Table 3. DC Characteristics[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Total Power Consumption[2]	P_D	VHF bands[3]	—	1.04	1.23	W
		UHF bands[3]	—	0.94	1.14	W
High Voltage Supply Active Current[2]	I_H	VHF bands[3]	—	212	228	mA
		UHF bands[3]	—	181	203	mA
Low Voltage Supply Active Current[2]	I_L		—	190	217	mA
High Voltage Supply Powerdown Current[4]	I_{PDH}		—	—	8	mA
Low Voltage Supply Powerdown Current[4]	I_{PDL}		—	—	15	mA
High Voltage Supply Standby Current[5]	I_{SH}		—	90	105	mA
Low Voltage Supply Standby Current[5]	I_{SL}		—	33	60	mA
I/O High Level Input Voltage[6,7]	V_{IH}		0.7 x V_{IO}	—	V_{IO} + 0.3	V
I/O Low Level Input Voltage[6,7]	V_{IL}		–0.3	—	0.3 x V_{IO}	V
I/O High Level Input Current[7]	I_{IH}	V_{IN} = V_{IO} = 3.6 V	–10	—	10	µA
I/O Low Level Input Current[7]	I_{IL}	V_{IN} = 0 V, V_{IO} = 3.6 V	–10	—	10	µA
I/O High Level Output Voltage[6,8]	V_{OH}	I_{OUT} = 500 µA	0.8 x V_{IO}	—	—	V
I/O Low Level Output Voltage[6,8]	V_{OL}	I_{OUT} = –500 µA	—	—	0.2 x V_{IO}	V
Interface High Level Input Voltage[6,9]	V_{IH}		0.7 x V_S	—	V_S + 0.3	V
Interface Low Level Input Voltage[6,9]	V_{IL}		–0.3	—	0.3 x V_S	V
Interface High Level Input Current[9]	I_{IH}	V_{IN} = V_S = 5.5 V	–5	—	20	µA
Interface Low Level Input Current[9]	I_{IL}	V_{IN} = 0 V, V_S = 5.5 V	–10	—	10	µA
Interface Low Level Output Voltage[6,10]	V_{OL}	I_{OUT} = –1 mA; V_S < 2 V	—	—	0.2 x V_S	V
		I_{OUT} = –1 mA; V_S > 2 V	—	—	0.4	V

Notes:

1. High Voltage Supply combines V_{DD_H}, V_{DD_IO}, and V_{DD_S}, and is tested at 3.3 V for Typ and at 3.6 V for Max. Low Voltage Supply combines V_{DD_L} and V_{DD_D}, and is tested at 1.8 V for Typ and at 1.9 V for Max.
2. Active currents are tested in ATV mode due to ATV demodulator being turned on. BCLK is enabled. The GET_REV command is issued continuously, which performs both writes and reads over the I^2C interface.
3. VHF bands refer to desired signals below approximately 230 MHz and UHF bands above approximately 230 MHz.
4. Measured after issuing the POWER_DOWN command. BCLK, XOUT, GPIO1 and GPIO2 are disabled.
5. Measured after issuing the STANDBY command, which keeps the LNA powered up (intended for dual-tuner applications). BCLK and XOUT are enabled. GPIO1 and GPIO2 are disabled.
6. V_H, V_L, V_D, V_{IO}, and V_S are the concise representations of V_{DD_H}, V_{DD_L}, V_{DD_D}, V_{DD_IO}, and V_{DD_S}, respectively.
7. For input pins GPIO1, GPIO2, DLIF_AGC, RSTB.
8. For output pins GPIO1, GPIO2, INTB.
9. For input pins SCL, SDA.
10. For output pin SDA.

Table 4. Hybrid Tuner Characteristics

(V_H = 3.3 V, V_L = 1.8 V, V_D = 1.8 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF Characteristics[1]						
RF Input Frequency Range[2,3]	f_{IN}		42	—	1002	MHz
Input Return Loss[4]	RL	terrestrial case	—	6	—	dB
		cable case	—	8	—	dB
Frequency Tuner Step Size[5]	f_{STEP}		—	31.25 to 166.67	—	kHz
Noise Figure[6]	NF	max gain	—	4.0	6.0	dB
In-Band IIP3[7]	$IIP3_{IB}$	N±1, ±2	–15	–5	—	dBm
Out-of-Band IIP3[7]	$IIP3_{OOB}$	N±6, ±12	–3	10	—	dBm
		N±18, ±36	—	23	—	dBm
Adjacent Channel Attenuation[8]	α_{FILT}	N±1	—	80	—	dB
LO Phase Noise at 860 MHz[9,10]	PN_{LO}	125 Hz offset	—	–83	–79	dBc/Hz
		250 Hz offset	—	–91	–85	dBc/Hz
		1 kHz offset	—	–96	–93	dBc/Hz
		10 kHz offset	—	–95	–92	dBc/Hz
		100 kHz offset	—	–104	–101	dBc/Hz
LO Integrated Phase Noise at 860 MHz[9,10]	PN_{int}	DSB: 125 Hz to 4 MHz offset	—	0.4 (–43)	0.6 (–40)	° rms (dBc)
Composite Triple Beat[9,11]	CTB	per OpenCable™ OC-SP-HOST2.0-CFR-IO3-050121	—	–68	–63	dBc
Composite Second Order[9,11]	CSO		—	–68	–60	dBc
Cross Modulation[9,11]	$XMOD_{OC}$		—	–62	–57	dBc

Notes:

1. At the F-connector input of the Si2173 reference design and includes all losses from connector, balun, and PCB. Z_{SOURCE} = 75 Ω. Refer to "AN501: Si2173 Programming Guide" for details regarding programmable ranges.
2. From the lower edge of the lowest channel to the higher edge of the highest channel.
3. 43 to 1002 MHz guaranteed by test, 42 MHz guaranteed by characterization.
4. Value is the worst-case return loss across the frequency band 42 to 860 MHz. The terrestrial case refers to the default configuration used on the Si2173 reference design. Refer to "AN413: Si217x Layout and Design Guidelines" for guidelines on optimization of return loss for the cable case and the resulting modest impact on noise figure.
5. For tuning frequency programming details, refer to "AN501: Si2173 Programming Guide".
6. Averaged over ten frequencies selected to capture the minimum and maximum performance values over 47 to 1002 MHz. Guaranteed by production test.
7. Performed with AGC frozen at maximum RF gain and minimum IF gain (zero RF gain backoff) using 6 MHz channel spacing. Min values measured at worst case frequencies.
8. Attenuation of on-chip brickwall filter from RFIN to DLIF output, relative to a tone at center of desired channel (N). Refer to Figure 7 on page 21 for a typical representation of the frequency response.
9. Guaranteed by characterization.
10. DTV modes. At offsets under 1 kHz, the LO phase noise is dependent on the crystal or RCLK. Measured with KDS crystal "AT-49 24.0000 MHz, ± 25 ppm, Cload = 8 pF."
11. Tested with recommended cable BOM per "AN468: Si217x Distortion Performance with Optimized Return Loss".
12. Measured at DLIF_P/N pins.

Table 4. Hybrid Tuner Characteristics (Continued)
(V_H = 3.3 V, V_L = 1.8 V, V_D = 1.8 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
DTV RSSI Measurement Accuracy[9]	$RSSI_D$	Input between –5 dBm and –75 dBm; read 400 ms after tune complete	—	±3	—	dB
DTV Tuner Output Driver[12]						
DLIF Output Center Frequency	LIF	channel BW = 6 MHz	—	4 to 7	—	MHz
		channel BW = 7 MHz	—	4.5 to 6.5	—	MHz
		channel BW = 8 MHz	—	5 to 6	—	MHz
Differential Output Voltage Swing	V_{OD}	ac-coupled output	—	0.5 to 2.0	—	V_{ppd}
Load Resistance (each pin)	R_L	ac-coupled output	1	—	—	kΩ
Load Capacitance (each pin)	C_L	ac-coupled output	—	—	15	pF

Notes:
1. At the F-connector input of the Si2173 reference design and includes all losses from connector, balun, and PCB. Z_{SOURCE} = 75 Ω. Refer to "AN501: Si2173 Programming Guide" for details regarding programmable ranges.
2. From the lower edge of the lowest channel to the higher edge of the highest channel.
3. 43 to 1002 MHz guaranteed by test, 42 MHz guaranteed by characterization.
4. Value is the worst-case return loss across the frequency band 42 to 860 MHz. The terrestrial case refers to the default configuration used on the Si2173 reference design. Refer to "AN413: Si217x Layout and Design Guidelines" for guidelines on optimization of return loss for the cable case and the resulting modest impact on noise figure.
5. For tuning frequency programming details, refer to "AN501: Si2173 Programming Guide".
6. Averaged over ten frequencies selected to capture the minimum and maximum performance values over 47 to 1002 MHz. Guaranteed by production test.
7. Performed with AGC frozen at maximum RF gain and minimum IF gain (zero RF gain backoff) using 6 MHz channel spacing. Min values measured at worst case frequencies.
8. Attenuation of on-chip brickwall filter from RFIN to DLIF output, relative to a tone at center of desired channel (N). Refer to Figure 7 on page 21 for a typical representation of the frequency response.
9. Guaranteed by characterization.
10. DTV modes. At offsets under 1 kHz, the LO phase noise is dependent on the crystal or RCLK. Measured with KDS crystal "AT-49 24.0000 MHz, ± 25 ppm, Cload = 8 pF."
11. Tested with recommended cable BOM per "AN468: Si217x Distortion Performance with Optimized Return Loss".
12. Measured at DLIF_P/N pins.

Table 5. Analog TV Receiver Characteristics[1]

(V_H = 3.3 V, V_L = 1.8 V, V_D = 1.8 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
System Performance (Tuner and Demodulator, End-to-End)						
Sensitivity for 30 dB Unweighted Video SNR[2,3]	SENS	M/N	—	–67.5	–65.5	dBm
		B/G, D/K	—	–67	–65	dBm
		I	—	–66	–64	dBm
		L/L'	—	–68	–66	dBm
Unweighted Video SNR[2,4]	$VSNR_u$	input level = –39 dBm; M/N	52.5	54	—	dB
		input level = –39 dBm; B/G, D/K	52	53.5	—	dB
		input level = –39 dBm; I	51	52.5	—	dB
		input level = –39 dBm; L/L'	53.5	55	—	dB
		input level = +1 dBm; M/N	54	55.5	—	dB
		input level = +1 dBm; B/G, D/K	53.5	55	—	dB
		input level = +1 dBm; I	52.5	53.5	—	dB
		input level = +1 dBm; L/L'	55	56.5	—	dB

Notes:

1. Measured on the Si2173-EVB at the output of external emitter followers which buffer the CVBS and SIF/AF pins and drive 75 Ω loads. Unless otherwise stated, RF input power is -39 dBm, residual carrier is 10% for PAL/SECAM (except L/L'), 12.5% for NTSC and 3% for SECAM L/L'; referenced to the F-connector input of the Si2173 reference design and includes all losses from connector, balun, and PCB, and Z_{SOURCE} = 75 Ω. Refer to "AN501: Si2173 Programming Guide" for programmable ranges.
2. Guaranteed by characterization.
3. For 30 dB unweighted video SNR at CVBS with max gain. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
4. Single channel, no blockers present. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
5. Weighted per CCIR 567
6. With default video filters. Where applicable, with group delay pre-correction per ITU BT.470-6 for systems M/N and B/G.
7. Single channel, no blockers present. Carrier error < $f_{carroff}$ x 90%.
8. Guaranteed by design.
9. Relative to 87.5% modulation depth for stable picture. Input signal is a black-to-white ramp. P/S_1 = 13 dB, P/S_2 = 20 dB (where applicable). Modulator input sync levels and white levels are: (input level) = (nominal level) x (OM%).
10. Relative to center of SIF band, where applicable. SIF filters configured for default (400%) FM overmodulation. Lower stop band from DC to color carrier. Upper stop band above N+1 picture carrier.
11. CVBS pin connected directly to AV processor.
12. CVBS pin to 75 Ω. buffer. Swing is programmable to compensate for voltage loss/gain in driver chain. Various buffering schemes are supported. Refer to "AN413: Si217x Layout and Design Guidelines" for details.
13. Variation due to process and temperature. Valid for standard modulation depths of 87.5% (system M), 90% (systems B/G, D/K), 80% (system I), 95% (system L/L'), and default video filter ATV_VIDEO_EQUALIZER setting. Measured at the output of the Si2173 CVBS pin.
14. SIF/AF pin. For SIF mode, directly connected to AV/sound processor. For AF mode, connected to 75 Ω. buffer.
15. Can support higher value in AF mode.

Table 5. Analog TV Receiver Characteristics[1] (Continued)

(V_H = 3.3 V, V_L = 1.8 V, V_D = 1.8 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Weighted Video SNR[2,4,5]	$VSNR_W$	input level = –39 dBm; M/N	57	60	—	dB
		input level = –39 dBm; L/L'	60	63	—	dB
		input level = –39 dBm; B/G, D/K	58	61.5	—	dB
		input level = –39 dBm; I	57.5	60.5	—	dB
		input level = +1 dBm; M/N	58.5	61	—	dB
		input level = +1 dBm; L/L'	62	64.5	—	dB
		input level = +1 dBm; B/G, D/K	59	62.5	—	dB
		input level = +1 dBm; I	58	61	—	dB
sin x/x Gain Response Error[2,6]		M/N; 100 kHz to 3.58 MHz	–1.5	±0.5	+0.7	dB
		other than M/N; 100 kHz - 4.43 MHz	–1.5	±0.5	+0.7	dB
sin x/x Group Delay Error[2,6]		M/N; 100 kHz to 3.58 MHz	—	±30	±70	ns
		other than M/N; 100 kHz - 4.43 MHz	—	±30	±50	ns

Notes:

1. Measured on the Si2173-EVB at the output of external emitter followers which buffer the CVBS and SIF/AF pins and drive 75 Ω loads. Unless otherwise stated, RF input power is -39 dBm, residual carrier is 10% for PAL/SECAM (except L/L'), 12.5% for NTSC and 3% for SECAM L/L'; referenced to the F-connector input of the Si2173 reference design and includes all losses from connector, balun, and PCB, and Z_{SOURCE} = 75 Ω. Refer to "AN501: Si2173 Programming Guide" for programmable ranges.
2. Guaranteed by characterization.
3. For 30 dB unweighted video SNR at CVBS with max gain. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
4. Single channel, no blockers present. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
5. Weighted per CCIR 567
6. With default video filters. Where applicable, with group delay pre-correction per ITU BT.470-6 for systems M/N and B/G.
7. Single channel, no blockers present. Carrier error < $f_{carroff}$ x 90%.
8. Guaranteed by design.
9. Relative to 87.5% modulation depth for stable picture. Input signal is a black-to-white ramp. P/S_1 = 13 dB, P/S_2 = 20 dB (where applicable). Modulator input sync levels and white levels are: (input level) = (nominal level) x (OM%).
10. Relative to center of SIF band, where applicable. SIF filters configured for default (400%) FM overmodulation. Lower stop band from DC to color carrier. Upper stop band above N+1 picture carrier.
11. CVBS pin connected directly to AV processor.
12. CVBS pin to 75 Ω. buffer. Swing is programmable to compensate for voltage loss/gain in driver chain. Various buffering schemes are supported. Refer to "AN413: Si217x Layout and Design Guidelines" for details.
13. Variation due to process and temperature. Valid for standard modulation depths of 87.5% (system M), 90% (systems B/G, D/K), 80% (system I), 95% (system L/L'), and default video filter ATV_VIDEO_EQUALIZER setting. Measured at the output of the Si2173 CVBS pin.
14. SIF/AF pin. For SIF mode, directly connected to AV/sound processor. For AF mode, connected to 75 Ω. buffer.
15. Can support higher value in AF mode.

Table 5. Analog TV Receiver Characteristics[1] (Continued)

(V_H = 3.3 V, V_L = 1.8 V, V_D = 1.8 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog TV Demodulator—Video						
Video Carrier Lock Range	$f_{carroff}$	Programmable range	—	±0.1,±0.5, ±1, ±2	—	MHz
Video Carrier Lock Time[2,7]	T_L	M/N, B/G, D/K, I	—	100	150	ms
		L/L'	—	100	175	ms
Attenuation of 1st Sound Carrier (±60 kHz)[8]	α_{SC1}	M/N	45	—	—	dB
		B/G, D/K, I, L/L'	50	—	—	dB
Attenuation of 2nd Sound Carrier (±60 kHz)[8]	α_{SC2}	M (Korea), B/G, D/K, I, L/L'	50	—	—	dB
Differential Gain[2]	G_{diff}	M;at CVBS pin;NTSC 7 Composite	—	±1	±1.5	%
Differential Phase[2]	ϕ_{diff}	M;at CVBS pin;NTSC 7 Composite	—	±0.5	±1.5	°
Overmodulation Tolerance[2,9]	OM	M/N, B/G, D/K, I	140	147	—	%

Notes:

1. Measured on the Si2173-EVB at the output of external emitter followers which buffer the CVBS and SIF/AF pins and drive 75 Ω loads. Unless otherwise stated, RF input power is -39 dBm, residual carrier is 10% for PAL/SECAM (except L/L'), 12.5% for NTSC and 3% for SECAM L/L'; referenced to the F-connector input of the Si2173 reference design and includes all losses from connector, balun, and PCB, and Z_{SOURCE} = 75 Ω. Refer to "AN501: Si2173 Programming Guide" for programmable ranges.
2. Guaranteed by characterization.
3. For 30 dB unweighted video SNR at CVBS with max gain. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
4. Single channel, no blockers present. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
5. Weighted per CCIR 567
6. With default video filters. Where applicable, with group delay pre-correction per ITU BT.470-6 for systems M/N and B/G.
7. Single channel, no blockers present. Carrier error < $f_{carroff}$ x 90%.
8. Guaranteed by design.
9. Relative to 87.5% modulation depth for stable picture. Input signal is a black-to-white ramp. P/S_1 = 13 dB, P/S_2 = 20 dB (where applicable). Modulator input sync levels and white levels are: (input level) = (nominal level) x (OM%).
10. Relative to center of SIF band, where applicable. SIF filters configured for default (400%) FM overmodulation. Lower stop band from DC to color carrier. Upper stop band above N+1 picture carrier.
11. CVBS pin connected directly to AV processor.
12. CVBS pin to 75 Ω. buffer. Swing is programmable to compensate for voltage loss/gain in driver chain. Various buffering schemes are supported. Refer to "AN413: Si217x Layout and Design Guidelines" for details.
13. Variation due to process and temperature. Valid for standard modulation depths of 87.5% (system M), 90% (systems B/G, D/K), 80% (system I), 95% (system L/L'), and default video filter ATV_VIDEO_EQUALIZER setting. Measured at the output of the Si2173 CVBS pin.
14. SIF/AF pin. For SIF mode, directly connected to AV/sound processor. For AF mode, connected to 75 Ω. buffer.
15. Can support higher value in AF mode.

Table 5. Analog TV Receiver Characteristics[1] (Continued)

(V_H = 3.3 V, V_L = 1.8 V, V_D = 1.8 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Video Bandwidth (3 dB)[2,6]	BW_{V3}	M/N	3.9	4.0	4.1	MHz
		B/G	4.7	4.8	4.9	MHz
		D/K	—	5.0	—	MHz
		I	—	5.3	—	MHz
		L/L'	—	5.0	—	MHz
Equalizer Chroma Peaking	EQ	programmable (approx. 1 dB steps)	—	–8 to +7	—	dB
2T K Factor[2,6]	K_{2T}		—	1	2	%
ATV RSSI Measurement Accuracy	$RSSI_A$	Only valid with ATV locked; input between –5 dB and –75 dBm; read 400 ms after demod lock	—	±3	—	dB

Notes:

1. Measured on the Si2173-EVB at the output of external emitter followers which buffer the CVBS and SIF/AF pins and drive 75 Ω loads. Unless otherwise stated, RF input power is -39 dBm, residual carrier is 10% for PAL/SECAM (except L/L'), 12.5% for NTSC and 3% for SECAM L/L'; referenced to the F-connector input of the Si2173 reference design and includes all losses from connector, balun, and PCB, and Z_{SOURCE} = 75 Ω. Refer to "AN501: Si2173 Programming Guide" for programmable ranges.
2. Guaranteed by characterization.
3. For 30 dB unweighted video SNR at CVBS with max gain. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
4. Single channel, no blockers present. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
5. Weighted per CCIR 567
6. With default video filters. Where applicable, with group delay pre-correction per ITU BT.470-6 for systems M/N and B/G.
7. Single channel, no blockers present. Carrier error < $f_{carroff}$ x 90%.
8. Guaranteed by design.
9. Relative to 87.5% modulation depth for stable picture. Input signal is a black-to-white ramp. P/S_1 = 13 dB, P/S_2 = 20 dB (where applicable). Modulator input sync levels and white levels are: (input level) = (nominal level) x (OM%).
10. Relative to center of SIF band, where applicable. SIF filters configured for default (400%) FM overmodulation. Lower stop band from DC to color carrier. Upper stop band above N+1 picture carrier.
11. CVBS pin connected directly to AV processor.
12. CVBS pin to 75 Ω. buffer. Swing is programmable to compensate for voltage loss/gain in driver chain. Various buffering schemes are supported. Refer to "AN413: Si217x Layout and Design Guidelines" for details.
13. Variation due to process and temperature. Valid for standard modulation depths of 87.5% (system M), 90% (systems B/G, D/K), 80% (system I), 95% (system L/L'), and default video filter ATV_VIDEO_EQUALIZER setting. Measured at the output of the Si2173 CVBS pin.
14. SIF/AF pin. For SIF mode, directly connected to AV/sound processor. For AF mode, connected to 75 Ω. buffer.
15. Can support higher value in AF mode.

Table 5. Analog TV Receiver Characteristics[1] (Continued)

(V_H = 3.3 V, V_L = 1.8 V, V_D = 1.8 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Analog TV Demodulator—Sound (SIF)[8, 10]						
SIF Bandwidth (20 dB)	BW_{SIF20}	M, BTSC/EIAJ	—	510	—	kHz
		M, A2; B, A2	—	850	—	kHz
		B, NICAM	—	920	—	kHz
		G, A2	—	880	—	kHz
		G, NICAM	—	950	—	kHz
		D/K, NICAM; L, NICAM	—	1.19	—	MHz
		D/K, A2 (SC_2; P/S_2 = 6.258 MHz)	—	860	—	kHz
		D/K, A2 (SC_2; P/S_2 = 6.742 MHz)	—	840	—	kHz
		D/K, A2 (SC_2; P/S_2 = 5.742 MHz)	—	1.24	—	MHz
		I, NICAM	—	1.21	—	kHz
Stop Band Attenuation	α_{stop}	M, A2 and B, A2: lower stop band	47	—	—	dB
		all other standards: lower stop band; all standards: upper stop band	50	—	—	dB
Attenuation at Picture Carrier	$\alpha_{PC(N)}$		70	—	—	dB

Notes:

1. Measured on the Si2173-EVB at the output of external emitter followers which buffer the CVBS and SIF/AF pins and drive 75 Ω loads. Unless otherwise stated, RF input power is -39 dBm, residual carrier is 10% for PAL/SECAM (except L/L'), 12.5% for NTSC and 3% for SECAM L/L'; referenced to the F-connector input of the Si2173 reference design and includes all losses from connector, balun, and PCB, and Z_{SOURCE} = 75 Ω. Refer to "AN501: Si2173 Programming Guide" for programmable ranges.
2. Guaranteed by characterization.
3. For 30 dB unweighted video SNR at CVBS with max gain. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
4. Single channel, no blockers present. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
5. Weighted per CCIR 567
6. With default video filters. Where applicable, with group delay pre-correction per ITU BT.470-6 for systems M/N and B/G.
7. Single channel, no blockers present. Carrier error < $f_{carroff}$ x 90%.
8. Guaranteed by design.
9. Relative to 87.5% modulation depth for stable picture. Input signal is a black-to-white ramp. P/S_1 = 13 dB, P/S_2 = 20 dB (where applicable). Modulator input sync levels and white levels are: (input level) = (nominal level) x (OM%).
10. Relative to center of SIF band, where applicable. SIF filters configured for default (400%) FM overmodulation. Lower stop band from DC to color carrier. Upper stop band above N+1 picture carrier.
11. CVBS pin connected directly to AV processor.
12. CVBS pin to 75 Ω. buffer. Swing is programmable to compensate for voltage loss/gain in driver chain. Various buffering schemes are supported. Refer to "AN413: Si217x Layout and Design Guidelines" for details.
13. Variation due to process and temperature. Valid for standard modulation depths of 87.5% (system M), 90% (systems B/G, D/K), 80% (system I), 95% (system L/L'), and default video filter ATV_VIDEO_EQUALIZER setting. Measured at the output of the Si2173 CVBS pin.
14. SIF/AF pin. For SIF mode, directly connected to AV/sound processor. For AF mode, connected to 75 Ω. buffer.
15. Can support higher value in AF mode.

Table 5. Analog TV Receiver Characteristics[1] (Continued)

(V_H = 3.3 V, V_L = 1.8 V, V_D = 1.8 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Attenuation at Color Carrier	α_{CC}	B, A2	48	—	—	dB
		G, A2	51	—	—	dB
		M, A2	47	—	—	dB
		all other standards	55	—	—	dB
Attenuation at Adjacent Picture Carrier	$\alpha_{PC(N+1)}$		55	—	—	dB
Carrier to Noise Ratio	CNR_{SC1}	G, NICAM; SC_1; P/S_1 = 13 dB; P = -30 dBm; F_{pc} = 62.25 MHz; BW_{noise} = 130 kHz; colorbar	—	57	—	dB
	CNR_{SC2}	G, NICAM; SC_2; P/S_2 = 13 dB; P = -30 dBm; F_{pc} = 62.25 MHz; BW_{noise} = 384 kHz; CW	—	51	—	dB
Out-of-band Spurious	S_{OOB}		40	—	—	dBr

Notes:

1. Measured on the Si2173-EVB at the output of external emitter followers which buffer the CVBS and SIF/AF pins and drive 75 Ω loads. Unless otherwise stated, RF input power is -39 dBm, residual carrier is 10% for PAL/SECAM (except L/L'), 12.5% for NTSC and 3% for SECAM L/L'; referenced to the F-connector input of the Si2173 reference design and includes all losses from connector, balun, and PCB, and Z_{SOURCE} = 75 Ω. Refer to "AN501: Si2173 Programming Guide" for programmable ranges.
2. Guaranteed by characterization.
3. For 30 dB unweighted video SNR at CVBS with max gain. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
4. Single channel, no blockers present. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
5. Weighted per CCIR 567
6. With default video filters. Where applicable, with group delay pre-correction per ITU BT.470-6 for systems M/N and B/G.
7. Single channel, no blockers present. Carrier error < $f_{carroff}$ x 90%.
8. Guaranteed by design.
9. Relative to 87.5% modulation depth for stable picture. Input signal is a black-to-white ramp. P/S_1 = 13 dB, P/S_2 = 20 dB (where applicable). Modulator input sync levels and white levels are: (input level) = (nominal level) x (OM%).
10. Relative to center of SIF band, where applicable. SIF filters configured for default (400%) FM overmodulation. Lower stop band from DC to color carrier. Upper stop band above N+1 picture carrier.
11. CVBS pin connected directly to AV processor.
12. CVBS pin to 75 Ω. buffer. Swing is programmable to compensate for voltage loss/gain in driver chain. Various buffering schemes are supported. Refer to "AN413: Si217x Layout and Design Guidelines" for details.
13. Variation due to process and temperature. Valid for standard modulation depths of 87.5% (system M), 90% (systems B/G, D/K), 80% (system I), 95% (system L/L'), and default video filter ATV_VIDEO_EQUALIZER setting. Measured at the output of the Si2173 CVBS pin.
14. SIF/AF pin. For SIF mode, directly connected to AV/sound processor. For AF mode, connected to 75 Ω. buffer.
15. Can support higher value in AF mode.

Table 5. Analog TV Receiver Characteristics[1] (Continued)

(V_H = 3.3 V, V_L = 1.8 V, V_D = 1.8 V, T_A = –20 to 85 °C)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
CVBS Output Driver						
Output Signal Voltage Swing	V_{CVBS}	sync-tip to white[11]	0.922	0.97	1.019	V_{pp}
		sync-tip to white[12]	—	2	—	V_{pp}
		white clipping level[12]	—	2.3	—	V_{pp}
CVBS Output Level Variation[2,13]	$V_{CVBSVAR}$	sync-tip to white	–5	—	5	%
DC Output Voltage	V_{DC}		—	1.5	—	V
Load Resistance	R_L		1	—	—	kΩ
Load Capacitance	C_L		—	—	15	pF
SIF/AF Output Driver[14]						
Output Signal Voltage Swing	V_{SIF}	programmable	—	0.5 to 2.0	—	V_{pp}
DC Output Voltage	V_{DC}		—	1.5	—	V
Load Resistance	R_L		1	—	—	kΩ
Load Capacitance[15]	C_L		—	—	15	pF

Notes:

1. Measured on the Si2173-EVB at the output of external emitter followers which buffer the CVBS and SIF/AF pins and drive 75 Ω loads. Unless otherwise stated, RF input power is -39 dBm, residual carrier is 10% for PAL/SECAM (except L/L'), 12.5% for NTSC and 3% for SECAM L/L'; referenced to the F-connector input of the Si2173 reference design and includes all losses from connector, balun, and PCB, and Z_{SOURCE} = 75 Ω. Refer to "AN501: Si2173 Programming Guide" for programmable ranges.
2. Guaranteed by characterization.
3. For 30 dB unweighted video SNR at CVBS with max gain. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
4. Single channel, no blockers present. Rohde & Schwarz VSA low-pass filter enabled and high-pass filter disabled. Averaged over ten frequencies over 54 to 891 MHz.
5. Weighted per CCIR 567
6. With default video filters. Where applicable, with group delay pre-correction per ITU BT.470-6 for systems M/N and B/G.
7. Single channel, no blockers present. Carrier error < $f_{carroff}$ x 90%.
8. Guaranteed by design.
9. Relative to 87.5% modulation depth for stable picture. Input signal is a black-to-white ramp. P/S_1 = 13 dB, P/S_2 = 20 dB (where applicable). Modulator input sync levels and white levels are: (input level) = (nominal level) x (OM%).
10. Relative to center of SIF band, where applicable. SIF filters configured for default (400%) FM overmodulation. Lower stop band from DC to color carrier. Upper stop band above N+1 picture carrier.
11. CVBS pin connected directly to AV processor.
12. CVBS pin to 75 Ω. buffer. Swing is programmable to compensate for voltage loss/gain in driver chain. Various buffering schemes are supported. Refer to "AN413: Si217x Layout and Design Guidelines" for details.
13. Variation due to process and temperature. Valid for standard modulation depths of 87.5% (system M), 90% (systems B/G, D/K), 80% (system I), 95% (system L/L'), and default video filter ATV_VIDEO_EQUALIZER setting. Measured at the output of the Si2173 CVBS pin.
14. SIF/AF pin. For SIF mode, directly connected to AV/sound processor. For AF mode, connected to 75 Ω. buffer.
15. Can support higher value in AF mode.

Table 6. Reset Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
RSTB Pulse Width	t_{SRST}	100	—	—	µs

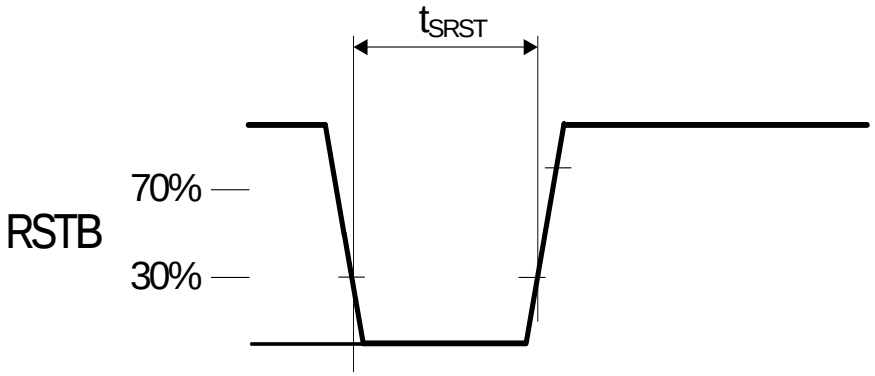


Figure 1. Reset Timing Parameter

Table 7. Control Interface Timing Characteristics[1,2]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCL Frequency	f_{SCL}		0	—	400	kHz
SCL Low Time	t_{LOW}		1.3	—	—	µs
SCL High Time	t_{HIGH}		0.6	—	—	µs
SCL Input to SDA↓ Setup (START)	$t_{SU:STA}$		0.6	—	—	µs
SCL Input to SDA↓ Hold (START)	$t_{HD:STA}$		0.6	—	—	µs
SDA Input to SCL↑ Setup	$t_{SU:DAT}$		100	—	—	ns
SDA Input to SCL↓ Hold[3,4]	$t_{HD:DAT}$		0	—	900	ns
SCL input to SDA↑ Setup (STOP)	$t_{SU:STO}$		0.6	—	—	µs
STOP to START Time	t_{BUF}		1.3	—	—	µs
SDA Input, SCL Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		—	—	300	ns
SDA Output Fall Time	$t_{f:OUT}$		—	—	250	ns
SDA Capacitive Load	C_b		—	—	50	pF
Input Filter Pulse Suppression	t_{SP}		—	—	50	ns

Notes:

1. The user must ensure that an I^2C start condition (falling edge of SDA while SCL is high) does not occur within 300 ns before the rising edge of RSTB.
2. The user must ensure that SCL is high during the rising edge of RSTB and stays high until after the first start condition.
3. The Si2173 delays SDA by a minimum of 300 ns from the V_{IH} threshold of SCL to comply with the minimum $t_{HD:DAT}$ specification.
4. The maximum $t_{HD:DAT}$ has only to be met when f_{SCL} = 400 kHz. At frequencies below 400 kHz, $t_{HD:DAT}$ may be violated as long as all other timing parameters are met.

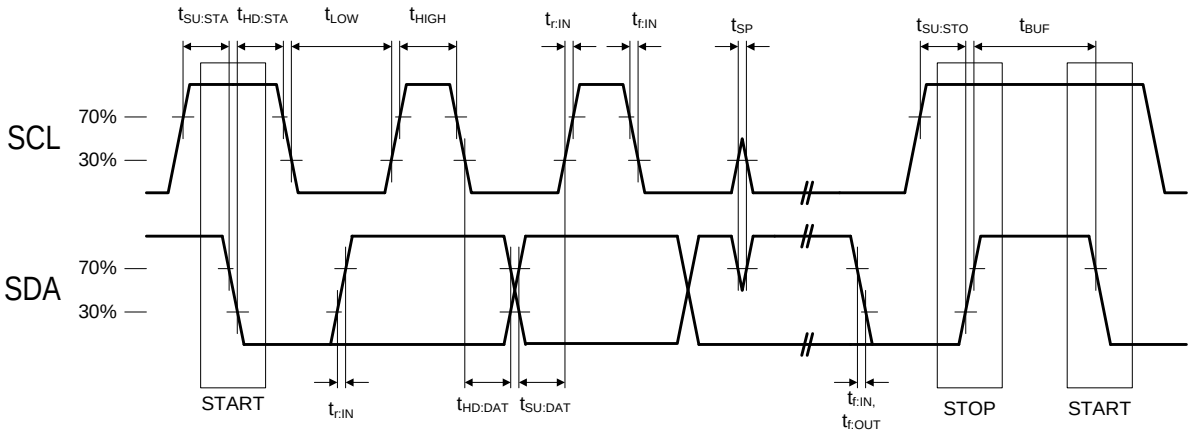


Figure 2. Control Interface Read and Write Timing Parameters

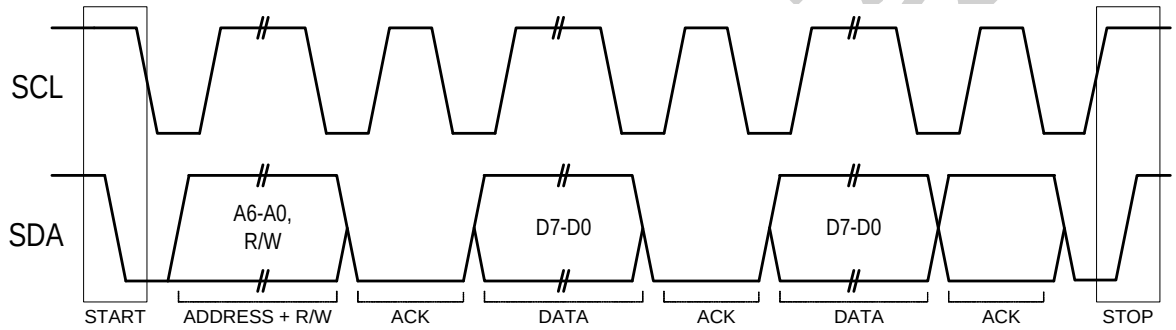


Figure 3. Control Interface Read and Write Timing Diagram

Table 8. Crystal Oscillator and Output Clocks Characteristics

Parameter[1]	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Oscillator Frequency	f_{OSC}		—	24	—	MHz
BCLK Output Frequency[2]	f_{BCLK}		—	24	—	MHz
BCLK Output Amplitude	V_{BCLK}		—	600	—	mVpp
XOUT Output Frequency[3]	f_{XOUT}		—	24	—	MHz
RCLK Input Frequency[3]	f_{RCLK}		—	24	—	MHz
RCLK Frequency Tolerance[4]	f_{RCLK}		–100	—	100	ppm
RCLK Input Amplitude	V_{RCLK}	Sinusoidal clock	—	400 to 600	—	mVpp
RCLK Jitter[4, 5]	J_{RCLK}	125 Hz to 12 MHz	—	—	1.7	ps rms
RCLK Input Capacitance	C_{RCLK}		—	8	—	pF

Notes:

1. Refer to "AN413: Si217x Layout and Design Guidelines" for details regarding clock schemes and requirements.
2. The BCLK signal is sinusoidal, with swing approximately 600 mVpp (depends on loading). When the Si2165 Multi-Standard DVB-T/C Demodulator is used, BCLK of the Si2173 should drive the RSSI_ADC pin of the Si2165. In this case, no crystal is needed for the Si2165.
3. For the case of dual Si2173 tuners, the XOUT pin of the primary Si2173 can drive the XTAL_I pin of the secondary Si2173 (RCLK function). In this case, no crystal is needed for the secondary Si2173.
4. Specifications for external clock source.
5. Total jitter on RCLK should be lower than 1.7 ps rms for less than 1 dB impact on synthesizer total phase noise.

2. Typical Application Schematics

Refer to "AN413: Si217x Layout and Design Guidelines" for additional details on application schematics, bill of materials, and design/PCB guidelines.

2.1. Typical Hybrid TV Tuner Application

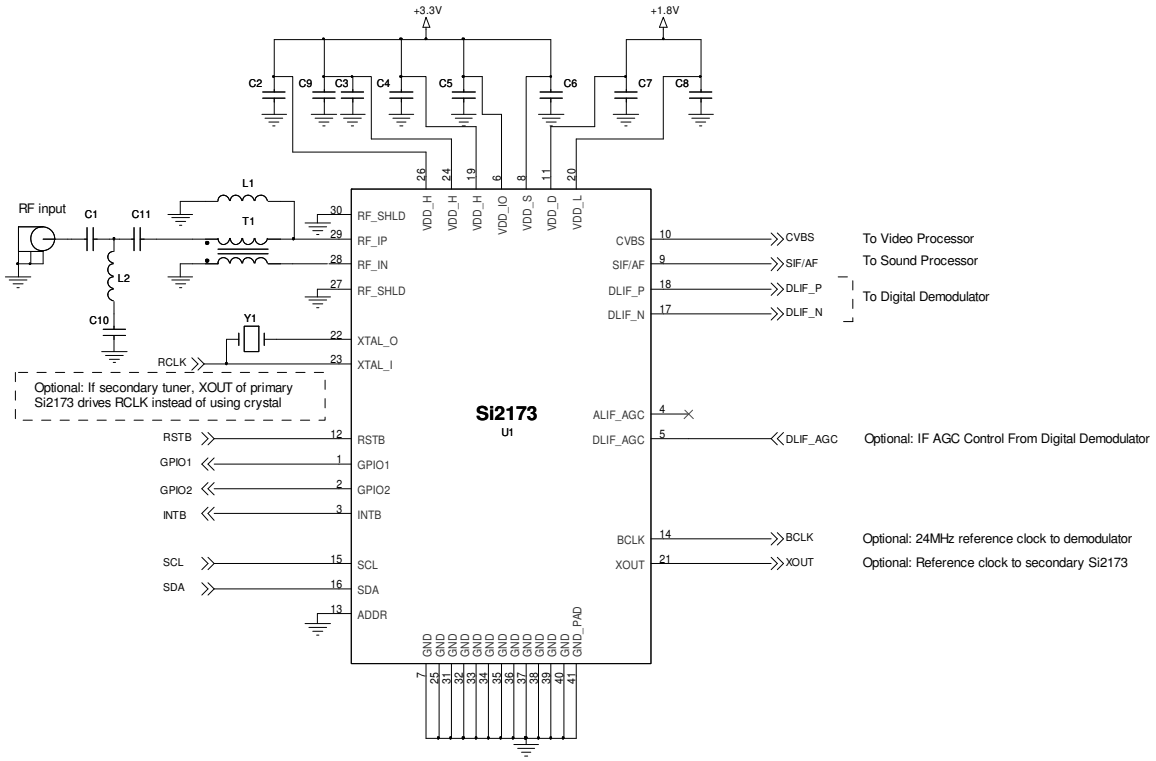
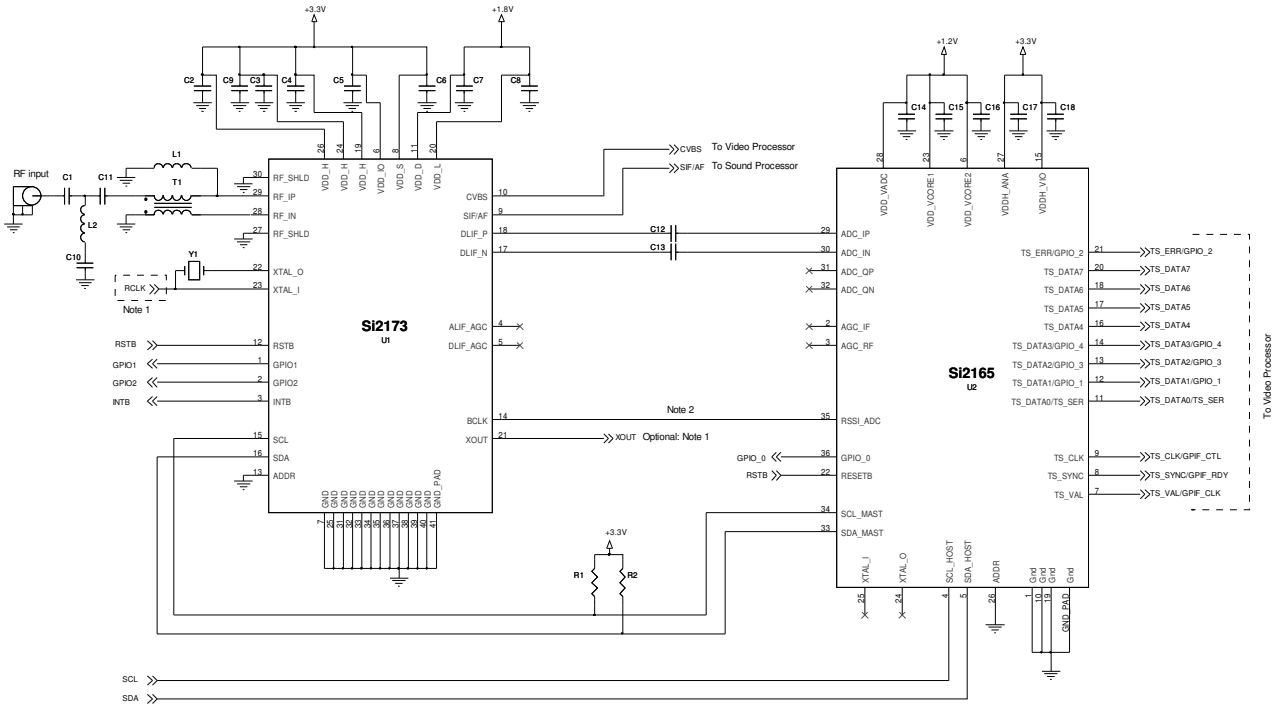


Figure 4. Hybrid TV Tuner Application Schematic

Table 9. Hybrid TV Tuner Application Bill of Materials

Component(s)	Description	Supplier(s)
C1	Capacitor, 470 pF, ±20%, COG	Various
C2, C4, C5, C6, C7, C8	Capacitor, 1.2 nF, ±20%, X7R	Various
C3	Capacitor, 4.7 nF, ±20%, X7R	Various
C9	Capacitor, 100 nF, ±20%, X7R	Various
C10	Capacitor, 120 pF, ±5%, COG	Various
C11	Capacitor, 82 pF, ±5%, COG	Various
L1	Multilayer chip inductor, 220 nH, 4 Ω (dc, max)	Various
L2	Wirewound inductor, 270 nH, ±5%	Various
T1	Balun, unbalanced to balanced, 1:1	Murata or Sunlord
Y1	24 MHz crystal, 8 pF C_{LOAD}	Various
U1	Si2173 Worldwide Hybrid TV Tuner with Analog Demodulator	Silicon Laboratories

2.2. Hybrid TV Receiver Application Using the Si2165 DVB-T/C Demodulator



Note 1: For the case of dual Si2173 tuners, the XOUT pin of the primary Si2173 can drive the XTAL_I pin of the secondary Si2173 (RCLK input).
Note 2: For Si2173 + Si2165 designs, the Si2165 receives its clock on the RSSI_ADC pin from the Si2173 BCLK pin.

Figure 5. Hybrid TV Receiver Application Schematic (Using the Si2165)

Table 10. Hybrid TV Receiver Application Bill of Materials (Using the Si2165)

Component(s)	Description	Supplier(s)
C1	Capacitor, 470 pF, ±20%, COG	Various
C2, C4, C5, C6, C7, C8	Capacitor, 1.2 nF, ±20%, X7R	Various
C3	Capacitor, 4.7 nF, ±20%, X7R	Various
C9, C12, C13, C14, C15, C16, C17, C18	Capacitor, 100 nF, ±20%, X7R	Various
C10	Capacitor, 120 pF, ±5%, COG	Various
C11	Capacitor, 82 pF, ±5%, COG	Various
L1	Multi-layer chip inductor, 220 nH, 4 Ω (dc, max)	Various
L2	Wirewound inductor, 270 nH, ±5%	Various
R1, R2	Pull-up resistors, 4.7 kΩ, ±5%	Various
T1	Balun, unbalanced to balanced, 1:1	Murata or Sunlord
Y1	24 MHz crystal, 8 pF C_{LOAD}	Various
U1	Si2173 Worldwide Hybrid TV Tuner with Analog Demodulator	Silicon Laboratories
U2	Si2165 Multi-Standard DVB-T/C Demodulator	Silicon Laboratories

3. Functional Description

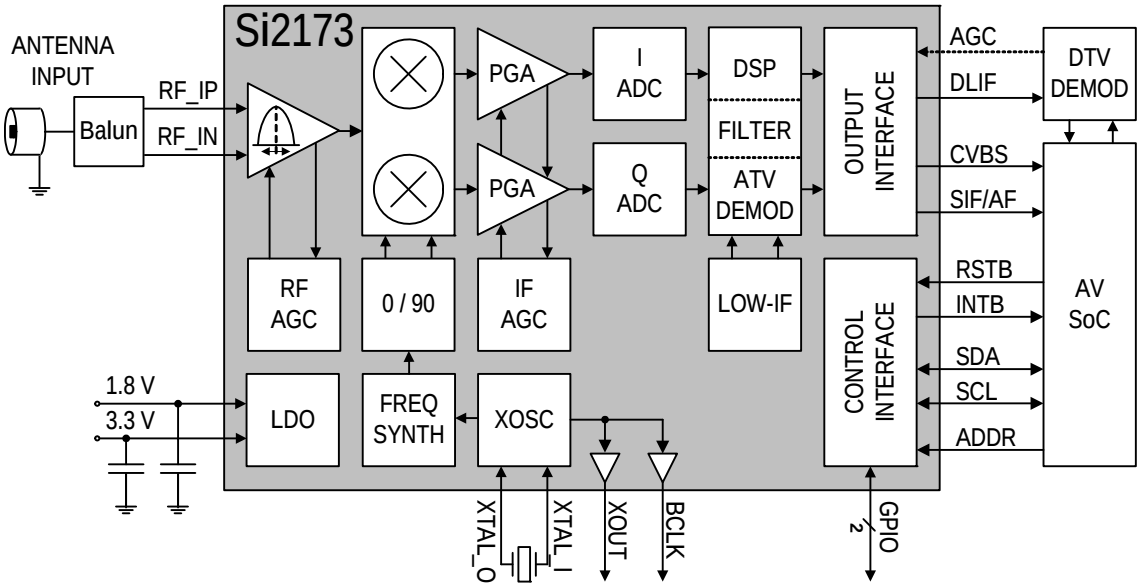


Figure 6. Functional Block Diagram

3.1. Overview

The Si2173 is a mixed-signal IC which integrates a complete hybrid tuner with analog TV demodulator supporting all worldwide analog and digital standards for terrestrial and cable broadcast applications. Leveraging Silicon Labs' proven digital low-IF architecture, the Si2173 achieves unmatched performance while minimizing design complexity and cost. No external LNAs, tracking filters, or SAW filters are used. The Si2173 is the industry's first silicon tuner to exceed the performance of traditional MOPLL-based tuners, delivering superior picture quality and a higher number of received stations in real-world, crowded spectrum conditions.

Interfacing the Si2173 seamlessly with the Si2165 DVB-T/C demodulator creates a complete terrestrial and cable hybrid PAL/SECAM and DVB-T/C receiver.

3.2. Tuner

The RF front-end is optimized for high linearity and low noise to achieve superior performance in real-world, crowded spectrum conditions. The differential-input LNA is driven by a low-cost external balun and works in conjunction with an automatically-tuned, integrated, high-Q tracking filter and RF AGC to provide gain only within the passband of the tracking filter and minimize desensitization in the presence of strong out-of-band interferers. The tracking filter is automatically tuned for consistent performance across the RF input frequency range, temperature, aging, and component variation.

A fully-integrated frequency synthesizer generates a quadrature local oscillator for the harmonic and image reject mixer, which downconverts the filtered RF input signal to a low-IF of approximately 3 MHz. All low-IF processing and channel filtering is performed on-chip, eliminating the need for external SAW filters. The final channel filter is implemented with digital signal processing (DSP) and is programmable for compliance to worldwide broadcast standards. The Video Filter Tool (VFT) enables rapid customization of the integrated channel filter response through an easy-to-use GUI application. Refer to the "Si217x Video Filter Tool User's Guide" for details. The default filter responses for ASTC/QAM, ISDB-T, DVB-T (7 MHz), DVB-T (8 MHz), and DTMB are shown in Figure 7.

The Si2173 autonomously controls RF and IF AGC to optimize dynamic range. The time constants are selectable to support various AGC speeds. The digital TV low IF output amplitude at the DLIF pins is software programmable. Alternatively, if the digital demodulator requires the tuner to close its AGC loop, the LIF output amplitude can be adjusted with an optional external analog input on the DLIF_AGC pin.

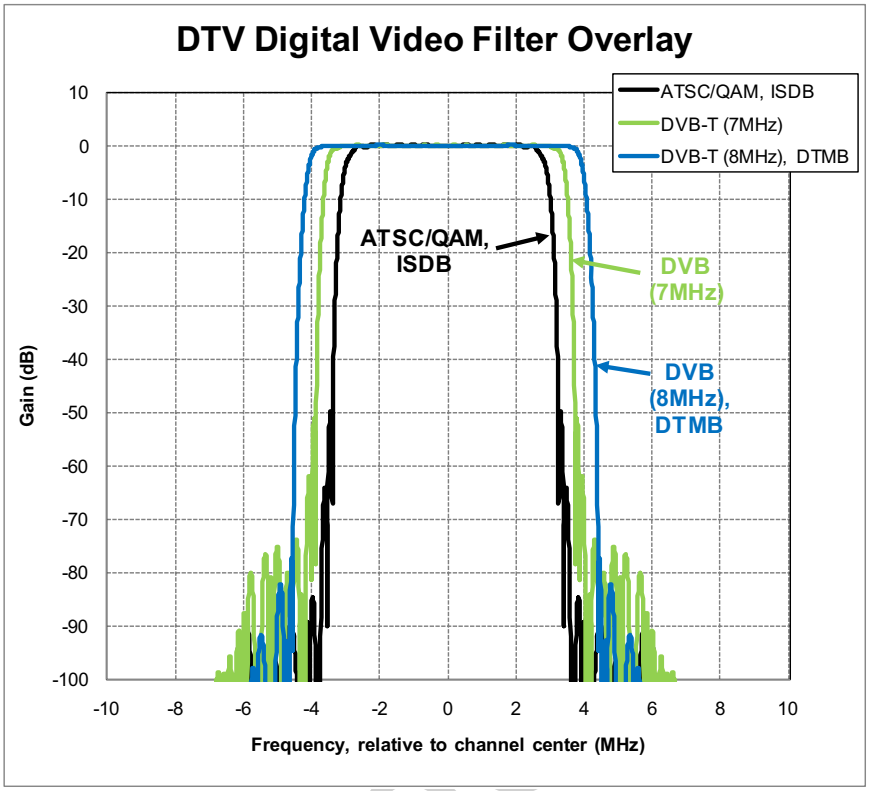


Figure 7. Integrated Channel Filters (Eliminate External IF SAW Filters)

3.3. Reference Clock Generation

The Si2173 creates its own reference clock with an integrated crystal oscillator, which requires only a low-cost 24 MHz crystal. Discrete tuning capacitors should not be used on the PCB. Instead, software-programmable on-chip tuning capacitors center the crystal oscillator to compensate for different PCB parasitic capacitances.

For dual-tuner applications, the primary Si2173 can provide a reference clock on its XOUT pin directly to the XTAL_I pin of the secondary Si2173, thus saving the cost and PCB area of one crystal. A 24 MHz buffered output clock can be provided on the BCLK pin for use as a clock source to a digital demodulator or host processor.

3.4. ATV Demodulator

The Si2173 integrates a complete worldwide, multi-standard NTSC, PAL/SECAM ATV demodulator for positive and negative video modulation and AM and FM mono sound modulation.

The following worldwide standards are supported:

- Video: B/G, D/K, I, L/L' and M/N
- SIF audio: A2, NICAM + AM/FM mono, FM mono, wideband (overmodulated) FM, BTSC, EIAJ
- Mono audio demodulation: A2, AM mono, FM mono, wideband (overmodulated) FM, BTSC, EIAJ

CVBS video and SIF or AF mono sound outputs are provided for interfacing with an external A/V processor.

An on-chip equalizer provides programmable peaking in the CVBS frequency response, allowing for convenient adjustment of the relative chroma level.

The Video Filter Tool (VFT) enables rapid customization of end-to-end (RF to CVBS) video filter response per standard through an easy-to-use GUI application. Refer to the "Si217x Video Filter Tool User's Guide" for details.

Figure 8 shows the default digital filter responses for video and a subset of the available audio filters.

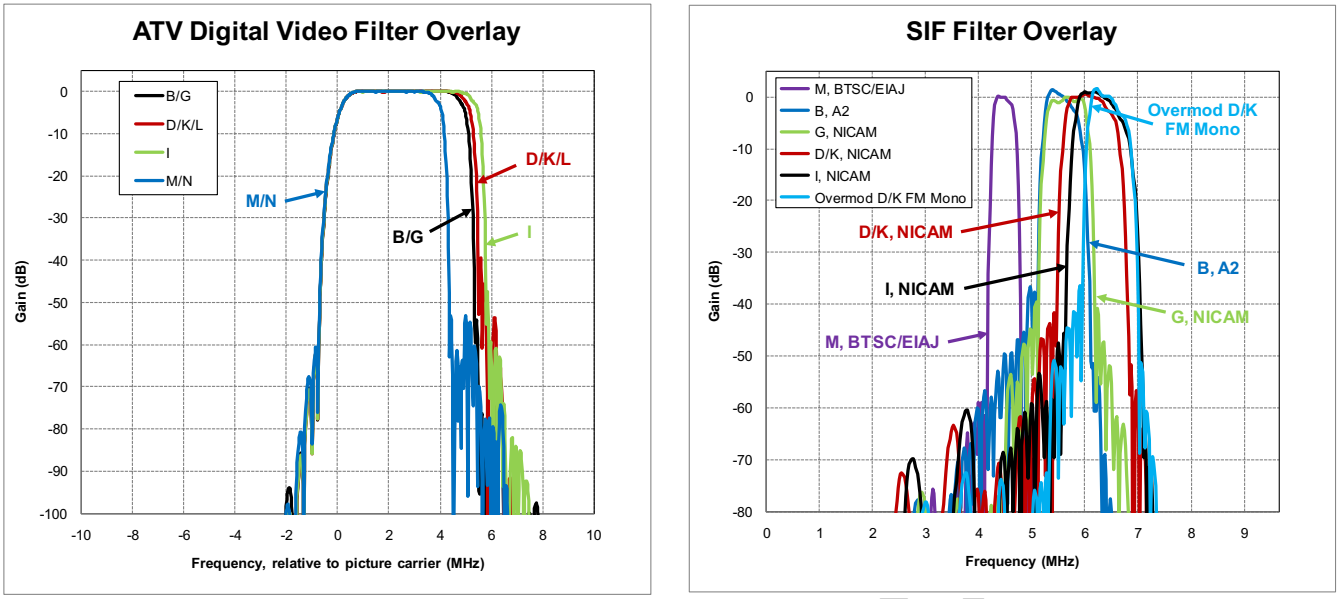


Figure 8. Analog TV Video and SIF Audio Filters (For Clarity, Only a Subset of All Audio Standards is Shown)

3.5. Output Interface

The output interface offers single-ended connections to an external A/V or host processor, demodulated video on the CVBS pin, and SIF or demodulated AF mono audio on the SIF/AF pin. For digital TV (DTV), the output interface offers low IF (LIF) differential connections to a DTV demodulator via the pins DLIF_P/DLIF_N.

3.6. Supply Voltages

The Si2173 has five internal supply domains. However, only two supply voltages are needed in most applications (1.8 and 3.3 V).

The analog portions of the device are powered by high and low voltage domains, V_{DD_H} and V_{DD_L}, respectively. The V_{DD_D} supply powers the digital core. The digital input/output interface supply, V_{DD_IO}, provides voltage to the RSTB, GPIO1, GPIO2, INTB, DLIF_AGC, and BCLK pins. The I^2C serial interface supply, V_{DD_S}, powers the SDA SCL pins.

The V_{DD_IO} and V_{DD_S} supplies may be connected to the host processor or digital demodulator supply voltage to save power and eliminate the need for voltage level translators. Alternatively, a single voltage regulator may be shared by the V_{DD_IO}, V_{DD_S}, and V_{DD_H} supplies (for instance 3.3 V). The supplies for V_{DD_L} and V_{DD_D} can also be shared (1.8 V). Until all supplies ramp up, the RSTB pin must remain low.

3.7. Control Interface

An I^2C serial interface is provided for configuration and monitoring of the chip. The Si2173 supports a 7-bit device addressing procedure. Individual data transfers to and from the device are 8-bits. The device always operates as a bus slave. In order for the I^2C interface to be active, the V_{DD_S} and V_{DD_D} supplies must be turned on.

The I^2C bus uses the serial clock line (SCL) and serial data line (SDA) pins. A transaction begins with the START condition, which occurs when SDA falls while SCL is high. Next, the user drives an 8-bit control word serially on SDA, which is captured by the device on rising edges of SCL. The control word consists of a seven bit device address followed by a read/write bit (read = 1, write = 0). The Si2173 acknowledges the control word by driving SDA low on the next falling edge of SCL.

The Si2173 responds to a single device address that can be changed with the ADDR pin. Four addresses are available, allowing up to four Si2173 devices to share the same I^2C serial bus. The 7-bit device address consists of a fixed part (5 MSBs) followed by a programmable 2-bit part. The LSB of the device address signals whether a read or write operation occurs.

The voltage on the ADDR pin is used to set the programmable 2-bit part of the device address. The ADDR pin embeds both internal pull-down and pull-up resistors to ground and V_{DD_H}. The various I^2C device addresses can be selected with a single external resistor as summarized in Table 11.

Table 11. I²C Device Address Selection

device_address[7:0]			External ADDR Termination
[7:3]	[2:1]	[0]	
11000	11	R = 1 W = 0	ADDR tied directly to V_{DD_H}
11000	10	R = 1 W = 0	ADDR tied to V_{DD_H} through 220 kΩ* pull-up
11000	01	R = 1 W = 0	ADDR tied to GND through 220 kΩ* pull-down
11000	00	R = 1 W = 0	ADDR tied directly to GND

*** Note:** 5% resistor tolerance is sufficient.

For write operations, the user then sends an 8-bit data byte on SDA, which is captured by the device on rising edges of SCL. The Si2173 acknowledges each data byte by driving SDA low for one cycle on the next falling edge of SCL. The user may write any number of data bytes in a single I²C transaction. The first byte is a command, and the next bytes are arguments.

For read operations, after the Si2173 has acknowledged the control byte, it drives an 8-bit data byte on SDA, changing the state of SDA on the falling edge of SCL. The user acknowledges each data byte by driving SDA low for one cycle, on the next falling edge of SCL. If a data byte is not acknowledged, the transaction ends. The user may read any number of data bytes in a single I²C transaction. These bytes contain the response data from the Si2173.

An I²C transaction ends with the STOP condition, which occurs when SDA rises while SCL is high.

The SDA and SCL pins do not include internal pull-up resistors and must always be pulled-high with external pull-up resistors to pin VDD_S.

The Si2173 I²C control bus (5 V compatible when V_{DD_S} = 5 V) implements a fast I²C interface (400 kHz). Since the internal I²C state machine runs from the SCL clock, there is no need for a high-speed clock. The I²C control interface always remains active, even if the device is in powerdown mode. However, only a few commands are accessible during powerdown mode. For further details on the command interface, see "4. Programming Interface Description" on page 24.

3.8. Programming Interface

The Si2173 uses a high level command API through the I²C serial interface (the physical layer in this case) to communicate with the host processor. This API is used instead of basic register reads/writes to control the device and set its operating modes. Details are provided in "4. Programming Interface Description" on page 24.

3.9. General Purpose Input/Output Pins

Two general-purpose input/output (GPIO) pins are provided and can be configured as a digital I/O port. The GPIO pins can be configured to output a constant low (0 V), constant high (V_{DD_IO}), or high impedance (high-Z).

3.10. Reset, Powerup, Powerdown, and Standby

Resetting and powering up the Si2173 is described in this section. The Si2173 can be placed into a hardware reset mode by holding the level on the RSTB pin to low. Reset mode disables the analog and digital circuitry, resets the registers to their default settings, and places I/O pins in output high-Z.

To take the Si2173 out of reset mode and into hardware powerdown mode, the RSTB pin should be set high after being held low for a minimum time of t_{SRST}. Refer to Figure 1, “Reset Timing Parameter,” on page 15. In hardware powerdown mode, the analog and digital circuitry is disabled, but certain blocks within the device remain active.

With the Si2173 in hardware powerdown mode, a specific powerup command must be issued over the programming interface to power up the device. At that point, the device can respond to subsequent commands.

To return to hardware powerdown, the RSTB pin can be toggled low and then high again. Alternatively, a powerdown command can place the device into a software powerdown mode, which is configurable for various levels of activity and power consumption. For instance, clock outputs can be selectively disabled.

The Si2173 also supports a software standby mode, which is entered from powerup mode. In standby mode, the LNA and clocks remain powered up while most of the chip is placed in a low power state. Output clocks BCLK and XOUT can be programmed on or off.

4. Programming Interface Description

The Si2173 provides a simple yet powerful software command API programming interface to program the various modes and blocks of the chip, reducing development time while offering maximum flexibility. The device is programmed using API commands.

4.1. Programming with Commands

To perform an action, the user writes a command OPCODE byte followed by its associated fields (packed in byte-sized arguments). This will cause the chip to execute the given command. Commands control actions, such as powering up the device, shutting down the device, or tuning to a channel. Fields are specific to a given command and are used to alter the behavior of the command. For example, the TUNER_TUNE_FREQ command uses fields to define the center frequency of the desired channel. Every command posts a response that can be retrieved to check the status. At a minimum, all commands provide a one-byte reply containing fields describing status information.

While commands issue immediate actions, static configuration information is set using properties. Properties modify the default chip operation, but immediate execution is not guaranteed. To set a property, the host needs to issue the SET_PROPERTY command, which will load the given property into the chip. This new property will subsequently be taken into account when the chip or another command requires the information related to that property.

An example of a property is DTV_MODE, which has a field that defines the channel bandwidth to be 6, 7, or 8 MHz.

A list of all commands and properties, their full descriptions, and their detailed usage is explained in the application note "AN501: Si2173 Programming Guide".

4.2. Conceptual Example of a Command

In order to illustrate the usage and format of a typical command, a conceptual example command, GENERIC_COMMAND, is described below (note that GENERIC_COMMAND is *not* an actual command). The format of this description of GENERIC_COMMAND shown below is similar to what is used in "AN501: Si2173 Programming Guide" for all commands and properties.

The 8-bit OPCODE of the command, GENERIC_COMMAND, is N. GENERIC_COMMAND contains three argument bytes and two response bytes. The three argument bytes contain four fields (FIELD_A, FIELD_B, FIELD_C, and FIELD_D) as shown in the “Command” table on page 25. The field definitions and values are described in the second table. The response for GENERIC_COMMAND contains a STATUS byte, which is always the same for all commands. The response contains two bytes (specific to GENERIC_COMMAND) in the form of two fields (FIELD_E and FIELD_F), as shown in the third table on page 25. The response field definitions and values are described in the last table.

Command 0xN GENERIC_COMMAND

GENERIC_COMMAND performs the following function.

<detailed description of command including description of fields>

Command Arguments: Three

Response Bytes: Two

Command

Bit	D7	D6	D5	D4	D3	D2	D1	D0
CMD	N_7	N_6	N_5	N_4	N_3	N_2	N_1	N_0
ARG1	0	0	0	0	0	FIELD_B	FIELD_A	
ARG2	0	0	0	0	FIELD_C			
ARG3	FIELD_D							

Bit	Name	Function
ARG1 1:0	FIELD_A[1:0]	***<Title of FIELD_A>*** 0 = *<description of value>* 1 = *<description of value>* 2 = ... *<Description of FIELD_A>*
ARG1 2	FIELD_B	***<Title of FIELD_B>*** *<description of values>* *<Description of FIELD_B>*
ARG2 3:0	FIELD_C[3:0]	***<Title of FIELD_C>*** *<description of values>* *<Description of FIELD_C>*
ARG3 7:0	FIELD_D	***<Title of FIELD_D>*** *<description of values>* *<Description of FIELD_D>*

Response

Bit	D7	D6	D5	D4	D3	D2	D1	D0
STATUS	*<standard response for all commands for* STATUS>							
RESP1	X	X	X	X	FIELD_E			
RESP2	FIELD_F							

Bit	Name	Function
RESP1 3:0	FIELD_E[3:0]	***<Title of FIELD_E>*** *<description of values>* *<Description of FIELD_E>*
RESP2 7:0	FIELD_F[7:0]	***<Title of FIELD_F>*** *<description of values>* *<Description of FIELD_F>*

5. Pin Descriptions

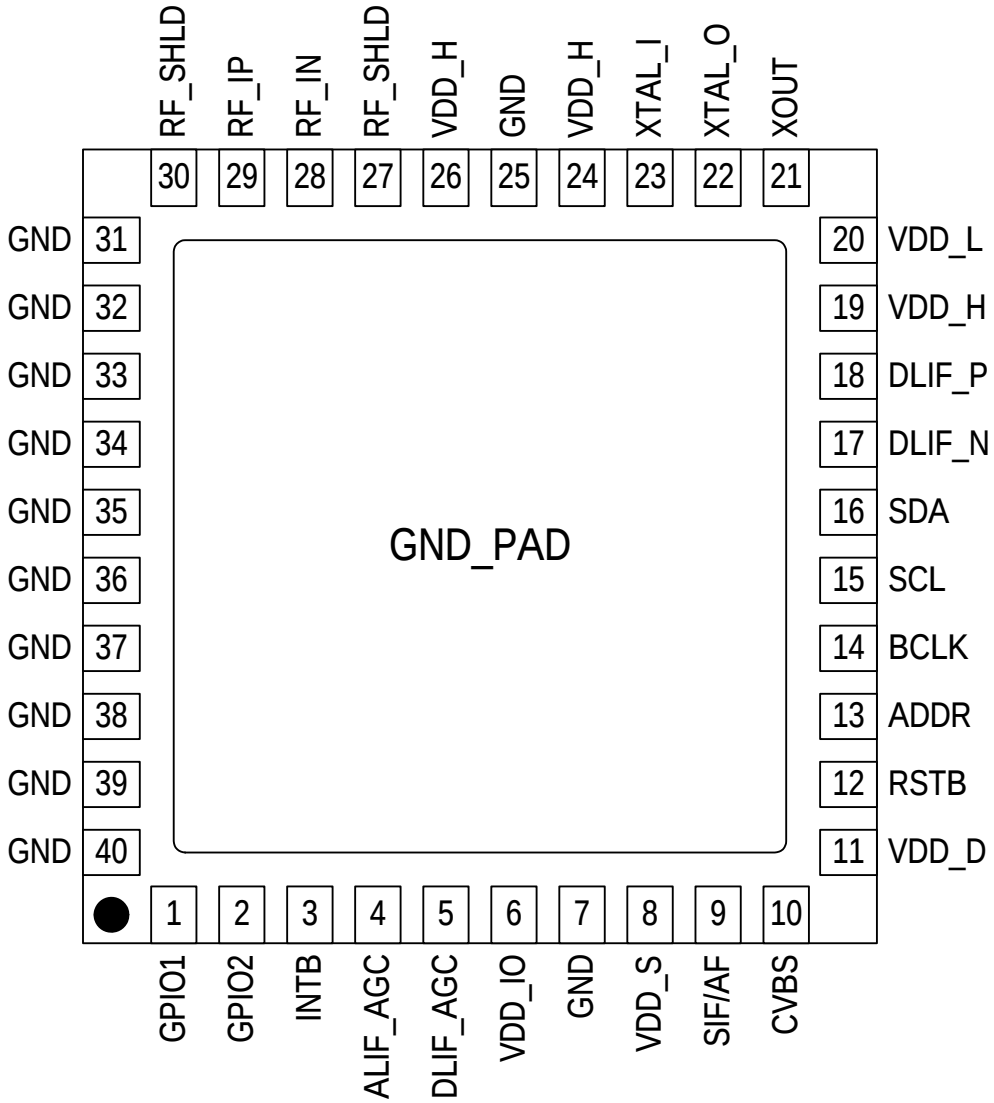


Table 12. Si2173 Pin Descriptions

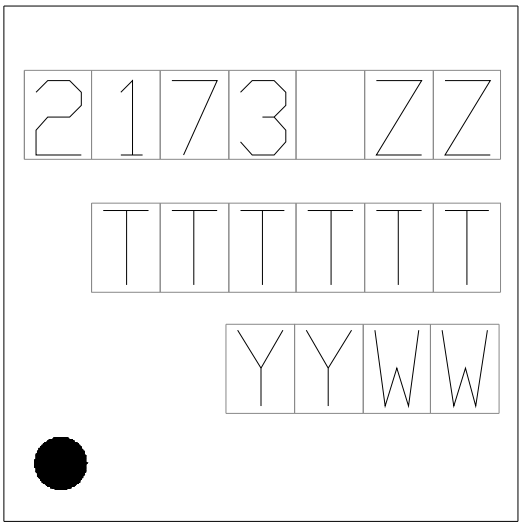
Pin Number(s)	Name	I/O	Description
1*	GPIO1	I/O	General purpose input/output #1
2*	GPIO2	I/O	General purpose input/output #2
3*	INTB	O	Interrupt request output
4*	ALIF_AGC	—	No connect (leave floating)
5*	DLIF_AGC	I	DLIF output amplitude control input (optional)
6	VDD_IO	S	I/O supply voltage, 1.8 to 3.3 V
7	GND	S	Ground. Connect GND pins to GND_PAD.
8	VDD_S	S	Interface supply voltage (I^2C), 1.8 to 5.0 V
9*	SIF/AF	O	Analog audio output, SIF or AF
10*	CVBS	O	Analog composite video output
11	VDD_D	S	Digital supply voltage, 1.8 V
12	RSTB	I	Hardware reset (active low)
13	ADDR	I	I^2C address select
14*	BCLK	O	Buffered clock output
15	SCL	I	I^2C clock input
16	SDA	I/O	I^2C data input/output
17*	DLIF_N	O	DLIF differential output to DTV demodulator (negative)
18*	DLIF_P	O	DLIF differential output to DTV demodulator (positive)
19	VDD_H	S	Analog high supply voltage, 3.3 V
20	VDD_L	S	Analog low supply voltage, 1.8 V
21*	XOUT	O	Output reference clock to secondary Si2173 (optional)
22*	XTAL_O	I	Crystal pin 2 (leave floating if XTAL_I is driven by XOUT of another Si2173)
23	XTAL_I	I	Crystal pin 1 (or RCLK input driven by XOUT of another Si2173)
24	VDD_H	S	Analog high supply voltage, 3.3 V
25	GND	S	Ground. Connect GND pins to GND_PAD.
26	VDD_H	S	Analog high supply voltage, 3.3 V
27	RF_SHLD	S	RF input shield
28	RF_IN	I	RF balanced input from balun (negative)
29	RF_IP	I	RF balanced input from balun (positive)
30	RF_SHLD	S	RF input shield
31 to 40	GND	S	Ground. Connect GND pins to GND_PAD.
	GND_PAD	S	Ground. Connect GND pins to GND_PAD.
*** Note:** Pin should be left floating if unused.			

6. Ordering Guide

Part Number*	Description	Package Type	Operating Temperature
Si2173-A30-GM	Worldwide hybrid TV tuner with analog demodulator for NTSC, PAL/SECAM, ATSC/QAM, DVB-T/T2/C, ISDB-T/C, DTMB	40-pin QFN, RoHS-compliant	–20 to 85 °C
***Note:** Add an “R” at the end of the device part number to denote tape and reel option. The “A” denotes product revision A and “30” denotes firmware revision 3.0.			

7. Package Markings (Top Mark)

7.1. Si2173 Top Mark



7.2. Top Mark Explanation

Mark Method	YAG Laser	
Line 1 Marking	Part Number	Si2173
	Customer Firmware Revision	ZZ = Firmware Revision (i.e., 30 = 3.0)
Line 2 Marking	TTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form.
Line 3 Marking	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	Circle = 0.7 mm Diameter (Bottom-left justified)	Pin 1 identifier

8. Package Outline

Figure 9 illustrates the package details for the Si2173. Table 13 lists the values for the dimensions shown in the illustration.

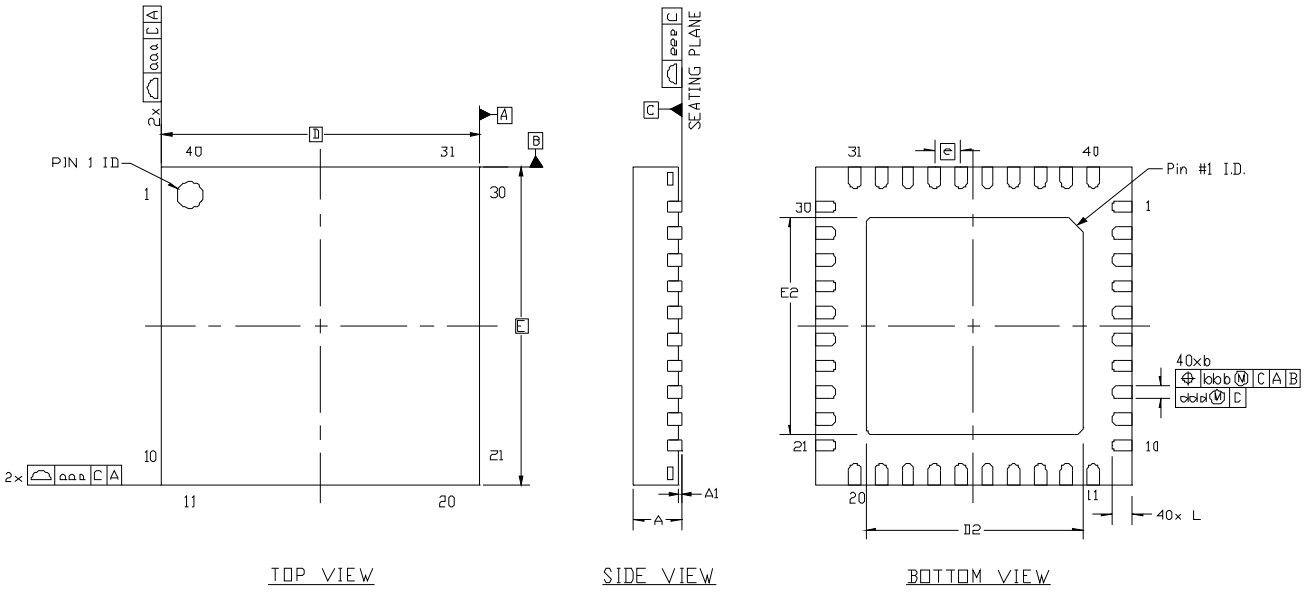


Figure 9. 40-Pin Quad Flat No-Lead (QFN)

Table 13. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	—	0.05
b	0.18	0.23	0.28
D		6.00 BSC	
D2	4.60	4.70	4.80
e		0.50 BSC	
E		6.00 BSC	

Symbol	Millimeters		
	Min	Nom	Max
E2	4.60	4.70	4.80
L	0.35	0.40	0.45
aaa		0.10	
bbb		0.10	
ddd		0.05	
eee		0.08	

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VJJD-5, except for features A, D2, and E2 which are toleranced per supplier designation.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

9. PCB Land Pattern

Figure 10 illustrates the PCB land pattern details for the Si2173. Table 14 lists the values for the dimensions shown in the illustration.

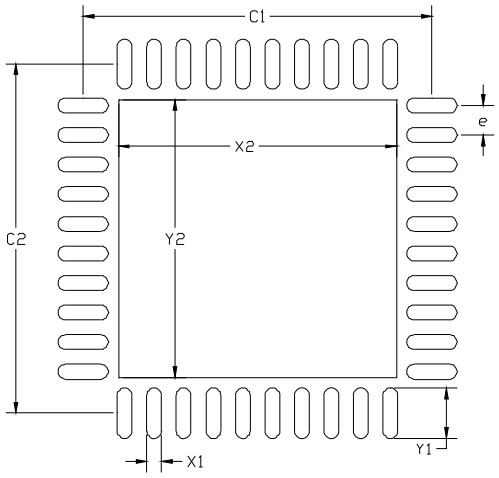


Figure 10. PCB Land Pattern

Table 14. PCB Land Pattern Dimensions

Symbol	Millimeters		Symbol	Millimeters	
	Min	Max		Min	Max
C1	5.80	5.90	X1	0.15	0.25
C2	5.80	5.90	X2	4.70	4.80
e	0.50 BSC		Y1	0.75	0.85
			Y2	4.70	4.80

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This land pattern design is based on IPC-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder-mask-defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
9. A 4x4 array of 0.90 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

10. Additional Reference Resources

- Si2173 Evaluation Board GUI User Manual
- AN501: Si2173 Programming Guide
- AN413: Si217x Layout and Design Guidelines
- AN468: Si217x Distortion Performance with Optimized Return Loss
- AN416: Si217x Evaluation Board Test Procedure
- Si217x Video Filter Tool User's Guide
- Si2165 Multi-Standard DVB-T/V Demodulator Data Sheet
- Si2167 Multi-Media DVB-T/C/S/S2 Demodulator Data Sheet
- Si217x Customer Support Email DTVinfo@silabs.com

DOCUMENT CHANGE LIST

Revision 0.3 to Revision 1.0

- Minor text changes on front page
- Updated Table 2 "Absolute Maximum Ratings[1]"
- Updated Table 3 "DC Characteristics[1]"
- Updated Table 4 "Hybrid Tuner Characteristics"
- Updated Table 5 "Analog TV Receiver Characteristics[1]"
- Updated Table 8 "Crystal Oscillator and Output Clocks Characteristics"
- Updated Section 3. "Functional Description"
  - Updated Figure 7, “Integrated Channel Filters (Eliminate External IF SAW Filters),” on page 21
  - Updated Figure 8, “Analog TV Video and SIF Audio Filters (For Clarity, Only a Subset of All Audio Standards is Shown),” on page 22
  - Minor wording changes in the text
- Added footnote in Table 12 "Si2173 Pin Descriptions"
- Updated Description in Section 6. "Ordering Guide”
- Updated Section 10. "Additional Reference Resources”

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