A General Three-Phase PFC Controller
Part I. for Rectifiers with a Parallel-Connected Dual Boost Topology

Chongming Qiao and Keyue M. Smedley
Department of Electrical and Computer Engineering
University of California, Irvine, CA 92697
Tel: (949) 824-6710, Fax: (949) 824-3203, email: smedley@ uci.edu

Abstract--A general constant-frequency power-factor-correction (PFC) controller is proposed for three-phase rectifiers with parallel-connected dual-boost topologies. This paper shows that unity fundamental power factor and low current distortion in all three phases can be realized by one-cycle control of a linear combination of the inductor currents using one integrator with reset along with a few logic components. This new extension of one-cycle control provides the core PFC function to the dual-boost topologies and the logical circuit rotates the PFC function in three phases. It does not require multipliers, used in many other control approaches, to scale the current reference according to the output power level. In each 60° of ac line cycle, only two switches are switched at high frequency; therefore the switching losses are significantly reduced. All switches are switched at low current, which results in reduced current ratings. This control method is simple and general. It is applicable to three-phase rectifiers that can be decoupled into parallel-connected dual-boost topologies by slight modification of the logic circuit. This control method is verified by theoretical analysis and experimental results. The proposed controller is ready to be integrated into a three-phase PFC control chip.

1 Introduction

Traditional diode rectifiers and thyristor rectifiers draw pulsed current from the ac main, causing significant current harmonics pollution. The international standards presented in IEC 1000-3-2 and IEEE 519 imposed firm harmonic restrictions to modern rectifiers, which results in a focused research effort on the topic of unity power factor rectifiers.

Three-phase boost PFC rectifiers are preferred topologies for high power applications due to their symmetric current drawing characteristics. A single-switch constant-duty-ratio control method was proposed in [1] for three-phase boost rectifiers operated in discontinuous conduction mode (DCM). It achieves relatively low current distortion with a very simple circuit. But the high voltage and current stress on the main switches are not desirable. Furthermore, unity power factor can not be achieved for all load range [2]. A third harmonic injection method was proposed in [3] for a dual boost converter with center-tapped dc-link and split output capacitors. This method achieves low current distortion. However, it is not convenient to generate the third harmonic signal tuned to the right frequency and right amplitude. Hysteresis control and d-q transformation control are frequently used control approaches. Hysteresis control results in variable switching frequency that is difficult for EMI filter design. The d-q approach is based on digital implementation that leads to complicated systems. An encouraging analog solution with constant switching frequency modulation was provided in [4] for a particular rectifier. Several multipliers are necessary to implement the three phase current references.

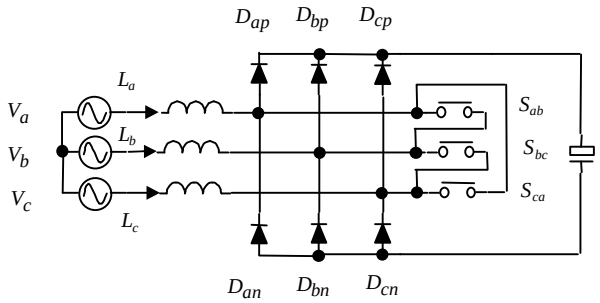
Many promising rectifier topologies have been also proposed using three-level or multi-level configurations [5-11]. A very systematic study of 3-phase PFC boost rectifiers with a non-isolated dc voltage rail was presented in [12-16], including several three-phase PWM boost rectifiers employing a series-connected dual boost topology.

Intrigued by the achievement both in the topologies and control, the objective of this research is to develop a simple and general control scheme that realizes unity power factor for boost-derived three-phase rectifiers.

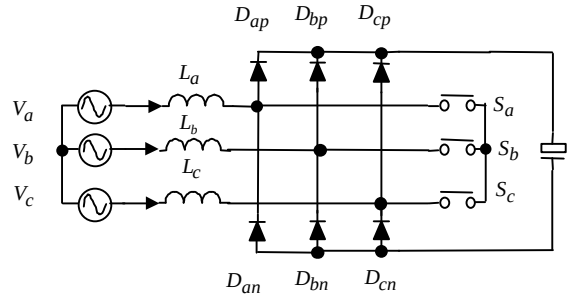
Most of boost-derived three-phase rectifiers can be categorized into two groups: one group of them can be decoupled into a series-connected dual-boost topology [12-16] that features central-tapped or split dc output capacitors. The other group can be decoupled into a parallel-connected dual-boost topology that features a single dc output capacitor. The dual-boost sub-topologies rotate their connection every 60° of the line cycle depending on the line voltage states. In the light of these observations, a general three-phase boost PFC controller based on one-cycle control [17,18,19] is proposed that employs an integrator with reset along with a few logic components to realize unity power factor in all three phase. This new extension of one-cycle control provides the core PFC function to a dual-boost topology and the logical circuit rotates the PFC function in three phases. The control scheme is simple and general. The proposed controller has the following features:

- Constant switching frequency,
- No need for multipliers that are required to scale the current reference according to the load level as used in many other control approaches,
- In each 60° of ac line cycle, only two switches are switched at high frequency. Therefore, the switching loss is significantly reduced.
- Switches operate at a current lower than the phase current, which results in reduced current ratings and conduction losses.
- It is applicable to most boost-derived three-phase rectifiers by slight modification of the logic circuit,

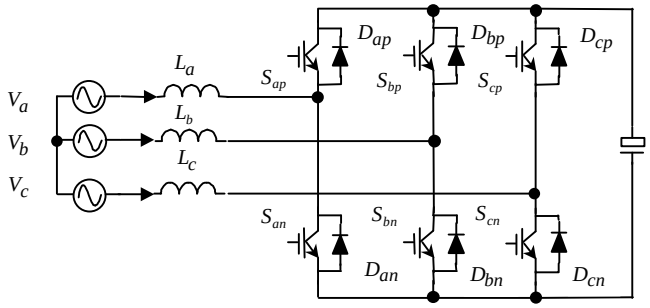
while the core of the PFC control function remains common for different rectifiers.



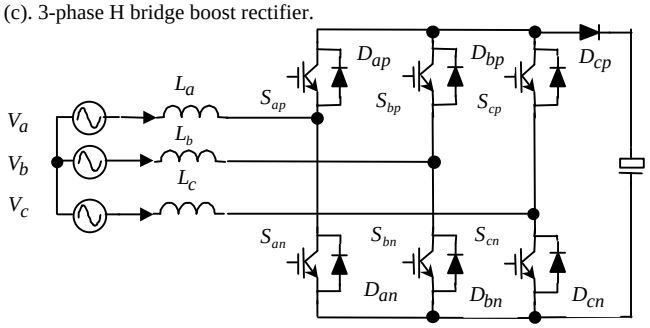
(a). 3-phase boost rectifier with delta-connected 3 f switches.



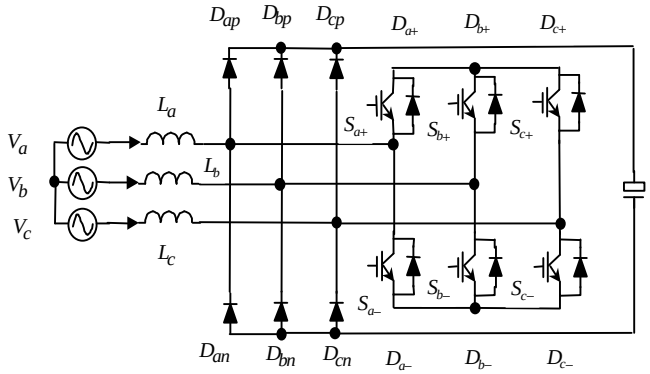
(b). 3-phase boost rectifier with star-connected 3 f switches.



(c). 3-phase H bridge boost rectifier.



(d). 3-phase H bridge boost rectifier with a diode.



(e). 3-phase boost rectifier with an inverter network

Fig. 1. Three-phase boost rectifiers using three ac inductors & a single dc-rail

This paper is devoted to rectifiers with paralleled-connected dual–boost topology. A companion paper [20] is followed that deals with the rectifiers with series-connected dual-boost topology. Section 2 of this paper discusses the operation of a family of rectifiers with a parallel-connected dual-boost topology. In Section 3, the proposed three-phase PFC controller is described in detailed. Experimental verification is given for the three-phase boost rectifier with delta connected 3f switches in Section 4. Analysis and simulation of this control approach for the H-bridge boost rectifier is presented in Section 5. Finally, a conclusion is given in Section 6.

2 A family of rectifiers with a parallel-connected dual-boost topology

A family of three-phase boost rectifiers with a single dc-rail is shown in Fig. 1. The three-phase H-bridge boost rectifier in Fig. 1 (c) and (d) are similar except for an additional diode in (d). The normalized three-phase input voltage waveforms are shown in Fig. 2. During each 60° of the ac line cycle as shown in Fig. 2, all the rectifiers given in Fig. 1 can be decoupled into a parallel-connected dual-boost topology. Take the rectifier with delta-connected 3f switched shown in Fig. 1 (a) as an example. During the 60 degree region (0~60°) of Fig. 2, switch S_{ca} is off, while the other two switches S_{ab} and S_{bc} are controlled so that the input inductor currents i_{La} and i_{Lc} follow the phase voltages V_a and V_c respectively. The equivalent circuit can be viewed as a parallel connected dual-boost topology as shown in Fig. 3 (a). In the next 60° (60°~120°), switch S_{bc} is off, while switches S_{ab} and S_{ca} are controlled. The equivalent circuit along with its dual-boost topology is shown in Fig. 3 (b). These dual-boost topologies are equivalent for each 60° interval, while the circuit parameters of the dual-boost topology are different as listed in Table 1. Note there are two possibilities for the parameter combination, i.e. voltage V_p can be either $V_a - V_b$ or $V_c - V_b$ during interval (0~60°), and so on. The first possibility is considered here, since the second one is similar.

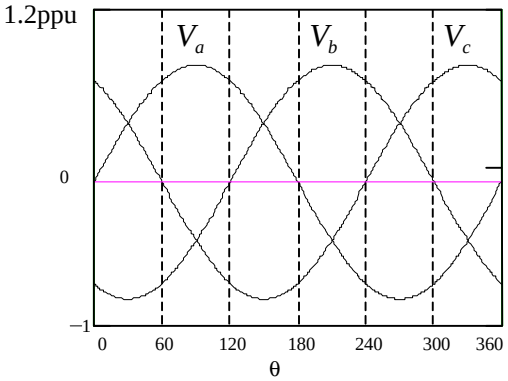


Fig. 2. Normalized three-phase voltage waveforms.

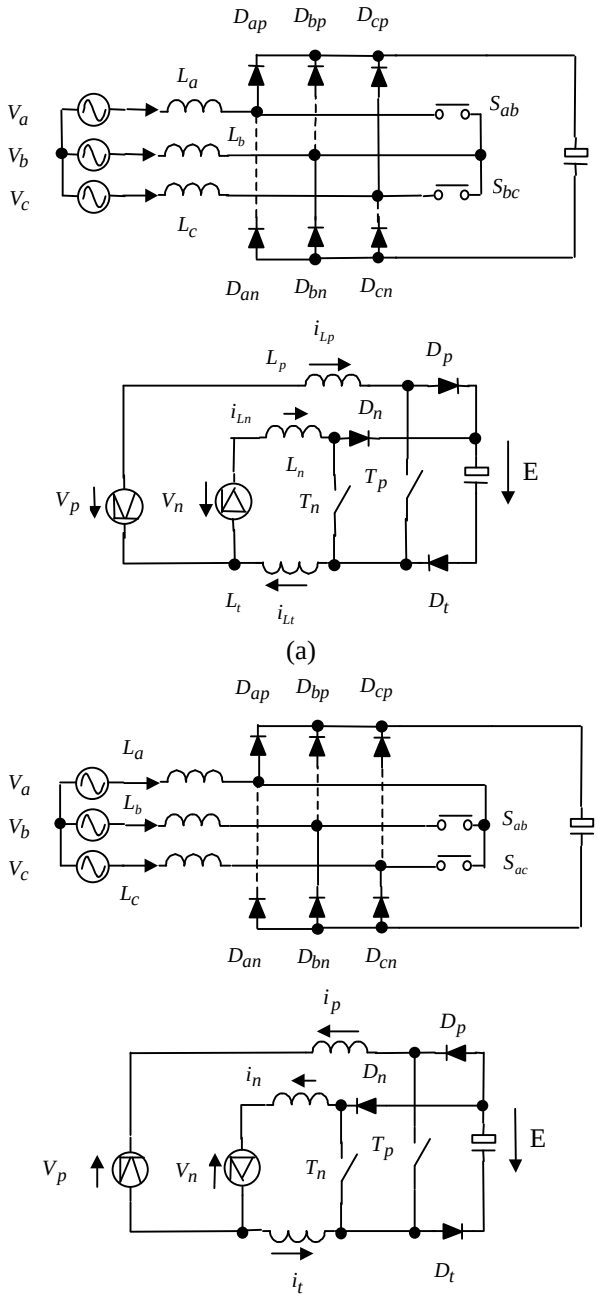


Fig. 3. The equivalent circuit of 3-phase boost rectifier with delta-connected switches and its corresponding parallel-connected dual-boost topology. (a) (0~60°). (b). (60°~120°).

Table 1. The cross-reference of the circuit parameters between the three-phase boost rectifier shown in Fig. 1 (a) and parallel-connected dual-boost topology.

	V_p	V_n	L_p	L_n	L_t	T_p	T_n	D_p	D_n	D_t
0~60	V_{ab}	V_{cb}	L_a	L_c	L_b	S_{ab}	S_{bc}	D_{ap}	D_{cp}	D_{bn}
60~120	V_{ab}	V_{ac}	L_b	L_c	L_a	S_{ab}	S_{ca}	D_{bn}	D_{cn}	D_{ap}
120~180	V_{bc}	V_{ac}	L_b	L_a	L_c	S_{bc}	S_{ca}	D_{bp}	D_{ap}	D_{cn}
180~240	V_{bc}	V_{ba}	L_c	L_a	L_b	S_{bc}	S_{ab}	D_{cn}	D_{an}	D_{bp}
240~300	V_{ca}	V_{ba}	L_c	L_b	L_a	S_{ca}	S_{ab}	D_{cp}	D_{bp}	D_{an}
300~360	V_{ca}	V_{cb}	L_a	L_b	L_c	S_{ca}	S_{bc}	D_{an}	D_{bn}	D_{cp}

For the dual-boost topology shown in Fig. 3 (a), four switch states are available for the two switches T_p and T_n. The switching states and inductor voltages are shown in Table 2. The equivalent circuits of the dual-boost topology in all switching states are shown in Fig. 4.

Table 2. Switching states and inductor voltages for the parallel-connected dual-boost topology

State	T_p	T_n	V_{Lp}	V_{Ln}	V_{Lt}
I	ON	ON	V_p^*	V_n^*	V_t^*
II	ON	OFF	$V_p^*+\frac{1}{3}\cdot E$	$V_n^*-\frac{2}{3}\cdot E$	$V_t^*-\frac{1}{3}\cdot E$
III	OFF	ON	$V_p^*-\frac{2}{3}\cdot E$	$V_n^*+\frac{1}{3}\cdot E$	$V_t^*-\frac{1}{3}\cdot E$
IV	OFF	OFF	$V_p^*-\frac{1}{3}\cdot E$	$V_n^*-\frac{1}{3}\cdot E$	$V_t^*-\frac{2}{3}\cdot E$

where

$$\begin{bmatrix} V_p^* \\ V_n^* \\ V_t^* \end{bmatrix} = \begin{bmatrix} \frac{2}{3} & -\frac{1}{3} \\ -\frac{1}{3} & \frac{2}{3} \\ \frac{1}{3} & \frac{1}{3} \end{bmatrix} \cdot \begin{bmatrix} V_p \\ V_n \end{bmatrix}$$

and voltage 'E' equals the output voltage V_o.

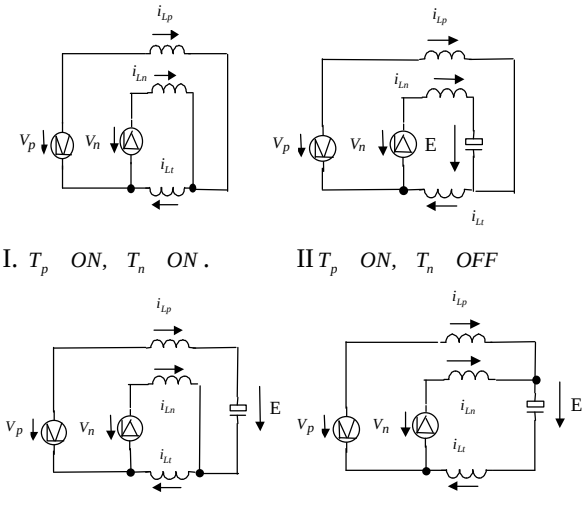


Fig. 4. The equivalent circuits for the parallel-connected dual-boost topology in all four switching states.

For a three-phase PFC with a constant switching frequency, only two switching sequences are possible, i.e. I, II, IV (condition $d_p > d_n$) or I, III, IV (condition $d_p < d_n$) during each switching cycle, if trailing-edge modulation is performed. The voltage and current waveforms of the inductors are shown in Fig. 5 for the first switching sequence ($d_p > d_n$).

Based on the assumption that switching frequency is much higher than the line frequency, the inductor voltage-second balance is used.

$$\begin{cases} V_p^* \cdot d_n + \left(V_p^* + \frac{1}{3} \cdot E\right) \cdot \left(d_p - d_n\right) + \left(V_p^* - \frac{1}{3} \cdot E\right) \cdot (1 - d_p) = 0 \\ V_n^* \cdot d_n + \left(V_n^* - \frac{2}{3} \cdot E\right) \cdot \left(d_p - d_n\right) + \left(V_n^* - \frac{1}{3} \cdot E\right) \cdot (1 - d_p) = 0 \\ V_t^* \cdot d_n + \left(V_t^* - \frac{1}{3} \cdot E\right) \cdot \left(d_p - d_n\right) + \left(V_t^* - \frac{2}{3} \cdot E\right) \cdot (1 - d_p) = 0 \end{cases} \text{---------(1)}$$

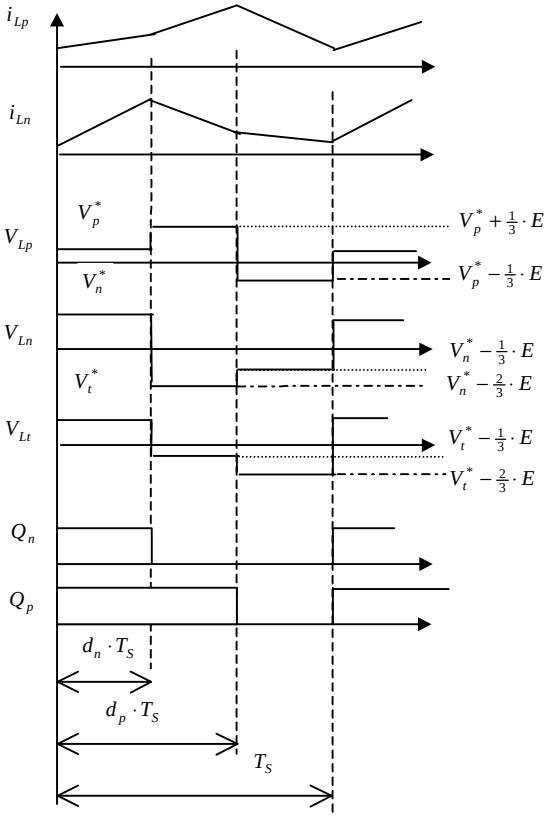


Fig. 5. The inductor voltage and current waveforms for the topology shown in Fig. 3 (a) under the condition $d_p > d_n$.

The following equation is true for a symmetrical three-phase system:

$$V_p^* + V_n^* - V_t^* = 0 \text{----------(2)}$$

Combination of the equation (1), (2) and further simplification yield

$$\begin{bmatrix} 1 - d_p \\ 1 - d_n \end{bmatrix} = \begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix} \cdot \begin{bmatrix} \frac{V_p^*}{E} \\ \frac{V_n^*}{E} \end{bmatrix} \text{-------(3)}$$

It can be verified that this equation is valid for the other switching sequence I, III, and IV ($d_p < d_n$) as well. In the steady sate, equation $\frac{E}{V_{in}} = \frac{1}{1 - D}$ is valid for a dc-dc boost converter operated in continuous conduction mode (CCM), where voltages V_{in}, E are the input and output voltages for the dc-dc boost converter respectively. Similarly Equation (3) gives an inherent relationships between the duty cycle and the input, output voltage for the parallel-connected dual-boost topology. This relationship is independent of the control scheme as long as the dual-boost topology operates in CCM.

3 Proposed three-phase PFC controller

For the unity power factor three-phase PFC, the control goal is to force the switching-cycle average of the inductor currents in each phase to follow the sinusoidal phase voltages.

$$V_a = R_e \cdot i_a; V_b = R_e \cdot i_b; V_c = R_e \cdot i_c \text{ -----(4)}$$

where R_e is the emulated resistance that reflects the load current.

This control goal can be realized by controlling the inductor currents i_{Lp} and i_{Ln} to follow the voltages V_p^* and V_n^* respectively. For example, during the interval (0-60°), assuming that $V_p = V_a - V_b$ and $V_n = V_c - V_b$, following equations are resulted:

$$\begin{cases} V_p^* = \frac{2}{3} \cdot V_p - \frac{1}{3} \cdot V_n = \frac{2}{3} \cdot (V_a - V_b) - \frac{1}{3} \cdot (V_c - V_b) = V_a \\ \left\langle i_{Lp} \right\rangle = \left\langle i_{La} \right\rangle = i_a \\ V_n^* = \frac{2}{3} \cdot V_n - \frac{1}{3} \cdot V_p = \frac{2}{3} \cdot (V_c - V_b) - \frac{1}{3} \cdot (V_a - V_b) = V_c \\ \left\langle i_{Ln} \right\rangle = \left\langle i_{Lc} \right\rangle = i_c \end{cases} \text{----(5)}$$

Therefore, the control goal of three-phase PFC can be rewritten as

$$\begin{cases} V_p^* = R_e \cdot \left\langle i_{Lp} \right\rangle \\ V_n^* = R_e \cdot \left\langle i_{Ln} \right\rangle \end{cases} \text{------(6)}$$

Substituting equation (6) into (3) yields

$$\begin{bmatrix} 1 - d_p \\ 1 - d_n \end{bmatrix} = \frac{R_e}{E \cdot R_s} \cdot R_s \cdot \begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix} \cdot \begin{bmatrix} \left\langle i_{Lp} \right\rangle \\ \left\langle i_{Ln} \right\rangle \end{bmatrix} \text{---(7)}$$

where R_s is the equivalent current sensing resistance (assuming all the current sensing resistances are equal to R_s).

Let

$$V_m = \frac{E \cdot R_s}{R_e} \text{ -------(8)}$$

where V_m is the output of the voltage loop compensator, equation (7) can be rewritten as

$$V_m \cdot \begin{bmatrix} 1 - d_p \\ 1 - d_n \end{bmatrix} = R_s \cdot \begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix} \cdot \begin{bmatrix} \left\langle i_{Lp} \right\rangle \\ \left\langle i_{Ln} \right\rangle \end{bmatrix} \text{--------(9)}$$

It shows that three-phase PFC can be realized by controlling the duty ratio of switches T_p and T_n such that the linear combination of inductor currents $\left\langle i_{Lp} \right\rangle$ and $\left\langle i_{Ln} \right\rangle$ satisfy equation (9). These equations can be realized through an integrator with reset and some linear network such as a clock, a comparator, a flip/flop and adders. The control core to realize the equation (9) is shown in Fig. 6. Since the parallel-connected dual-boost topologies change its parameters such as i_{Lp}, i_{Ln} during each 60° of line cycle, an input multiplexer circuit and an output logic

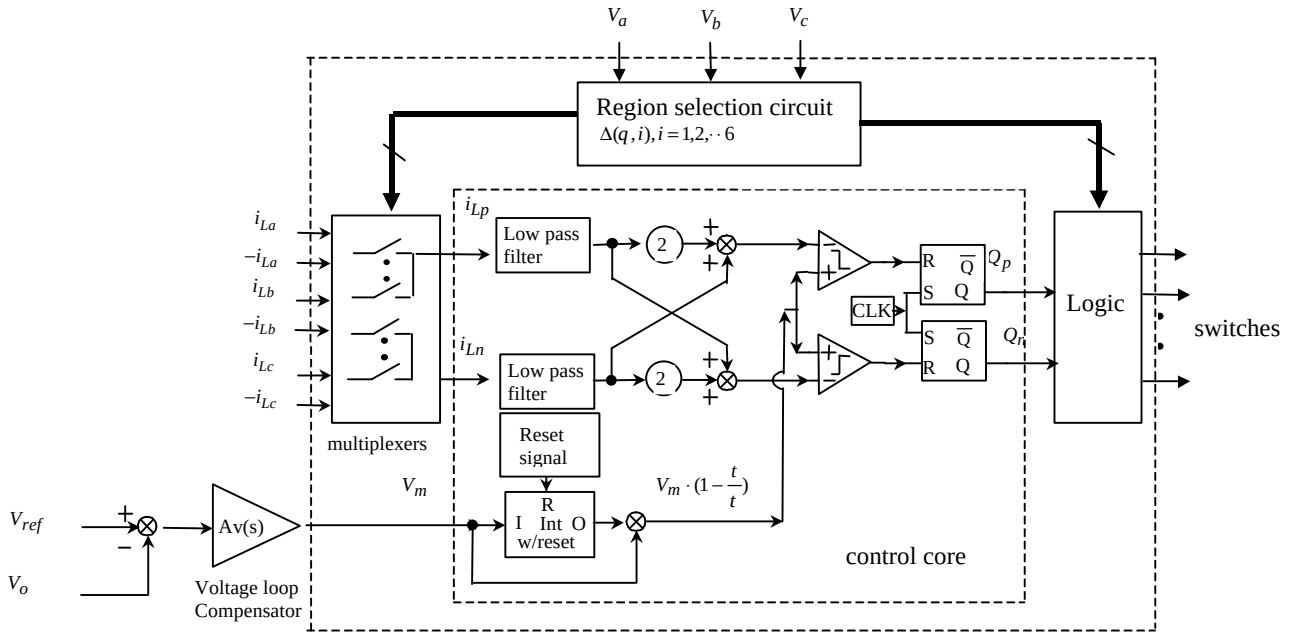
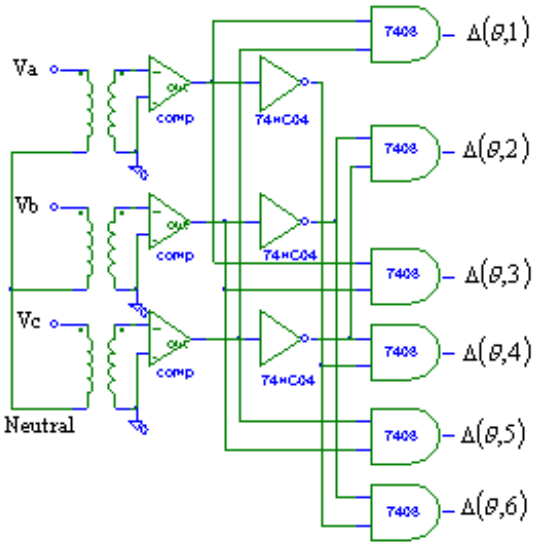
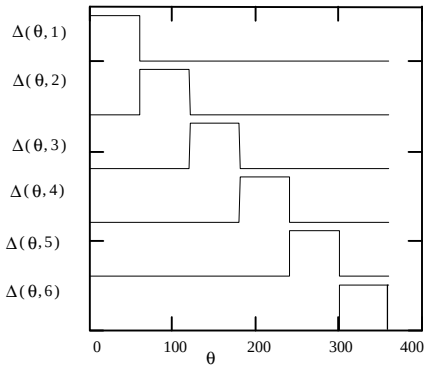


Fig. 6. The control block of the proposed general three-phase PFC controller-I



(a)



(b)

Fig.7. (a) Schematic implementation of the selection function $\Delta(i,q)$ $i=1,2,..6$. (b) Operation waveforms.

circuit are required. Overall, the control block to realize the three-phase PFC function is shown in Fig. 6.

This control block includes four functional circuits:

(1). The region selection circuit is to determine the operation region as well as the corresponding equivalent circuit at a given time. The region selection function $\Delta(q,i)$ is defined as:

$$\Delta(q,i)=u(q-(i-1)\cdot 60)-u(q-i\cdot 60) \text{----(10).}$$

It can be implemented by sensing the input voltage as shown in Fig.7 (a). The waveforms of selection function are shown in Fig.7(b).

(2).The input multiplexer circuit is used to select the input inductor current in order to configure the $\langle i_{Lp}\rangle and \langle i_{Ln}\rangle$. For example, the equivalent current i_{Lp} can be expressed as

$$i_{Lp}=|i_{La}|\cdot(\Delta(1,q)+\Delta(6,q))+|i_{Lb}|\cdot(\Delta(2,q)+\Delta(3,q)) \\ ++|i_{Lc}|\cdot(\Delta(4,q)+\Delta(5,q))$$

.

(3).The core circuit includes an adder, comparators, and an integrator with reset to realize the equation (9). The time constant of integrator is set to equal the switching period. The operation waveforms are shown in Fig. 8.

(4). The output logic circuit applies the equivalent switching control signal Q_p and Q_n to switches in the rectifier. The logic function varies from one rectifier to another. The control signals for output switches are also functions of selection function $\Delta(i,q)$ and control signal for switches T_p and T_n. For example, the control signal of switches S_{ab} is given by:

$$Q_{ab}=Q_p\cdot(\Delta(1,q)+\Delta(2,q))+Q_n\cdot(\Delta(4,q)+\Delta(5,q));$$

where Q_{ab}, Q_p and Q_n are control signals for

switches S_{ab}, T_p and T_n respectively. The implementation circuit is shown in Fig. 9.

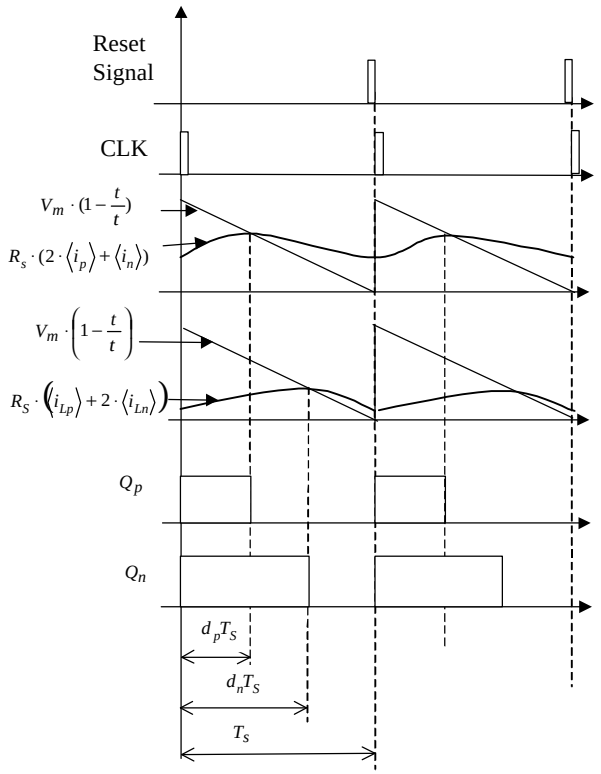


Fig. 8. The waveforms of the control core in Fig. 6.

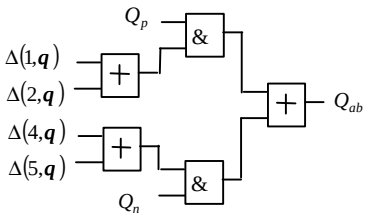


Fig. 9. Realization of control signal for switch S_{ab}.

The control algorithm for the boost PFC shown in Fig. 1 (a) is listed in Table 3. From the table, two conclusions can be obtained:

- The current i_{Lp} and i_{Ln} are smaller than the phase current. Therefore, the switches S_{ab}, S_{bc}, and S_{ca} have lower current rating and lower conduction losses.
- During each 60° region, only two switches T_p and T_n are operating at high frequency. Therefore, switching losses are expected to be lower.

Table 3. The control algorithm for the 3-phase boost rectifier with delta-connected switches

Region	V_p	V_n	i_{Lp}	i_{Ln}	i_{Lt}	Q_{ab}	Q_{bc}	Q_{ca}
0~60	V_{ab}	V_{cb}	i_{La}	i_{Lc}	$-i_{Lb}$	Q_p	Q_n	0
60~120	V_{ab}	V_{ac}	$-i_{Lb}$	$-i_{Lc}$	i_{La}	Q_p	0	Q_n
120~180	V_{bc}	V_{ac}	i_{Lb}	i_{La}	$-i_{Lc}$	0	Q_p	Q_n
180~240	V_{bc}	V_{ba}	$-i_{Lc}$	$-i_{La}$	i_{Lb}	Q_n	Q_p	0
240~300	V_{ca}	V_{ba}	i_{Lc}	i_{Lb}	$-i_{La}$	Q_n	0	Q_p
300~360	V_{ca}	V_{cb}	$-i_{La}$	$-i_{Lb}$	i_{Lc}	0	Q_n	Q_p

4 Experimental verification

A 1.5 kW prototype of the three-phase rectifier with delta-connected 3 f switches shown in Fig. 1 (a) was built. In order to improve the efficiency and reduce switching noise, an active zero-voltage soft-switching circuit was employed. The experimental schematic is shown in Fig. 10. The parameters of the components are listed as follows: the inductors $L_a = L_b = L_c = 560uH$; the output capacitor $C_o = 470uF$; the main switches use MTY25N60E; and the main diodes $d_{ap}, d_{an}, \cdots d_{cn}$ *and* d_1 are MUR3080; the auxiliary switch is MTY8N60E; the soft-switching inductor and capacitor are $L_r = 10uH$ and $C_r = 3nF$; diodes d_2, d_3 are MUR860. The experimental conditions are as follows: the input phase voltage is $120Vrms$; the output voltage is 475VDC; switching frequency: 55kHz; load resistance is 160Ω; output power is 1.41KW. The measured three-phase current waveforms are shown in Fig. 11. The phase A voltage and current are shown in Fig. 12. All the waveforms are measured by Tektronix oscilloscope TDS 520. The measured THD at full load and 120Vrms input is 6.1%, while the phase voltages have a THD of 3.9% themselves.

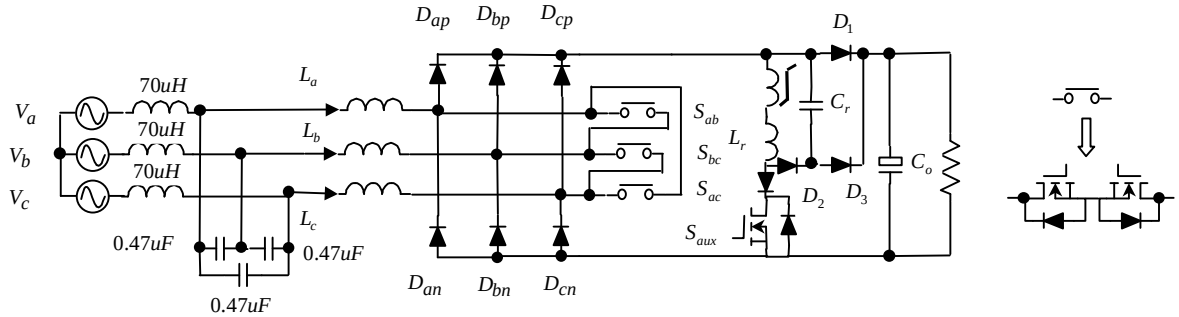


Fig. 10. The schematic of experimental three-phase boost PFC with active soft switching.

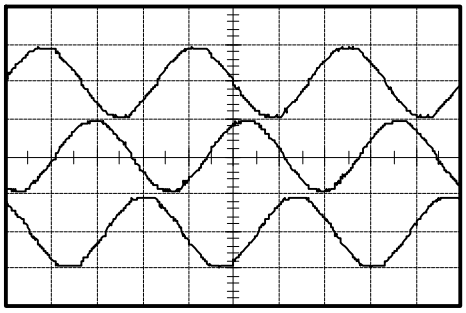


Fig. 11. Three phase inductor current waveforms at full load. Horizontal scale: 5ms/div; vertical scale, 5A/div.

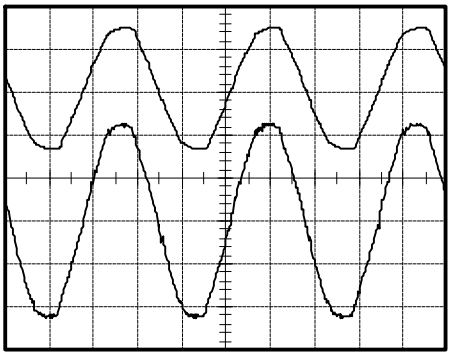


Fig. 12. Waveforms of phase voltage and current at full load. Horizontal scale, 5ms/div. Top: input phase voltage 100V/div. Bottom: input phase A current, 2A/div.

5 Analysis and simulation of the proposed controller for the H-bridge boost rectifier as well as the rest of the family

All the members in the parallel connected dual-boost family can be controlled in a similar way. The H-bridge boost rectifier shown in Fig. 1 (c) is decoupled into the parallel-connected dual-boost topology as shown in Fig. 3. For example, during the 0~60° interval, switches S_{an} and S_{cn} are controlled so that the inductor currents i_{La}, i_{Lc} follow the phase voltages V_a, V_c respectively. The equivalent circuit for this interval and the parallel-connected dual boost topology are shown in Fig. 13. As a result, the H-bridge rectifier can also be controlled by proposed controller shown in Fig. 6 with slight modification of the output logic circuit. The corresponding parameters are listed in the Table 4. Control algorithm is shown in Table 5. The simulated current waveforms for the H-bridge rectifier are shown in Fig. 14. The simulated THD is 2.86% when the input voltage is purely sinusoidal. The operation, the corresponding parameters, and control algorithm for rectifier shown in Fig. 1 (d) are the same as that of the H-bridge rectifier shown in Fig. 1 (c) in CCM operation. However, the operations are different when they get into DCM mode. The rectifier in Fig. 1 (c) can be designed to operate always in CCM by slightly modifying output logic circuits.

The rest of the family members, the boost rectifier with star-connected switches shown in Fig. 1 (b) and boost rectifier with inverter network shown in Fig. 1 (e), can also be decoupled into dual-boost topologies in each 60°. The parameter cross-references for these two rectifiers are listed in Table 6. The control algorithm can be derived in a similar way. The simulated waveforms for circuit in Fig. 1(b) and (e) are not listed here, since they are similar to the simulated waveforms shown in Fig. 14.

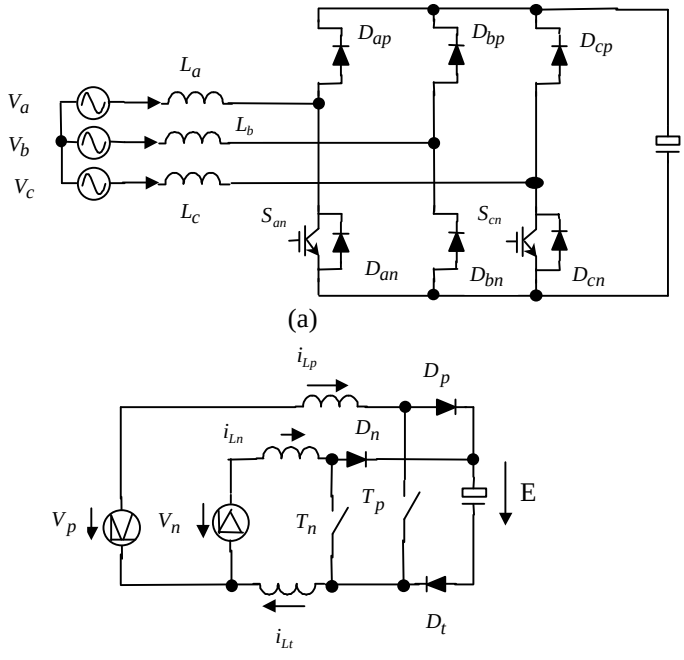


Fig. 13. The three-phase H bridge boost rectifier (a). The equivalent circuit for interval 0~60°. (b). The parallel-connected dual-boost topology.

Table 4. The cross-reference between the H-bridge boost rectifier and the parallel-connected dual-boost topology.

Region	V_p	V_n	L_p	L_n	L_t	T_p	T_n	D_p	D_n	D_t
0~60	V_{ab}	V_{cb}	L_a	L_c	L_b	S_{an}	S_{cn}	D_{ap}	D_{cp}	D_{bn}
60~120	V_{ab}	V_{ac}	L_b	L_c	L_a	S_{bp}	S_{cp}	D_{bn}	D_{cn}	D_{ap}
120~180	V_{bc}	V_{ac}	L_b	L_a	L_c	S_{bn}	S_{an}	D_{bp}	D_{ap}	D_{cn}
180~240	V_{bc}	V_{ba}	L_c	L_a	L_b	S_{cp}	S_{ap}	D_{cn}	D_{an}	D_{bp}
240~300	V_{ca}	V_{ba}	L_c	L_b	L_a	S_{cn}	S_{bn}	D_{cp}	D_{bp}	D_{an}
300~360	V_{ca}	V_{cb}	L_a	L_b	L_c	S_{ap}	S_{bp}	D_{an}	D_{bn}	D_{cp}

Table 5. The control algorithm for the topologies shown in Fig. 1 (c) and (d).

Region	i_{Lp}	i_{Ln}	i_{Lt}	Q_{ap}	Q_{an}	Q_{bp}	Q_{bn}	Q_{cp}	Q_{cn}
0~60	i_{La}	i_{Lc}	$-i_{Lb}$	0	Q_p	0	0	0	Q_n
60~120	$-i_{Lb}$	$-i_{Lc}$	i_{La}	0	0	Q_p	0	Q_n	0
120~180	i_{Lb}	i_{La}	$-i_{Lc}$	0	Q_n	0	Q_p	0	0
180~240	$-i_{Lc}$	$-i_{La}$	i_{Lb}	Q_n	0	0	0	Q_p	0
240~300	i_{Lc}	i_{Lb}	$-i_{La}$	0	0	0	Q_n	0	Q_p
300~360	$-i_{La}$	$-i_{Lb}$	i_{Lc}	Q_p	0	Q_n	0	0	0

Table 6. The cross-references between the boost rectifier in Fig. 1(b), (e) and the parallel-connected dual-boost topologies.

Region	Topology parameters for rectifier in Fig. 1 (b)					Topology parameters for rectifier in Fig. 1 (e)				
	T_p	T_n	D_p	D_n	D_t	T_p	T_n	D_p	D_n	D_t
0~60	S_a	S_c	D_{ap}	D_{cp}	D_{bn}	S_{a-}	S_{c-}	D_{ap}	D_{cp}	D_{bn}, D_{b-}
60~120	S_b	S_c	D_{bn}	D_{cn}	D_{ap}	S_{b+}	S_{c+}	D_{bn}	D_{cn}	D_{ap}, D_{a+}
120~180	S_b	S_a	D_{bp}	D_{ap}	D_{cn}	S_{b-}	S_{a-}	D_{bp}	D_{ap}	D_{cn}, D_{c-}
180~240	S_c	S_a	D_{cn}	D_{an}	D_{bp}	S_{c+}	S_{a+}	D_{cn}	D_{an}	D_{bp}, D_{b+}
240~300	S_c	S_b	D_{cp}	D_{bp}	D_{an}	S_{c-}	S_{b-}	D_{cp}	D_{bp}	D_{an}, D_{a-}
300~360	S_a	S_b	D_{an}	D_{bn}	D_{cp}	S_{a+}	S_{b+}	D_{an}	D_{bn}	D_{cp}, D_{c+}

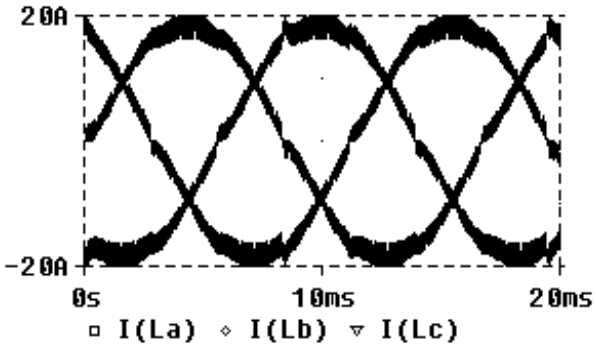


Fig. 14. Simulated current waveforms for three-phase H bridge boost rectifiers shown in Fig. 1 (c) and (d) with proposed general three-phase PFC controller.

6 Conclusion

A new controller for three-phase power-factor correction has been described in this paper. The controller is derived for a parallel-connected dual-boost topology that is a sub-topology for most three-phase boost PFC topologies with a single dc-rail capacitor.

With the proposed controller, low current THD and high power factor can be achieved. Furthermore, because only two switches are operated in high frequency during each 60°, switching losses are reduced significantly. The conduction losses are minimized and the switch current rating is reduced since only a small portion of input current flows into the switches T_p and T_n. All findings are supported by simulation and experiments. The proposed general controller provides a high performance and low cost solution for realizing three-phase power factor correction. The logic circuit may be implemented by a programmable logic circuit. The proposed controller is ready to be integrated into a three-phase PFC control chip.

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