Multicycles Explained

Using TimeQuest Timing Analyzer

Introduction

To properly constrain a design, it is important to provide multicycle assignments to timing-driven compilation. Multicycle assignments relax the timing requirements, thus allowing the fitter a greater degree of freedom. As such, they reduce the overall compilation time and provide greater quality of results. Multicycle assignments are often misunderstood and poorly applied. This Tech Note aims to do the following:

1. Provide a concise definition for multicycles
2. Show the basic types of multicycles with examples
3. Illustrate applications of multicycles in common circuits

All examples will be provided with accompanying analysis in the Altera® Quartus® II TimeQuest Timing Analyzer. It is assumed the reader is familiar with static timing analysis and operation of TimeQuest.

Multicycle Defined

Figure 1 shows a simple circuit[1] for setup and hold slack:

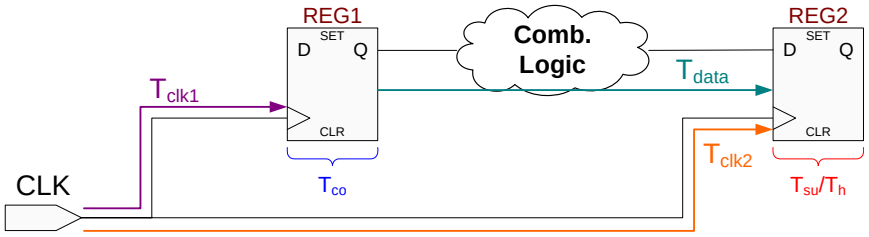


Figure 1. Simple Register-Register Path

Let's begin with a setup check:

$$\text{Setup slack}^{2} = \text{Data Required Time} - \text{Data Arrival Time} \quad [1]$$

$$= (\text{Latch Edge} + T_{clk2}{}^{3} - T_{su}) - (\text{Launch Edge} + T_{clk1}{}^{4} + T_{co} + T_{data}{}^{4}) \quad [2]$$

$$= \underbrace{(\text{Latch Edge} - \text{Launch Edge})}_{\text{Setup Relationship}} + \underbrace{(T_{clk2} - T_{clk1})}_{\text{Clock Skew}} - \underbrace{(T_{co} + T_{data} + T_{su})}_{\text{Data Path}} \quad [3]$$

[1] Simplified circuit shown. REG1/REG2 may be internal or external to FPGA. For example, REG1 could be in an upstream external device or REG2 could be in a downstream external device. Clock source for REG1/REG2 do not necessarily need to be the same. Examples of non-similar clock sources will be shown later in this document.
[2] Clock uncertainty, early & late clock latency ignored for the sake of simplicity.
[3] Minimum delay used
[4] Maximum delay used

where,

T_{clk1}	- propagation delay from clock source to clock input on source register
T_{clk2}	- propagation delay from clock source to clock input on destination register
T_{data}	- propagation delay from source register to data input on destination register
T_{co}	- Clock to output delay of source register
T_{su}	- Setup requirement of destination register
T_h	- Hold requirement of destination register

From equation [3] the setup relationship is the number of clock periods between the latch edge and the launch edge.

Typically for single cycle setup analysis: Latch Edge – Launch Edge = 1 clock cycle

When this relationship is greater than one clock period and an integer multiple of the clock period, then a multicycle setup relationship is said to exist.

Multicycle Setup Relationship: (Latch Edge – Launch Edge) = N*(clock period), N>1 [4]

TimeQuest timing analyzer defaults to single cycle setup analysis. If your design has multicycle relationships, then applying multicycle assignments reduces the timing burden placed upon the fitter. By applying multicycle setup constraints, the setup slack equation is loosened by integer multiples of the clock period.

Multicycle setup constraint is defined as the integer number of clock periods, N, where N>1, to relax the setup slack equation. The default value is one.

Next, let's examine a hold check:

Hold slack[5] = Data Arrival Time - Data Required Time [5]

$= (\text{Launch Edge} + T_{clk1}^{6} + T_{co} + T_{data}^{6}) - (\text{Latch Edge} + T_{clk2}^{7} - T_h)$ [6]

$= \underbrace{(\text{Launch Edge} - \text{Latch Edge})}_{\text{Hold Relationship}} - \underbrace{(T_{clk2} - T_{clk1})}_{\text{Clock Skew}} + \underbrace{(T_{co} + T_{data} - T_h)}_{\text{Data Path}}$ [7]

From equation [7], the hold relationship is the number of clock periods between the latch edge and the launch edge.

Typically for single cycle hold analysis: Launch Edge – Latch Edge = 0 clock cycles

When this relationship is greater than zero clock periods and an integer multiple of the clock period, then a multicycle hold relationship is said to exist.

Multicycle Hold Relationship: (Launch Edge – Latch Edge) = N*(clock period), N>0 [8]

[5] Clock uncertainty, early & late clock latency ignored for sake of simplicity
[6] Minimum delay used
[7] Maximum delay used

As with setup, TimeQuest timing analyzer will default to single cycle hold analysis. If your design has multicycle relationships, then applying multicycle assignments reduces the timing burden placed upon the fitter. By applying multicycle hold constraints, the hold slack equation is loosened by integer multiples of the clock period.

Multicycle hold constraint is defined as the integer number of clock periods, N, where N>0, to relax the hold slack equation. The default value is zero.

TimeQuest Timing Analyzer

TimeQuest timing analyzer will examine all register-to-register paths and perform setup and hold checks. These checks are based upon evaluating the launch and latch edge relationships.

When performing setup checks, for each and every latch edge at the destination register, TimeQuest uses the closest previous clock edge at the source register as the launch edge.

$$\text{Setup Check} = \text{Current Latch Edge} - \text{Closest Previous Launch Edge} \quad [9]$$

When performing hold checks, TimeQuest performs two checks. The first hold check determines that the data launched by the current launch edge is not captured by the previous latch edge. The second hold check determines that the data launched by the next launch edge is not captured by the current latch edge.

$$\text{Hold Check 1} = \text{Current Launch Edge} - \text{Previous Latch Edge} \quad [10]$$
$$\text{Hold Check 2} = \text{Next Launch Edge} - \text{Current Latch Edge} \quad [11]$$

TimeQuest will perform hold checks for every possible setup relationship and not just the worst case setup relationship. Note though, only the worst case relationship is reported.

If hold check overlaps a setup check, then the hold check is ignored.

Types of Multicycles

There are two categories of multicycles:

1. Destination Multicycles: This type of multicycle loosens the slack equation by changing the destination clock edge. i.e. relaxing the latch edge
2. Source Multicycles: This type of multicycle loosens the slack equation by changing the source clock edge. i.e. relaxing the launch edge

For each of these categories, it is further possible to define setup and hold variants. Table 1 summarizes common types of multicycles[8].

Table 1 Multicycle Types

Type	Clock	Timing Check	Shorthand
Destination Multicycle Setup	Destination	Setup	DMS
Destination Multicycle Hold	Destination	Hold	DMH
Source Multicycle Setup	Source	Setup	SMS
Source Multicycle Hold	Source	Hold	SMH

The shorthand in Table 1 will be used for the remainder of this document.

[8] The most commonly used types are shown in Table 1. The set_multicycle_path constraint will support other variants

Basic Cases

In this section, we will examine the application of multicycle assignments to the simple register-register circuit shown in Figure 1. We will go thru the analysis of the type of multicycle assignments defined in Table 1.

Basic Case: Single Cycle

Let's first look at the setup and hold checks performed by TimeQuest during single cycle analysis.

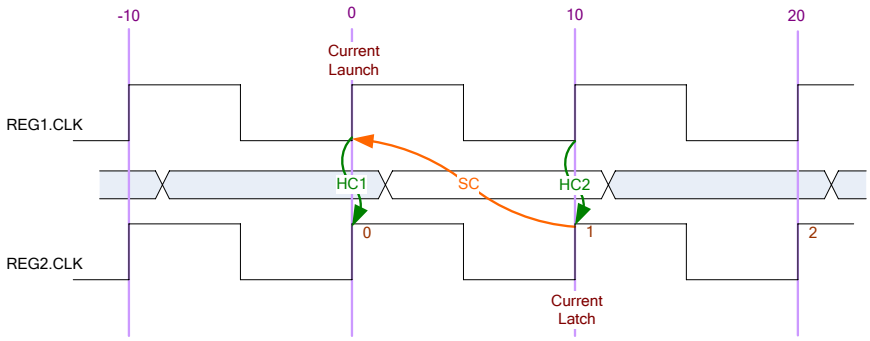


Figure 2 Single Cycle Analysis

Applying equations 9, 10, and 11:

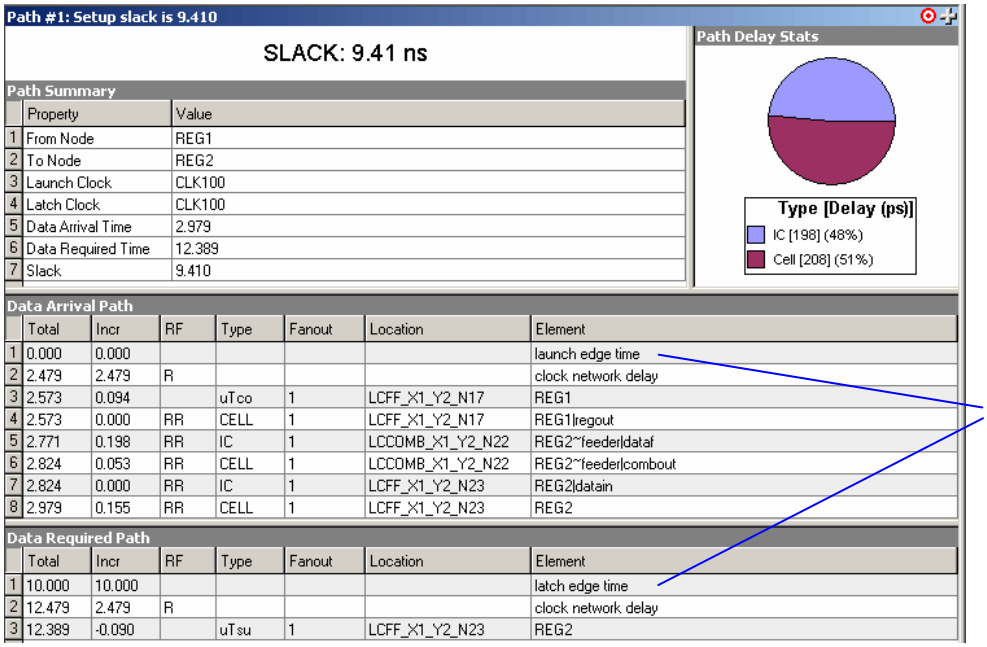
Setup Check = Current Latch Edge – Closest Previous Launch Edge
= 10 ns – 0 ns
= 10 ns

Hold Check 1 = Current Launch Edge – Previous Latch Edge
= 0 ns – 0 ns
= 0 ns

Hold Check 2 = Next Launch Edge – Current Latch Edge
= 10 ns – 10 ns
= 0 ns

Note that both Hold Checks are equivalent in magnitude.

Examining TimeQuest results for setup:



Path #1: Setup slack is 9.410

SLACK: 9.41 ns

Path Delay Stats

Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Data Arrival Time	2.979
6	Data Required Time	12.389
7	Slack	9.410

Data Arrival Path

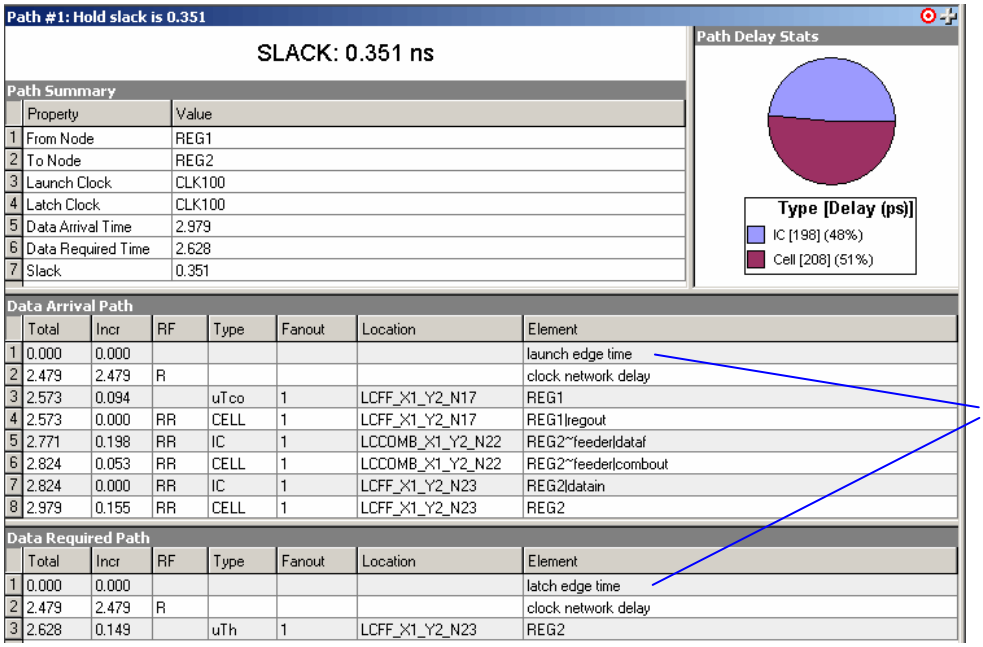
	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	2.479	2.479	R				clock network delay
3	2.573	0.094		uTco	1	LCFF_X1_Y2_N17	REG1
4	2.573	0.000	RR	CELL	1	LCFF_X1_Y2_N17	REG1|regout
5	2.771	0.198	RR	IC	1	LCCOMB_X1_Y2_N22	REG2~feeder|dataf
6	2.824	0.053	RR	CELL	1	LCCOMB_X1_Y2_N22	REG2~feeder|combout
7	2.824	0.000	RR	IC	1	LCFF_X1_Y2_N23	REG2|datain
8	2.979	0.155	RR	CELL	1	LCFF_X1_Y2_N23	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	10.000	10.000					latch edge time
2	12.479	2.479	R				clock network delay
3	12.389	-0.090		uTsu	1	LCFF_X1_Y2_N23	REG2

Latch Edge = 10 ns
Launch Edge = 0 ns
Setup Check = 10 ns

Examining TimeQuest results for hold:



Path #1: Hold slack is 0.351

SLACK: 0.351 ns

Path Delay Stats

Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Data Arrival Time	2.979
6	Data Required Time	2.628
7	Slack	0.351

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	2.479	2.479	R				clock network delay
3	2.573	0.094		uTco	1	LCFF_X1_Y2_N17	REG1
4	2.573	0.000	RR	CELL	1	LCFF_X1_Y2_N17	REG1|regout
5	2.771	0.198	RR	IC	1	LCCOMB_X1_Y2_N22	REG2~feeder|dataf
6	2.824	0.053	RR	CELL	1	LCCOMB_X1_Y2_N22	REG2~feeder|combout
7	2.824	0.000	RR	IC	1	LCFF_X1_Y2_N23	REG2|datain
8	2.979	0.155	RR	CELL	1	LCFF_X1_Y2_N23	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					latch edge time
2	2.479	2.479	R				clock network delay
3	2.628	0.149		uTh	1	LCFF_X1_Y2_N23	REG2

Launch Edge = 0 ns
Latch Edge = 0 ns
Hold Check = 0 ns

TimeQuest timing analyzer does not report both hold checks. It will display the worst case check.

Basic Case: DMS = 2 & DMH = 0

In this case we have a Destination Multicycle Setup, DMS, of 2 and a Destination Multicycle Hold, DMH, of zero. We are relaxing the setup slack equation by latching the data a clock cycle later than the single cycle case. Hold analysis remains single cycle[9].

Figure 3 displays the setup check for this case. Note the latch edge is now a cycle later than the default single cycle analysis. By applying a DMS= 2, the setup relationship will be 20 ns for each and every latch edge.

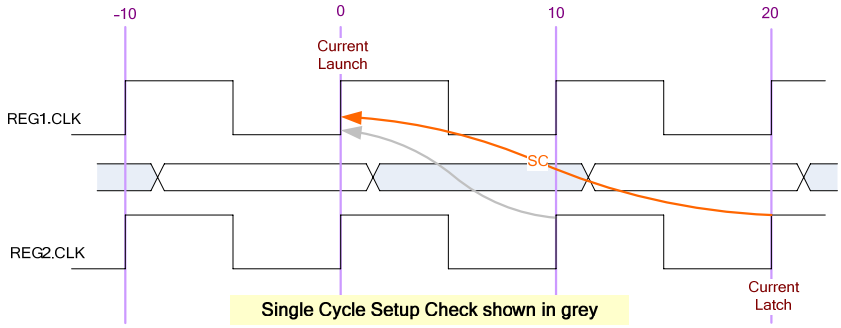


Figure 3 DMS=2, DMH=0 Setup Check

Applying equation 9:

Setup Check = Current Latch Edge[10] – Closest Previous Launch Edge
= 20 ns – 0 ns
= 20 ns

Examining TimeQuest results for setup:

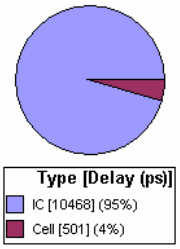
Path #1: Setup slack is 8.847

SLACK: 8.847 ns

Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Multicycle - Setup End	2
6	Data Arrival Time	13.542
7	Data Required Time	22.389
8	Slack	8.847

Path Delay Stats



Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	2.479	2.479	R				clock network delay
3	2.573	0.094		uTco	1	LCFF_X1_Y2_N13	REG1
4	2.573	0.000	RR	CELL	1	LCFF_X1_Y2_N13	REG1|regout
5	13.041	10.468	RR	IC	1	LCCOMB_X1_Y2_N10	REG2~feeder|datab
6	13.387	0.346	RR	CELL	1	LCCOMB_X1_Y2_N10	REG2~feeder|combout
7	13.387	0.000	RR	IC	1	LCFF_X1_Y2_N11	REG2|datain
8	13.542	0.155	RR	CELL	1	LCFF_X1_Y2_N11	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	20.000	20.000					latch edge time
2	22.479	2.479	R				clock network delay
3	22.389	-0.090		uTsu	1	LCFF_X1_Y2_N11	REG2

Latch Edge = 20 ns
Launch Edge = 0 ns
Setup Check = 20 ns

[9] Recall from earlier definition, the default value for hold multicycle is zero.
[10] Adjusted for multicycle assignment

Since Hold analysis remains single cycle, analysis will be consistent with previous discussions on single cycle hold. Figure 4 displays the hold checks for this case. Note hold checks are relative to the setup check. In general Hold checks are performed on every possible setup check and not just to the most conservative setup check edges.

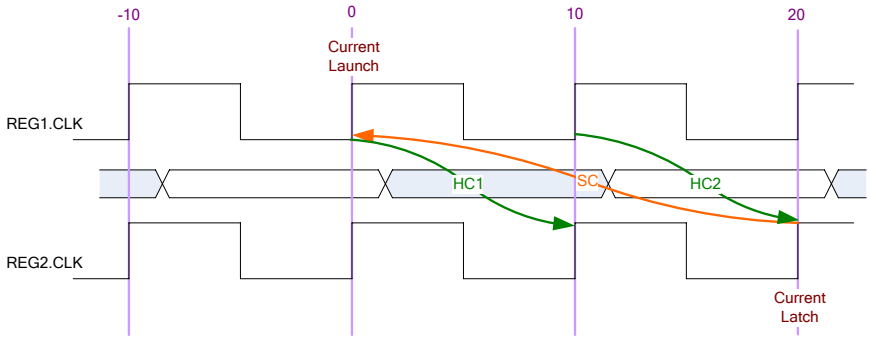


Figure 4 DMS=2, DMH=0 Hold Checks

Applying equations 10 and 11:

Hold Check 1 = Current Launch Edge – Previous Latch Edge
= 0 ns – 10 ns
= -10 ns

Hold Check 2 = Next Launch Edge – Current Latch Edge
= 10 ns – 20 ns
= -10 ns

Note that both Hold Checks are equivalent in magnitude. Examining TimeQuest results for hold:

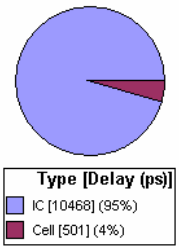
Path #1: Hold slack is 0.914

SLACK: 0.914 ns

Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Multicycle - Setup End	2
6	Data Arrival Time	13.542
7	Data Required Time	12.628
8	Slack	0.914

Path Delay Stats



Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	2.479	2.479	R				clock network delay
3	2.573	0.094		uTco	1	LCFF_X1_Y2_N13	REG1
4	2.573	0.000	RR	CELL	1	LCFF_X1_Y2_N13	REG1|regout
5	13.041	10.468	RR	IC	1	LCCOMB_X1_Y2_N10	REG2~feeder|datab
6	13.387	0.346	RR	CELL	1	LCCOMB_X1_Y2_N10	REG2~feeder|combout
7	13.387	0.000	RR	IC	1	LCFF_X1_Y2_N11	REG2|datain
8	13.542	0.155	RR	CELL	1	LCFF_X1_Y2_N11	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	10.000	10.000					latch edge time
2	12.479	2.479	R				clock network delay
3	12.628	0.149		uTh	1	LCFF_X1_Y2_N11	REG2

Launch Edge = 0 ns
Latch Edge = 10 ns
Hold Check = -10 ns

Basic Case: DMS = 1 & DMH = 1

In this case we have a Destination Multicycle Setup, DMS, of 1 and a Destination Multicycle Hold, DMH, of 1. Setup analysis remains single cycle. For hold slack equation, we are latching the data a clock cycle later than the single cycle case.

Since setup analysis remains single cycle, analysis will be consistent with previous discussions on single cycle setup. Figure 5 displays the setup check for this case.

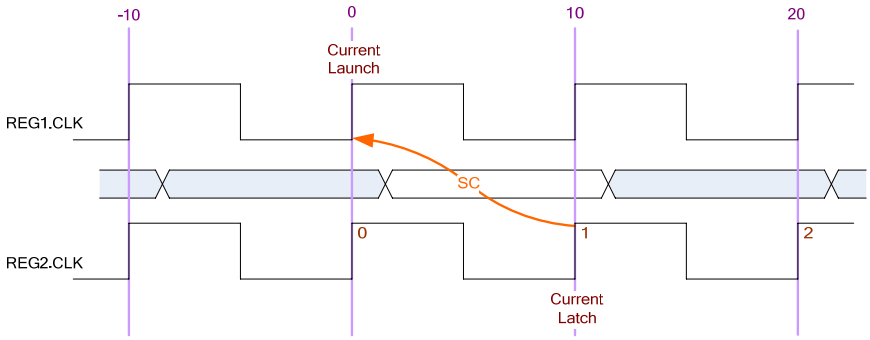


Figure 5 DMS=1, DMH=1 Setup Check

Applying equation 9:

Setup Check = Current Latch Edge – Closest Previous Launch Edge
= 10 ns – 0 ns
= 10 ns

Examining TimeQuest results for Setup:

Path #1: Setup slack is 9.410

SLACK: 9.41 ns

Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Data Arrival Time	2.979
6	Data Required Time	12.389
7	Slack	9.410

Path Delay Stats

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	2.479	2.479	R				clock network delay
3	2.573	0.094		uTco	1	LCFF_X1_Y2_N17	REG1
4	2.573	0.000	RR	CELL	1	LCFF_X1_Y2_N17	REG1|regout
5	2.771	0.198	RR	IC	1	LCCOMB_X1_Y2_N22	REG2~feeder|dataf
6	2.824	0.053	RR	CELL	1	LCCOMB_X1_Y2_N22	REG2~feeder|combout
7	2.824	0.000	RR	IC	1	LCFF_X1_Y2_N23	REG2|datain
8	2.979	0.155	RR	CELL	1	LCFF_X1_Y2_N23	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	10.000	10.000					latch edge time
2	12.479	2.479	R				clock network delay
3	12.389	-0.090		uTsu	1	LCFF_X1_Y2_N23	REG2

Latch Edge = 10 ns
Launch Edge = 0 ns
Setup Check = 10 ns

By applying a DMH=1, the hold relationship will be 10 ns for each and every latch edge. Recall that for single cycle analysis, the hold relationship is 0 ns. Figure 6 displays the hold checks for this case. Note hold checks are relative to the setup check.

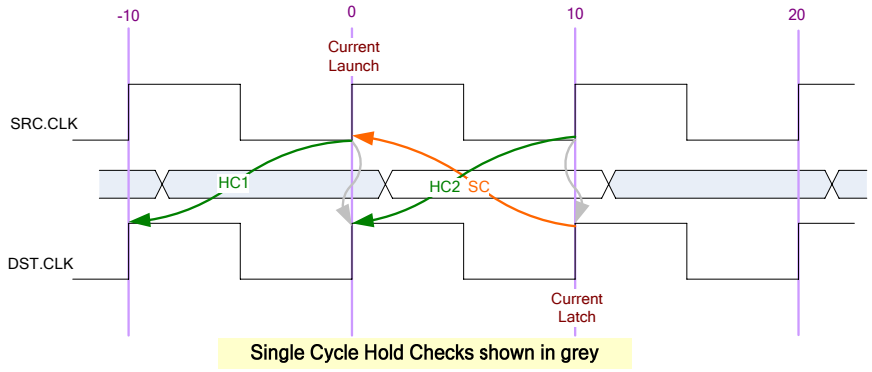


Figure 6 DMS=1, DMH=1 Hold Checks

Applying equations 10 and 11:

Hold Check 1 = Current Launch Edge – Previous Latch Edge[11]
= 0 ns – (-10 ns)[12]
= 10 ns

Hold Check 2 = Next Launch Edge – Current Latch Edge[11]
= 10 ns – 0 ns[12]
= 10 ns

Note that both Hold Checks are equivalent in magnitude. Examining TimeQuest results for hold:

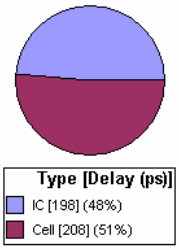
Path #1: Hold slack is 10.351

SLACK: 10.351 ns

Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Multicycle - Hold End	1
6	Data Arrival Time	12.979
7	Data Required Time	2.628
8	Slack	10.351

Path Delay Stats



Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	10.000	10.000					launch edge time
2	12.479	2.479	R				clock network delay
3	12.573	0.094		uTco	1	LCFF_X1_Y2_N17	REG1
4	12.573	0.000	RR	CELL	1	LCFF_X1_Y2_N17	REG1|regout
5	12.771	0.198	RR	IC	1	LCCOMB_X1_Y2_N22	REG2~feeder|dataf
6	12.824	0.053	RR	CELL	1	LCCOMB_X1_Y2_N22	REG2~feeder|combout
7	12.824	0.000	RR	IC	1	LCFF_X1_Y2_N23	REG2|datain
8	12.979	0.155	RR	CELL	1	LCFF_X1_Y2_N23	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					latch edge time
2	2.479	2.479	R				clock network delay
3	2.628	0.149		uTh	1	LCFF_X1_Y2_N23	REG2

Launch Edge = 10 ns
Latch Edge = 0 ns
Hold Check = 10 ns

[11] Adjusted for multicycle assignment
[12] Hold timing is relaxed by moving the clock edge in the opposite direction to Setup.

Basic Case: DMS =2 & DMH = 1

In this case we have a Destination Multicycle Setup, DMS, of 2 and a Destination Multicycle Hold, DMH, of 1. For both setup and hold slack equations, we are latching the data a clock cycle later than the single cycle case.

Figure 7 displays the setup check for this case. Note the latch edge is now a cycle later than the default single cycle analysis. By applying a DMS= 2, the setup relationship will be 20 ns for each and every latch edge.

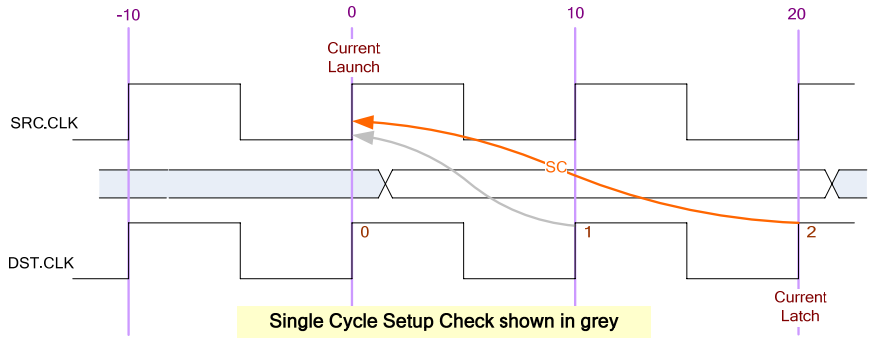


Figure 7 DMS=2, DMH=1 Setup Check

Applying equation 9:

Setup Check = Current Latch Edge[13] – Closest Previous Launch Edge
= 20 ns – 0 ns
= 20 ns

Examining TimeQuest results for setup:

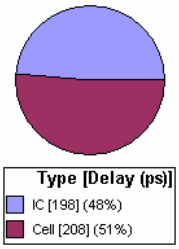
Path #1: Setup slack is 19.410

SLACK: 19.41 ns

Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Multicycle - Setup End	2
6	Data Arrival Time	2.979
7	Data Required Time	22.389
8	Slack	19.410

Path Delay Stats



Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	2.479	2.479	R				clock network delay
3	2.573	0.094		uTco	1	LCFF_X1_Y2_N21	REG1
4	2.573	0.000	RR	CELL	1	LCFF_X1_Y2_N21	REG1|regout
5	2.771	0.198	RR	IC	1	LCCOMB_X1_Y2_N18	REG2~feeder|dataf
6	2.824	0.053	RR	CELL	1	LCCOMB_X1_Y2_N18	REG2~feeder|combout
7	2.824	0.000	RR	IC	1	LCFF_X1_Y2_N19	REG2|datain
8	2.979	0.155	RR	CELL	1	LCFF_X1_Y2_N19	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	20.000	20.000					latch edge time
2	22.479	2.479	R				clock network delay
3	22.389	-0.090		uTsu	1	LCFF_X1_Y2_N19	REG2

Latch Edge = 20 ns
Launch Edge = 0 ns
Setup Check = 20 ns

[13] Adjusted for multicycle assignment

By applying a DMH=1, the hold relationship will be 10 ns for each and every latch edge. Recall that for single cycle analysis, the hold relationship is 0 ns. Figure 8 displays the hold checks for this case. Note hold checks are relative to the setup check.

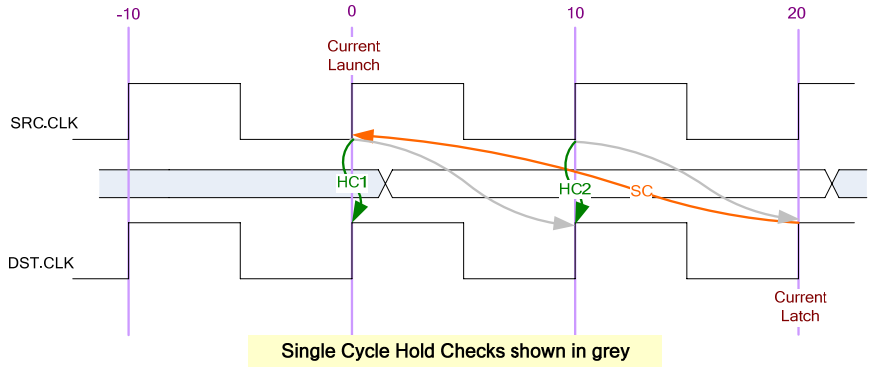


Figure 8 DMS=2, DMH=1 Hold Checks

Applying equations 10 and 11:

Hold Check 1 = Current Launch Edge – Previous Latch Edge[14]
= 0 ns – 0 ns[15]
= 0 ns

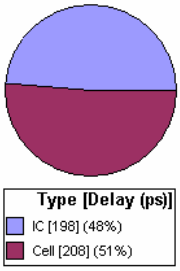
Hold Check 2 = Next Launch Edge – Current Latch Edge[14]
= 10 ns – 10 ns[15]
= 0 ns

Note that both Hold Checks are equivalent in magnitude. Examining TimeQuest results for hold:

Path #1: Hold slack is 0.351

SLACK: 0.351 ns

Path Delay Stats



Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Multicycle - Setup End	2
6	Multicycle - Hold End	1
7	Data Arrival Time	2.979
8	Data Required Time	2.628
9	Slack	0.351

Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	2.479	2.479	R				clock network delay
3	2.573	0.094		uTco	1	LCFF_X1_Y2_N21	REG1
4	2.573	0.000	RR	CELL	1	LCFF_X1_Y2_N21	REG1|regout
5	2.771	0.198	RR	IC	1	LCCOMB_X1_Y2_N18	REG2~feeder|dataf
6	2.824	0.053	RR	CELL	1	LCCOMB_X1_Y2_N18	REG2~feeder|combout
7	2.824	0.000	RR	IC	1	LCFF_X1_Y2_N19	REG2|datain
8	2.979	0.155	RR	CELL	1	LCFF_X1_Y2_N19	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					latch edge time
2	2.479	2.479	R				clock network delay
3	2.628	0.149		uTh	1	LCFF_X1_Y2_N19	REG2

Launch Edge = 0 ns
Latch Edge = 0 ns
Hold Check = 0 ns

[14] Adjusted for multicycle assignment
[15] Hold timing is relaxed by moving the clock edge in the opposite direction to Setup.

Basic Case: SMS = 2 & SMH = 0

In this case we have a Source Multicycle Setup, SMS, of 2 and a Source Multicycle Hold, SMH, of 0. We are relaxing the setup slack equation by launching the data a clock cycle earlier than the single cycle case. Hold analysis remains single cycle.

Figure 9 displays the setup check for this case. Note the launch edge is now a cycle earlier than the default single cycle analysis. By applying a SMS= 2, the setup relationship will be 20 ns for each and every launch edge.

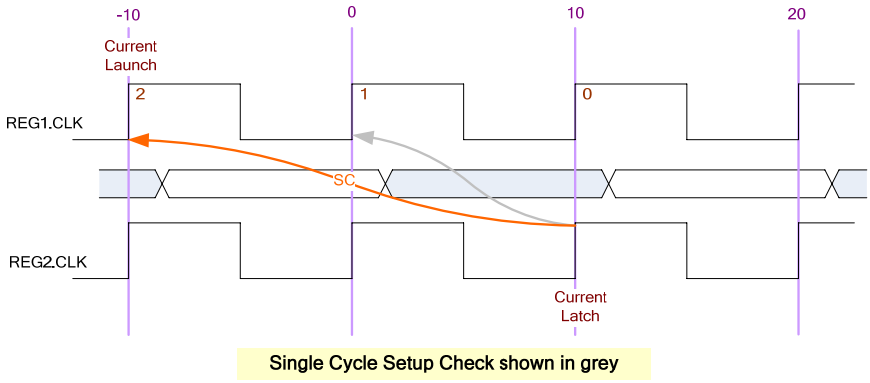


Figure 9 SMS=2, SMH=0 Setup Check

Applying equation 9:

Setup Check = Current Latch Edge – Closest Previous Launch Edge[16]
= 10 ns – (-10 ns)
= 20 ns

Examining TimeQuest results for setup:

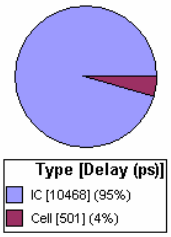
Path #1: Setup slack is 8.847

SLACK: 8.847 ns

Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Multicycle - Setup Start	2
6	Data Arrival Time	13.542
7	Data Required Time	22.389
8	Slack	8.847

Path Delay Stats



Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	2.479	2.479	R				clock network delay
3	2.573	0.094		uTco	1	LCFF_X1_Y2_N13	REG1
4	2.573	0.000	RR	CELL	1	LCFF_X1_Y2_N13	REG1|regout
5	13.041	10.468	RR	IC	1	LCCOMB_X1_Y2_N10	REG2~feeder|datab
6	13.387	0.346	RR	CELL	1	LCCOMB_X1_Y2_N10	REG2~feeder|combout
7	13.387	0.000	RR	IC	1	LCFF_X1_Y2_N11	REG2|datain
8	13.542	0.155	RR	CELL	1	LCFF_X1_Y2_N11	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	20.000	20.000					latch edge time
2	22.479	2.479	R				clock network delay
3	22.389	-0.090		uTsu	1	LCFF_X1_Y2_N11	REG2

Latch Edge = 20 ns
Launch Edge = 0 ns
Setup Check = 20 ns

[16] Adjusted for multicycle assignment

Since Hold analysis remains single cycle, analysis will be consistent with previous discussions on single cycle hold. Figure 10 displays the hold checks for this case. Note hold checks are relative to the setup check.

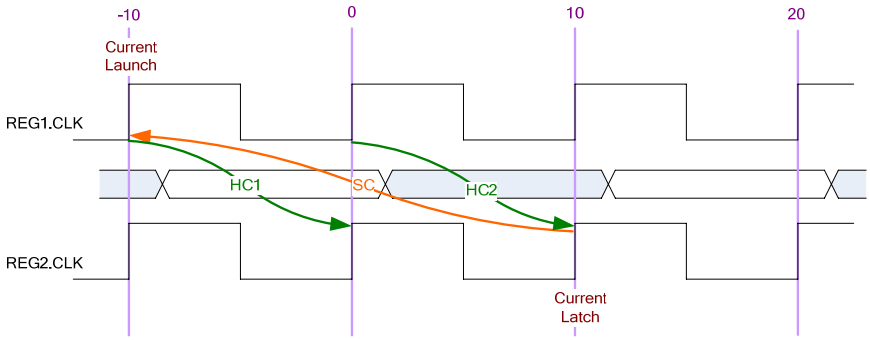


Figure 10 SMS=2, SMH=0 Hold Checks

Applying equations 10 and 11:

Hold Check 1 = Current Launch Edge – Previous Latch Edge
= -10 ns – 0 ns
= -10 ns

Hold Check 2 = Next Launch Edge – Current Latch Edge
= 0 ns – 10 ns
= -10 ns

Note that both Hold Checks are equivalent in magnitude. Examining TimeQuest results for hold:

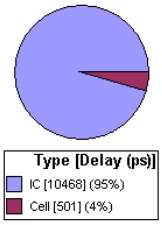
Path #1: Hold slack is 0.914

SLACK: 0.914 ns

Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Multicycle - Setup Start	2
6	Data Arrival Time	13.542
7	Data Required Time	12.628
8	Slack	0.914

Path Delay Stats



Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	2.479	2.479	R				clock network delay
3	2.573	0.094		uTco	1	LCFF_X1_Y2_N13	REG1
4	2.573	0.000	RR	CELL	1	LCFF_X1_Y2_N13	REG1|regout
5	13.041	10.468	RR	IC	1	LCCOMB_X1_Y2_N10	REG2~feeder|datab
6	13.387	0.346	RR	CELL	1	LCCOMB_X1_Y2_N10	REG2~feeder|combout
7	13.387	0.000	RR	IC	1	LCFF_X1_Y2_N11	REG2|datain
8	13.542	0.155	RR	CELL	1	LCFF_X1_Y2_N11	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	10.000	10.000					latch edge time
2	12.479	2.479	R				clock network delay
3	12.628	0.149		uTh	1	LCFF_X1_Y2_N11	REG2

Launch Edge = 0 ns
Latch Edge = 10 ns
Hold Check = -10 ns

Basic Case: SMS = 1 & SMH = 1

In this case we have a Source Multicycle Setup, SMS, of 1 and a Source Multicycle Hold, SMH, of 1. Setup analysis remains single cycle. For hold slack equation, we are launching the data a clock cycle earlier than the single cycle case.

Since setup analysis remains single cycle, analysis will be consistent with previous discussions on single cycle setup. Figure 11 displays the setup check for this case.

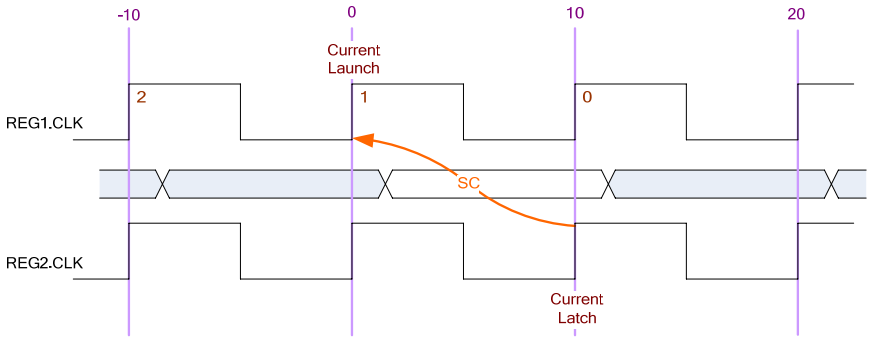


Figure 11 SMS=1, SMH=1 Setup Check

Applying equation 9:

Setup Check = Current Latch Edge – Closest Previous Launch Edge
= 10 ns – 0 ns
= 10 ns

Examining TimeQuest results for Setup:

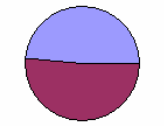
Path #1: Setup slack is 9.410

SLACK: 9.41 ns

Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Data Arrival Time	2.979
6	Data Required Time	12.389
7	Slack	9.410

Path Delay Stats



Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	2.479	2.479	R				clock network delay
3	2.573	0.094		uTco	1	LCFF_X1_Y2_N17	REG1
4	2.573	0.000	RR	CELL	1	LCFF_X1_Y2_N17	REG1|regout
5	2.771	0.198	RR	IC	1	LCCOMB_X1_Y2_N22	REG2~feeder|dataf
6	2.824	0.053	RR	CELL	1	LCCOMB_X1_Y2_N22	REG2~feeder|combout
7	2.824	0.000	RR	IC	1	LCFF_X1_Y2_N23	REG2|datain
8	2.979	0.155	RR	CELL	1	LCFF_X1_Y2_N23	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	10.000	10.000					latch edge time
2	12.479	2.479	R				clock network delay
3	12.389	-0.090		uTsu	1	LCFF_X1_Y2_N23	REG2

Latch Edge = 10 ns
Launch Edge = 0 ns
Setup Check = 10 ns

By applying a SMH=1, the hold relationship will be 10 ns for each and every launch edge. Recall that for single cycle analysis, the hold relationship is 0 ns. Figure 12 displays the hold checks for this case. Note hold checks are relative to the setup check.

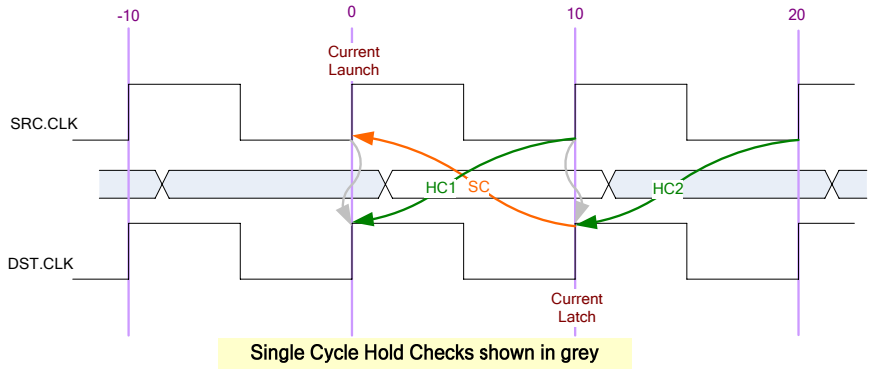


Figure 12 SMS=1, SMH=1 Hold Checks

Applying equations 10 and 11:

Hold Check 1 = Current Launch Edge[17] – Previous Latch Edge
= 10 ns[18] – 0 ns
= 10 ns

Hold Check 2 = Next Launch Edge[17] – Current Latch Edge
= 20 ns[18] – 10 ns
= 10 ns

Note that both Hold Checks are equivalent in magnitude. Examining TimeQuest results for hold:

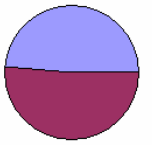
Path #1: Hold slack is 10.351

SLACK: 10.351 ns

Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Multicycle - Hold Start	1
6	Data Arrival Time	12.979
7	Data Required Time	2.628
8	Slack	10.351

Path Delay Stats



Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	10.000	10.000					launch edge time
2	12.479	2.479	R				clock network delay
3	12.573	0.094		uTco	1	LCFF_X1_Y2_N17	REG1
4	12.573	0.000	RR	CELL	1	LCFF_X1_Y2_N17	REG1|regout
5	12.771	0.198	RR	IC	1	LCCOMB_X1_Y2_N22	REG2~feeder|dataf
6	12.824	0.053	RR	CELL	1	LCCOMB_X1_Y2_N22	REG2~feeder|combout
7	12.824	0.000	RR	IC	1	LCFF_X1_Y2_N23	REG2|datain
8	12.979	0.155	RR	CELL	1	LCFF_X1_Y2_N23	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					latch edge time
2	2.479	2.479	R				clock network delay
3	2.628	0.149		uTh	1	LCFF_X1_Y2_N23	REG2

Launch Edge = 10 ns
Latch Edge = 0 ns
Hold Check = 10 ns

[17] Adjusted for multicycle assignment
[18] Hold timing is relaxed by moving the clock edge in the opposite direction to Setup.

Basic Case: SMS = 2 & SMH = 1

In this case we have a Source Multicycle Setup, SMS, of 2 and a Source Multicycle Hold, SMH, of 1. For both setup and hold slack equations, we are launching the data a clock cycle earlier than the single cycle case.

Figure 13 displays the setup check for this case. Note the latch edge is now a cycle later than the default single cycle analysis. By applying a SMS= 2, the setup relationship will be 20 ns for each and every launch edge.

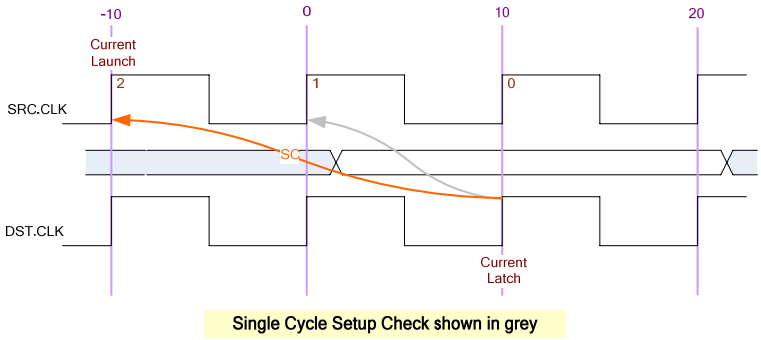


Figure 13 SMS=2, SMH=1 Setup Check

Applying equation 9:

Setup Check = Current Latch Edge – Closest Previous Launch Edge[19]
= 10 ns – (-10 ns)
= 20 ns

Examining TimeQuest results for setup:

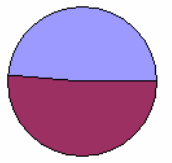
Path #1: Setup slack is 19.410

SLACK: 19.41 ns

Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Multicycle - Setup Start	2
6	Data Arrival Time	2.979
7	Data Required Time	22.389
8	Slack	19.410

Path Delay Stats



Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	2.479	2.479	R				clock network delay
3	2.573	0.094		uTco	1	LCFF_X1_Y2_N21	REG1
4	2.573	0.000	RR	CELL	1	LCFF_X1_Y2_N21	REG1|regout
5	2.771	0.198	RR	IC	1	LCCOMB_X1_Y2_N18	REG2~feeder|dataf
6	2.824	0.053	RR	CELL	1	LCCOMB_X1_Y2_N18	REG2~feeder|combout
7	2.824	0.000	RR	IC	1	LCFF_X1_Y2_N19	REG2|datain
8	2.979	0.155	RR	CELL	1	LCFF_X1_Y2_N19	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	20.000	20.000					latch edge time
2	22.479	2.479	R				clock network delay
3	22.389	-0.090		uTsu	1	LCFF_X1_Y2_N19	REG2

Latch Edge = 20 ns
Launch Edge = 0 ns
Setup Check = 20 ns

[19] Adjusted for multicycle assignment

By applying a SMH=1, the hold relationship will be 10 ns for each and every launch edge. Recall that for single cycle analysis, the hold relationship is 0 ns. Figure 14 displays the hold checks for this case. Note hold checks are relative to the setup check.

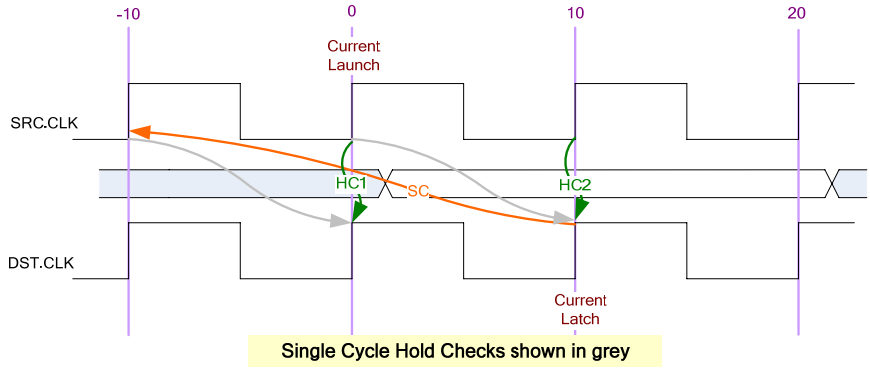


Figure 14 SMS=2, SMH=1 Hold Checks

Applying equations 10 and 11:

Hold Check 1 = Current Launch Edge[20] – Previous Latch Edge
= 0 ns[21] – 0 ns
= 0 ns

Hold Check 2 = Next Launch Edge[20] – Current Latch Edge
= 10 ns[21] – 10 ns
= 0 ns

Note that both Hold Checks are equivalent in magnitude. Examining TimeQuest results for hold:

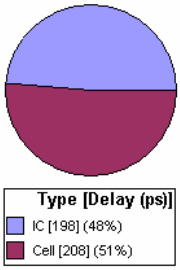
Path #1: Hold slack is 0.351

SLACK: 0.351 ns

Path Summary

	Property	Value
1	From Node	REG1
2	To Node	REG2
3	Launch Clock	CLK100
4	Latch Clock	CLK100
5	Multicycle - Setup Start	2
6	Multicycle - Hold Start	1
7	Data Arrival Time	2.979
8	Data Required Time	2.628
9	Slack	0.351

Path Delay Stats



Data Arrival Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	2.479	2.479	R				clock network delay
3	2.573	0.094		uTco	1	LCFF_X1_Y2_N21	REG1
4	2.573	0.000	RR	CELL	1	LCFF_X1_Y2_N21	REG1|regout
5	2.771	0.198	RR	IC	1	LCCOMB_X1_Y2_N18	REG2~feeder|dataf
6	2.824	0.053	RR	CELL	1	LCCOMB_X1_Y2_N18	REG2~feeder|combout
7	2.824	0.000	RR	IC	1	LCFF_X1_Y2_N19	REG2|datain
8	2.979	0.155	RR	CELL	1	LCFF_X1_Y2_N19	REG2

Data Required Path

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					latch edge time
2	2.479	2.479	R				clock network delay
3	2.628	0.149		uTh	1	LCFF_X1_Y2_N19	REG2

Launch Edge = 0 ns
Latch Edge = 0 ns
Hold Check = 0 ns

[20] Adjusted for multicycle assignment
[21] Hold timing is relaxed by moving the clock edge in the opposite direction to Setup.

Applications

In this section, we will examine common cases where multicycle constraints should be applied. All of these cases are between related clock domains. If your design contains related clocks, for example PLL clocks and there are paths between the related clock domains, then multicycle constraints are applicable.

Case 1: $Freq_{DST} = Freq_{SRC} + Offset$

In this case, the source and destination clocks are the same frequency. However the destination clock is offset with a positive phase shift.

Figure 15 shows the default setup analysis performed by TimeQuest. Assume 2 ns offset for the purposes of this discussion.

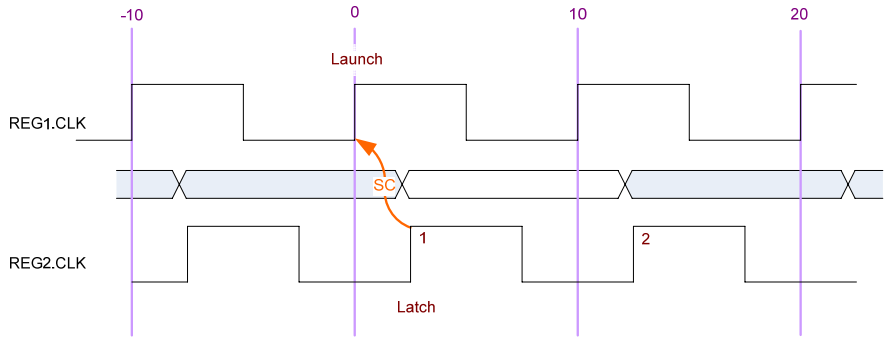


Figure 15 Case 1 – Default Setup Analysis

Applying equation 9:

Setup Check = Current Latch Edge – Closest Previous Launch Edge
= 2 ns – 0 ns
= 2 ns

In general, the setup relationship shown in Figure 15 is not the correct setup relationship required for typical circuits. Usually the desired setup relationship is as shown in Figure 16:

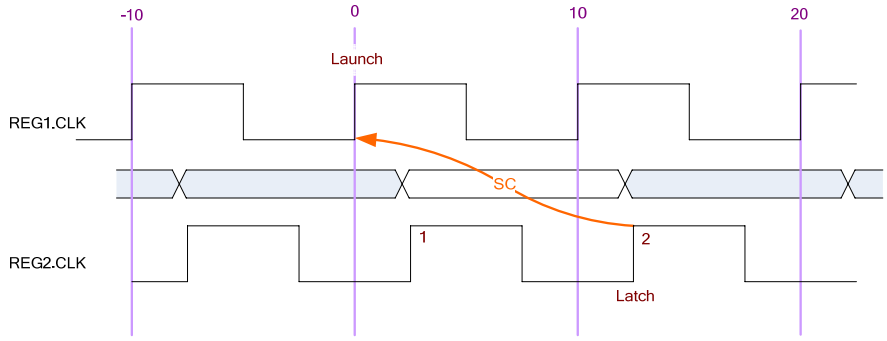


Figure 16 Case 1 – Desired Setup Analysis

To correct the default analysis, multicycle setup assignments must be applied.

For Desired Setup Analysis, DMS = 2 must be applied.

Next, let's look at the hold analysis for this case with DMS=2 applied. Figure 17 shows the hold analysis:

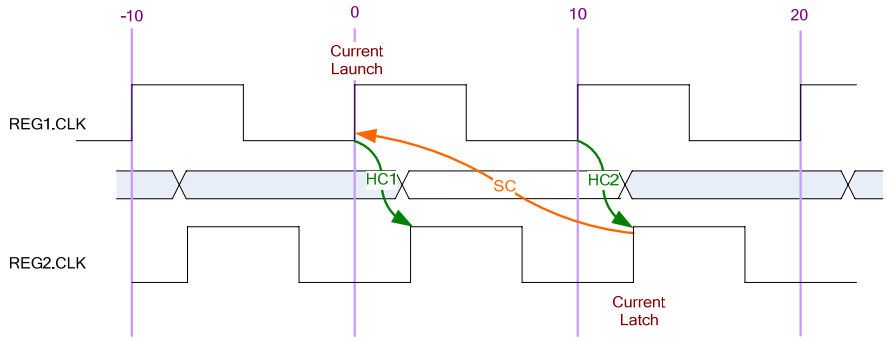


Figure 17 Case 1 – Hold Analysis

Applying equations 10 and 11:

Hold Check 1 = Current Launch Edge – Previous Latch Edge
= 0 ns – 2 ns
= 2 ns

Hold Check 2 = Next Launch Edge – Current Latch Edge
= 10 ns – 12 ns
= 2 ns

The default hold analysis is correct. As such nothing further needs to be done. A DMH = 0 can be applied for completeness.

Now the question needs to be asked: *What if there is a negative phase shift?*

Figure 18 depicts this case and the associated setup and hold analysis.

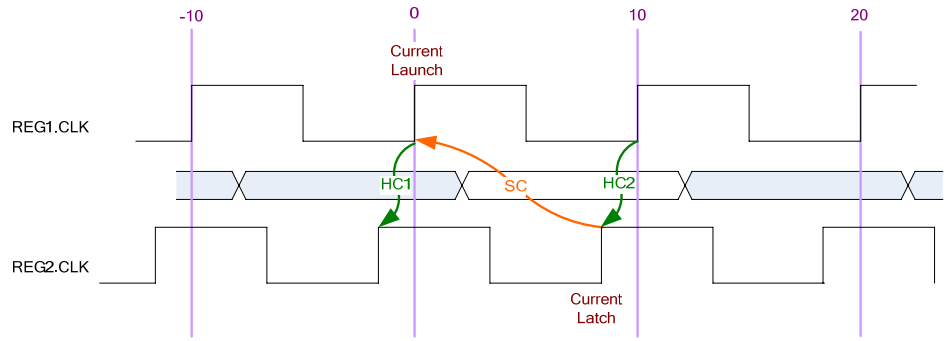


Figure 18 Negative Phase Offset Case

Clearly the default analysis is correct. No multicycles assignments are needed in this case.

Summary

- Destination clock is a positive phase shifted version of the source clock
- For correct analysis, the following are applicable:
  - DMS = 2
  - DMH = 0
- For negative phase shift, depending on amount of shift, multicycles may not be required.

Case 2: $Freq_{DST} = N*Freq_{SRC}$, N>1

In this case, the destination clock is an integer multiple of the source clock frequency. Figure 19 shows the default setup analysis performed by TimeQuest.

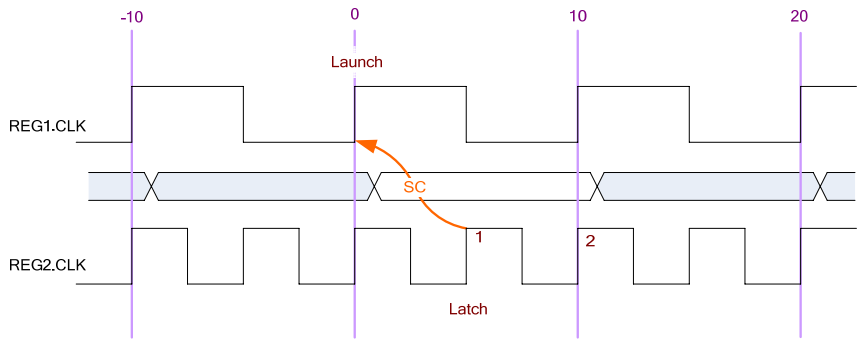


Figure 19 Case 2 – Default Setup Analysis

Applying equation 9:

Setup Check = Current Latch Edge – Closest Previous Launch Edge
= 5 ns – 0 ns
= 5 ns

Note that the data is not changing at edge 1 but rather at edge 2. Therefore, it is possible to relax the setup requirement by shifting the latch edge one clock period. The desired setup relationship is as shown in Figure 20:

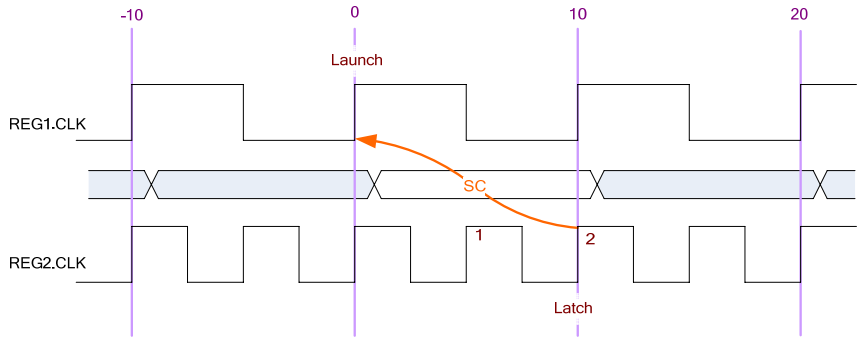


Figure 20 Case 2 – Desired Setup Analysis

To correct the default analysis, multicycle setup assignments must be applied.

For Desired Setup Analysis, DMS = 2 must be applied.
Or For the more general case, DMS = N, where N>1 & N = integer multiplication factor.

Next, let's look at the hold analysis for this case with DMS=2 applied. Figure 21 shows the default hold analysis.

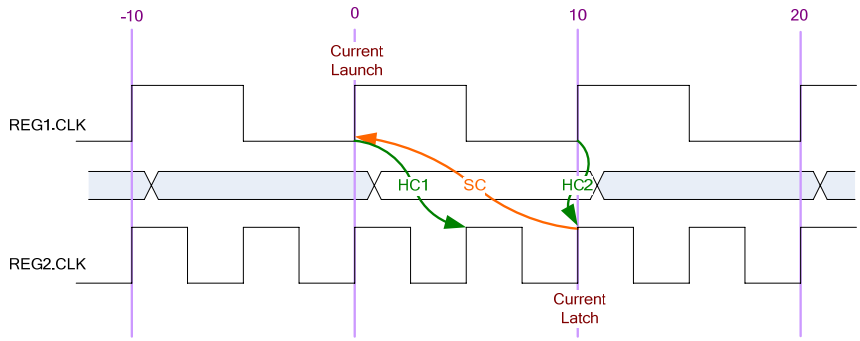


Figure 21 Case 2 – Default Hold Analysis

Applying equations 10 and 11:

Hold Check 1 = Current Launch Edge – Previous Latch Edge
= 0 ns – 5 ns
= 5 ns

Hold Check 2 = Next Launch Edge – Current Latch Edge
= 10 ns – 10 ns
= 0 ns

Note Hold Check 1 is too restrictive. The data is launched by the edge at time 0 ns and should check against data capture by the previous latch edge at time 0 ns, not as depicted by HC1. To correct this, multicycle hold assignments must be applied.

For Desired Hold Analysis, DMH = 1 must be applied.
Or For the more general case, DMH = N-1, where N>1& N = integer multiplication factor

Summary

- Destination clock is an integer multiple, N, of the source clock
- For correct analysis, the following are applicable:
  - DMS = N
  - DMH = N-1

Case 3: $Freq_{DST} = N*Freq_{SRC} + Offset$, N>1

In this case, we have a combination of case 1 and case 2. The destination clock is an integer multiple of the source clock frequency with a positive phase shift. Figure 22 shows the default setup analysis performed by TimeQuest. Assume 2 ns offset for the purposes of this discussion.

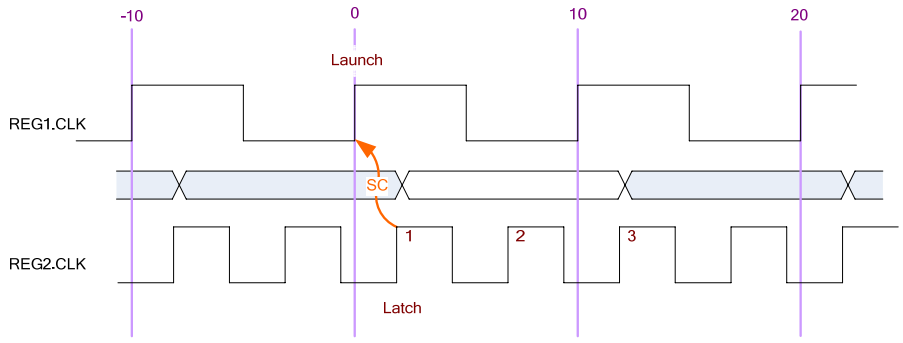


Figure 22 Case 3 – Default Setup Analysis

Applying equation 9:

Setup Check = Current Latch Edge – Closest Previous Launch Edge
= 2 ns – 0 ns
= 2 ns

As with the previous cases, it is possible to relax the setup requirement by correcting for the offset and shifting the latch edge two clock periods. The desired setup relationship is as shown in Figure 23

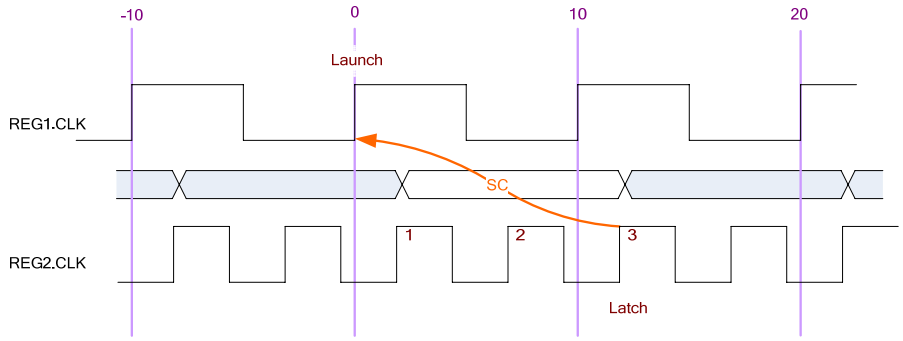


Figure 23 Case 3 – Desired Setup Analysis

To correct the default analysis, multicycle setup assignments must be applied.

For Desired Setup Analysis, DMS = 3 must be applied.
Or For the more general case, DMS = N+1, where N>1 & N = integer multiplication factor.

Next, let's look at the hold analysis for this case with DMS=2 applied. Figure 21 shows the default hold analysis.

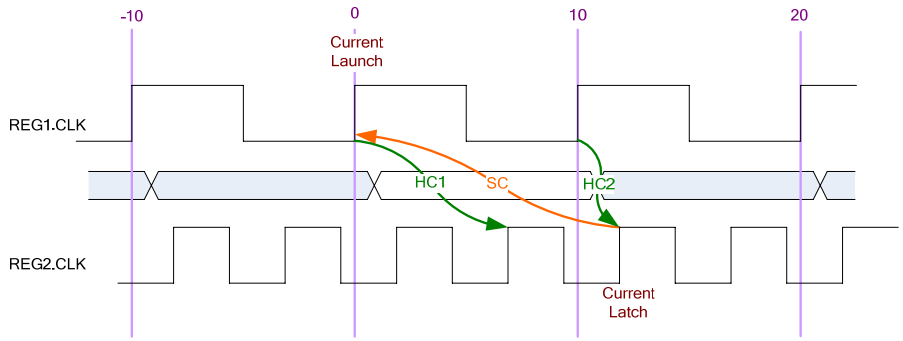


Figure 24 Case 2 – Default Hold Analysis

Applying equations 10 and 11:

Hold Check 1 = Current Launch Edge – Previous Latch Edge
= 0 ns – 5 ns
= 5 ns

Hold Check 2 = Next Launch Edge – Current Latch Edge
= 10 ns – 10 ns
= 0 ns

Note Hold Check 1 is too restrictive. The data is launched by the edge at time 0 ns and should check against data capture by the previous latch edge at time 2 ns, not as depicted by HC1. To correct this, multicycle hold assignments must be applied.

For Desired Hold Analysis, DMH = 1 must be applied.
Or For the more general case, DMH = N-1, where N>1 & N = integer multiplication factor

Summary

- Destination clock is an integer multiple, N, of the source clock with positive offset
- For correct analysis, the following are applicable:
  - DMS = N+1
  - DMH = N-1

Case 4: $Freq_{DST} = Freq_{SRC} /N, N>1$

In this case, the destination clock is an integer divisor of the source clock frequency. Figure 25 shows the default setup analysis performed by TimeQuest.

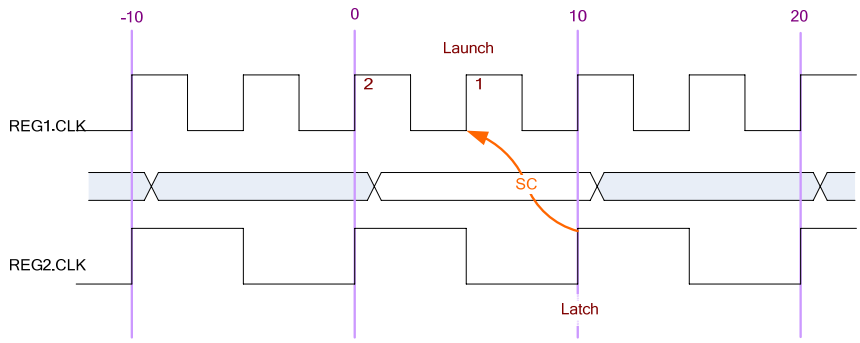


Figure 25 Case 4 – Default Setup Analysis

Applying equation 9:

Setup Check = Current Latch Edge – Closest Previous Launch Edge
= 10 ns – 5 ns
= 5 ns

Note that the data is not launched at edge 1 but rather at edge 2. Therefore it is possible to relax the setup requirement by shifting the launch edge one clock period. The desired setup relationship is as shown in Figure 26

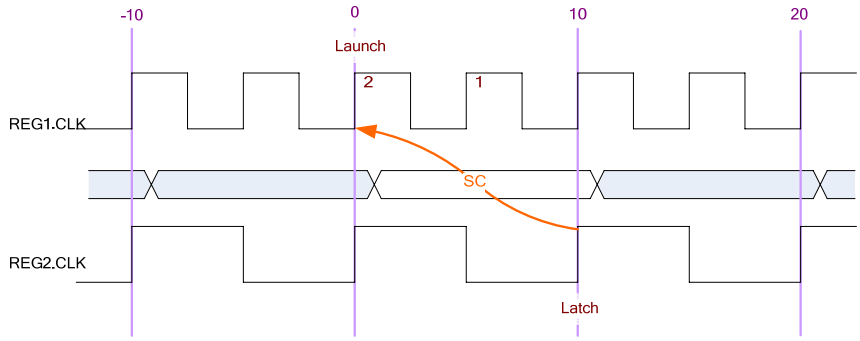


Figure 26 Case 4 – Desired Setup Analysis

To correct the default analysis, multicycle setup assignments must be applied.

For Desired Setup Analysis, SMS = 2 must be applied.
Or For the more general case, SMS = N, where N>1 & N = integer divisor factor.

Next, let's look at the hold analysis for this case with SMS=2 applied. Figure 27 shows the default hold analysis.

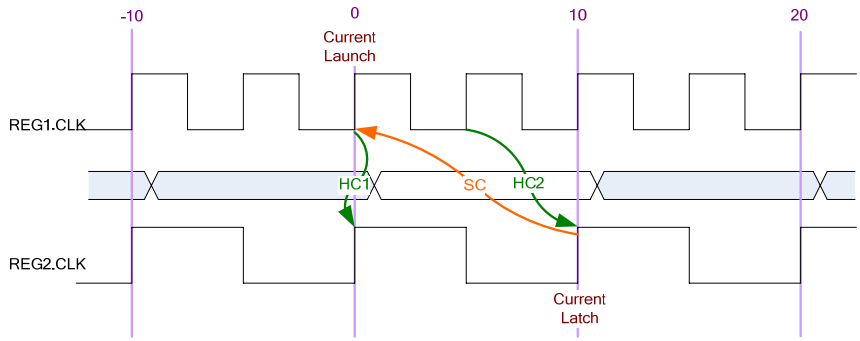


Figure 27 Case 4 – Default Hold Analysis

Applying equations 10 and 11:

Hold Check 1 = Current Launch Edge – Previous Latch Edge
= 0 ns – 0 ns
= 0 ns

Hold Check 2 = Next Launch Edge – Current Latch Edge
= 5 ns – 10 ns
= -5 ns

Note Hold Check 2 is too restrictive. The data is launched next by the edge at time 10 ns and should check against data capture by the current latch edge at time 10 ns, not as depicted by HC2. To correct this, multicycle hold assignments must be applied.

For Desired Hold Analysis, SMH = 1 must be applied.
Or For the more general case, SMH = N-1, where N>1 & N = integer divisor factor

Summary

- Destination clock is an integer divisor, N, of the source clock
- For correct analysis, the following are applicable:
  - SMS = N
  - SMH = N-1

Case 5: $Freq_{DST} = Freq_{SRC} /N + Offset, N>1$

In this case, the destination clock is an integer divisor of the source clock frequency plus positive phase offset. Figure 28 shows the default setup analysis performed by TimeQuest. Assume 2 ns offset for the purposes of this discussion.

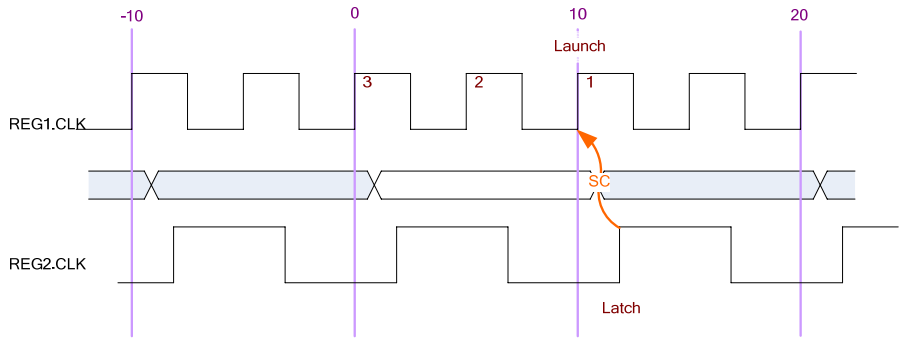


Figure 28 Case 5 – Default Setup Analysis

Applying equation 9:

Setup Check = Current Latch Edge – Closest Previous Launch Edge
= 12 ns – 10 ns
= 2 ns

Note that the data is not launched at edge 1 but rather at edge 3. Therefore it is possible to relax the setup requirement by shifting the launch edge two clock periods. The desired setup relationship is as shown in Figure 29:

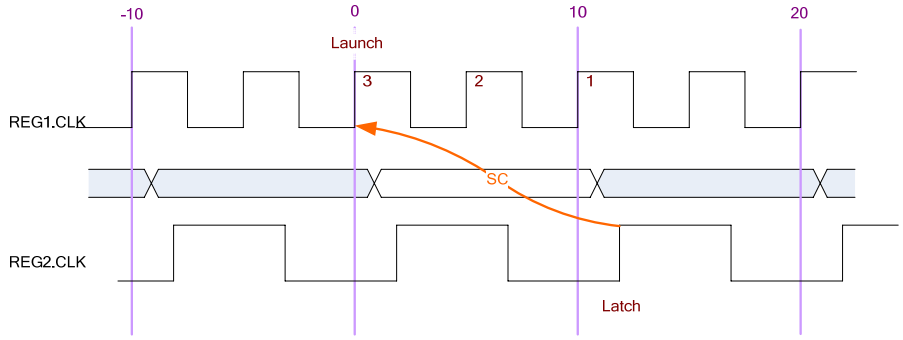


Figure 29 Case 5 – Desired Setup Analysis

To correct the default analysis, multicycle assignments must be applied.

For Desired Setup Analysis, SMS = 3 must be applied.
Or For the more general case, SMS = N+1, where N>1 & N = integer divisor factor.

Next, let's look at the hold analysis for this case with SMS=3 applied. Figure 30 shows the default hold analysis.

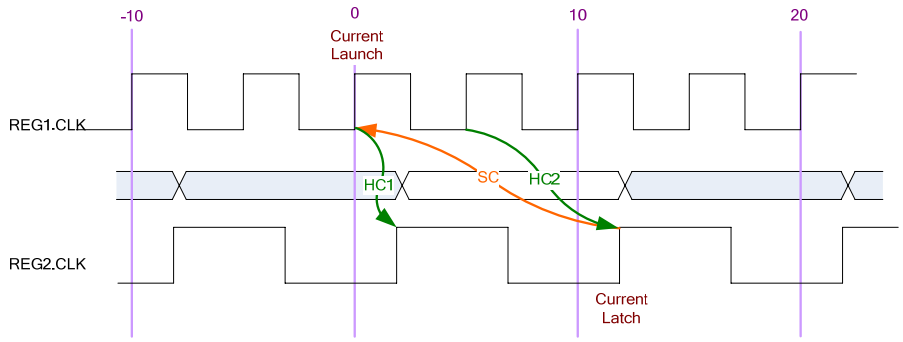


Figure 30 Case 5 – Default Hold Analysis

Applying equations 10 and 11:

Hold Check 1 = Current Launch Edge – Previous Latch Edge
= 0 ns – 2 ns
= -2 ns

Hold Check 2 = Next Launch Edge – Current Latch Edge
= 5 ns – 12 ns
= -7 ns

Note Hold Check 2 is too restrictive. The data is launched next by the edge at time 10 ns and should check against data capture by the current latch edge at time 12 ns, not as depicted by HC2. To correct this, multicycle hold assignments must be applied.

For Desired Hold Analysis, SMH = 1 must be applied.
Or For the more general case, SMH = N-1, where N>1 & N=integer divisor factor

Summary

- Destination clock is an integer divisor, N, of the source clock
- For correct analysis, the following are applicable:
  - SMS = N+1
  - SMH = N-1