Cadence Academic Network Certification Program

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Presentation Contents

- What the certification program offers
- Information about the certification

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    II. iLS training classes
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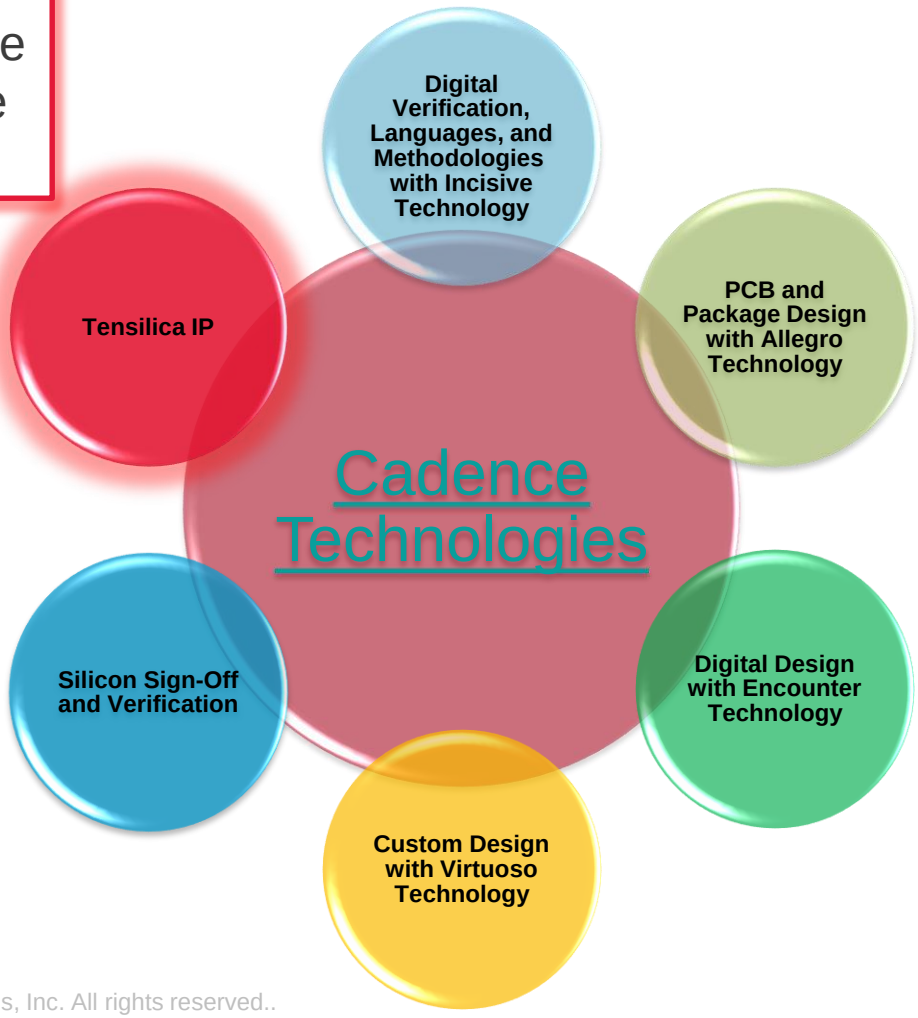
- Certified Universities
- Frequently Asked Questions

Benefits of Certification

- Get comprehensive knowledge of Cadence's state of the art technology in order to **keep a high quality standard in education**
- Share our **leading edge industry standard technology** in the area of electronic design automation with your students
- Be **recognized as experts** in a certain Cadence technology

STEP 1: Choose one or more Cadence Technologies to be certified

Use the **latest versions** of Cadence Products used in the lab



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STEP 2: Selecting a group of lab instructors

The Lab Instructors will be in charge as **instructors** in the Program and they will receive a certificate as **Cadence Certified Lab Instructor**:

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Cadence Internet Learning Series training classes

In order to become **certified**, the lab instructors must **accomplish** a number of iLS training classes.

The **Internet Learning Series** training classes (**iLS**):

These are self-paced, online training courses. Unlike the conventional instructor-led courses, each course can be undertaken at the end-user's **normal working location**, over an **extended period of time**. The iLS courses include:

- Dynamic course content
- Downloadable labs
- Instructor Notes
- Bulletin boards

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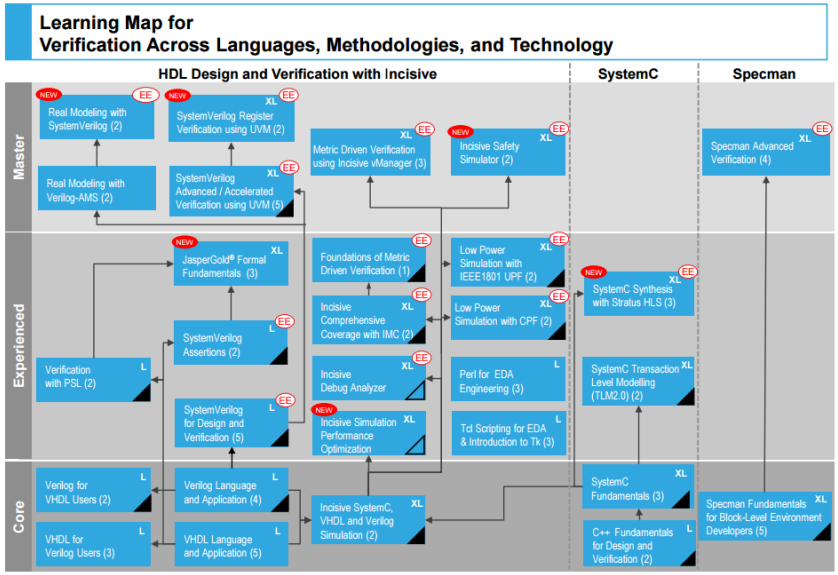
Cadence Internet Learning Series training classes

The **Internet Learning Series** training classes (**iLS**):

They include 3 levels of difficulty:

- **Core**: These are the **foundation courses** that someone needs to fulfil in order to continue their training.
- **Experienced**: The **2nd level** of iLS courses is targeted at those who have completed the core courses.
- **Master**: The 3rd and **final level** of the Internet Learning Series.



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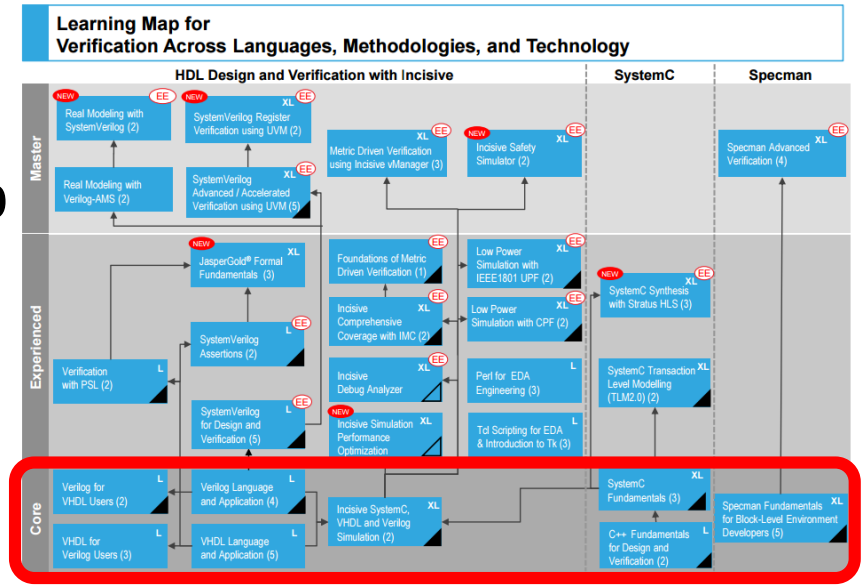
Cadence Internet Learning Series training classes

The **Internet Learning Series** training classes (**iLS**):

They include 3 levels of difficulty:

- **Core**: These the **foundation courses** that someone needs to fulfil in order to continue their training.

  In order to be certified you only need to complete the Core courses of the iLS learning map!



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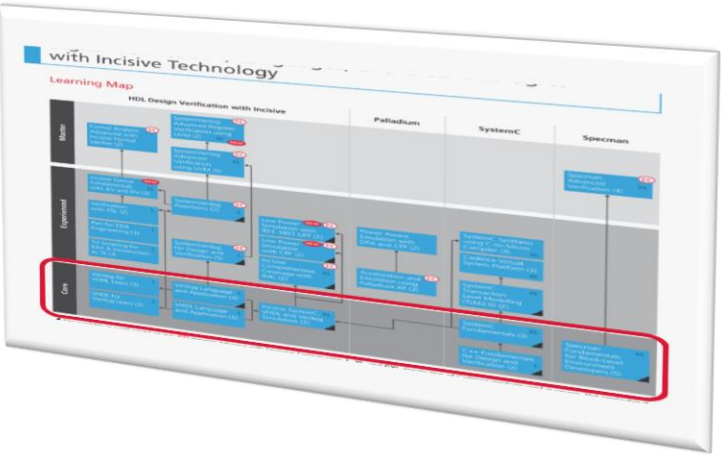
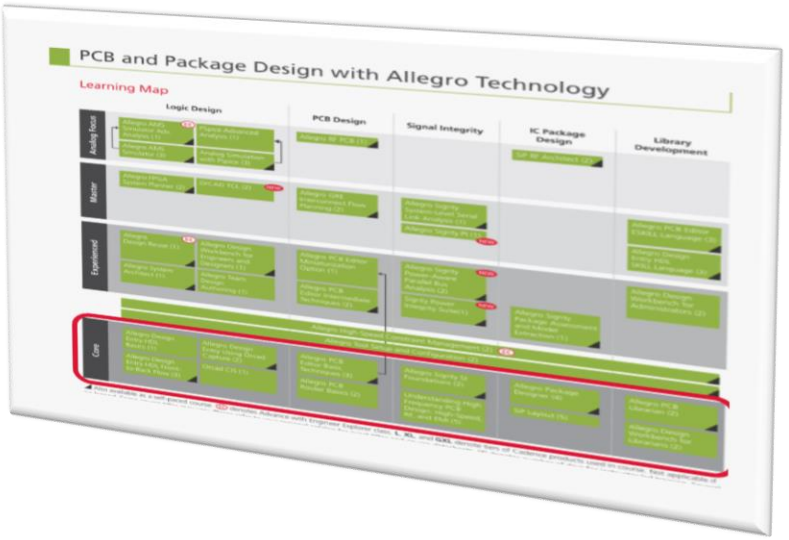
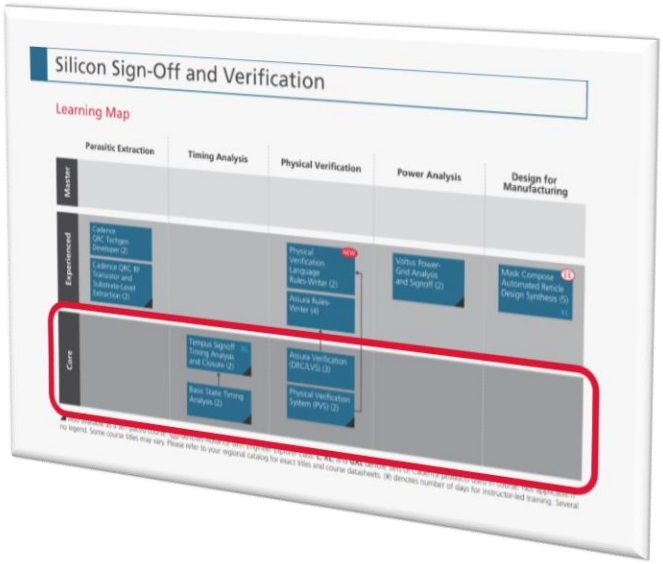
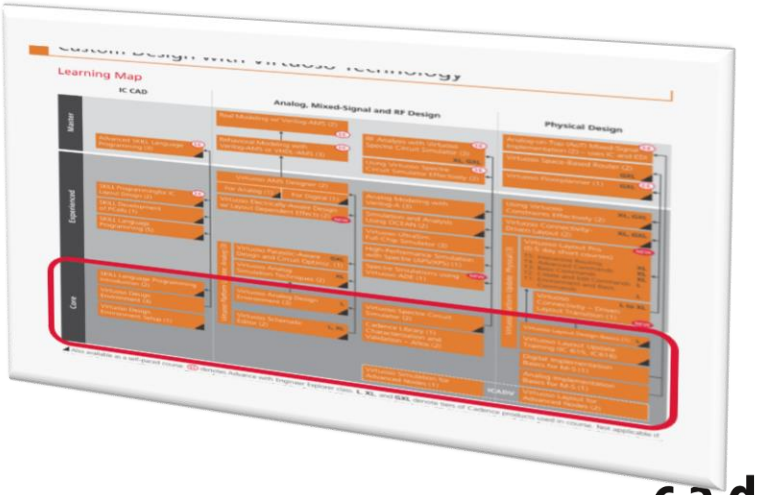
STEP 3: Attend and pass all the required iLS courses for the selected Cadence Technology









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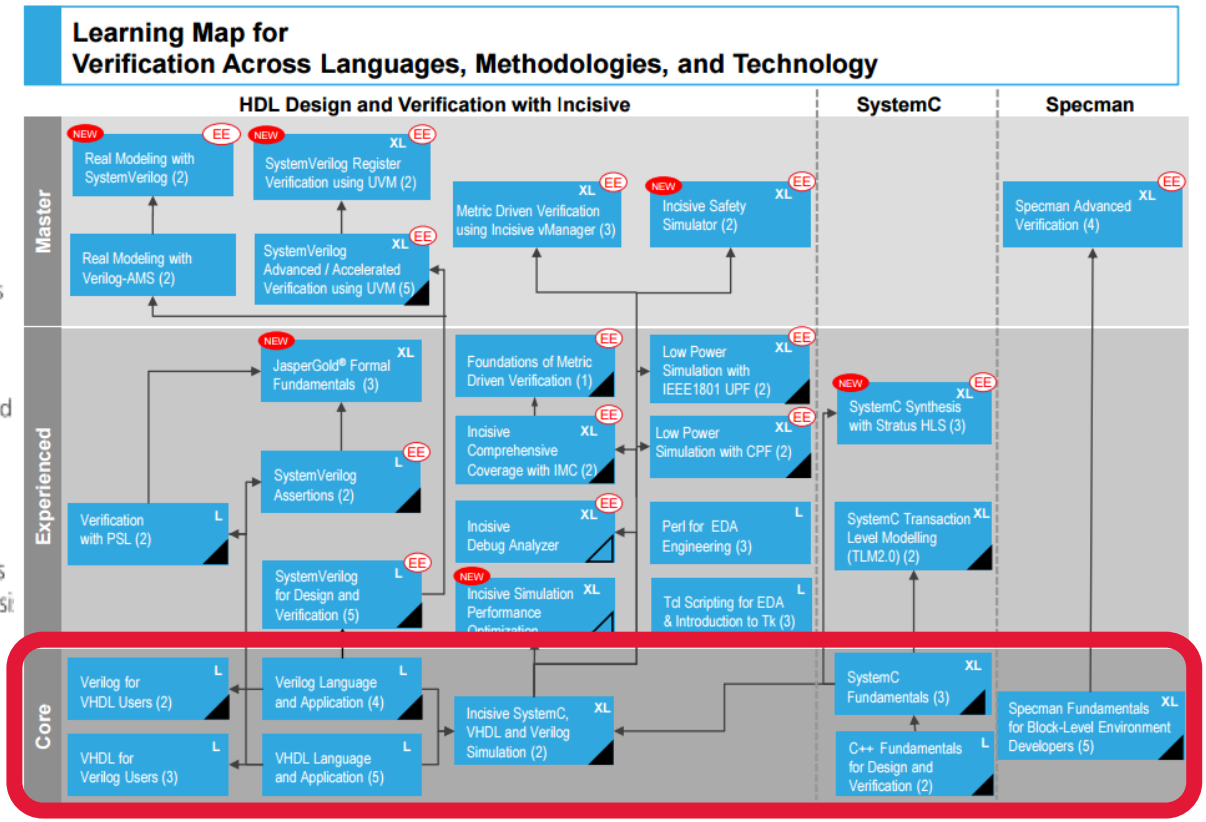
The required sub topics for Incisive Technology

Course Descriptions

HDL Design and Verification

Verilog Language and Application: This course provides a solid background in the use and application of Verilog to digital hardware design. This training package covers all aspects of the language, from basic concepts and syntax, through synthesis coding styles and guidelines, to advanced language constructs and design verification.

Incisive SystemC, VHDL, and Verilog Simulation: This course addresses Incisive® mixed-language (SystemC, VHDL, and Verilog) event-driven digital simulation. The course steps you through compilation, elaboration, simulation, and analysi explaining the most popular options at each step.



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The required sub topics for Incisive Technology

Course Descriptions

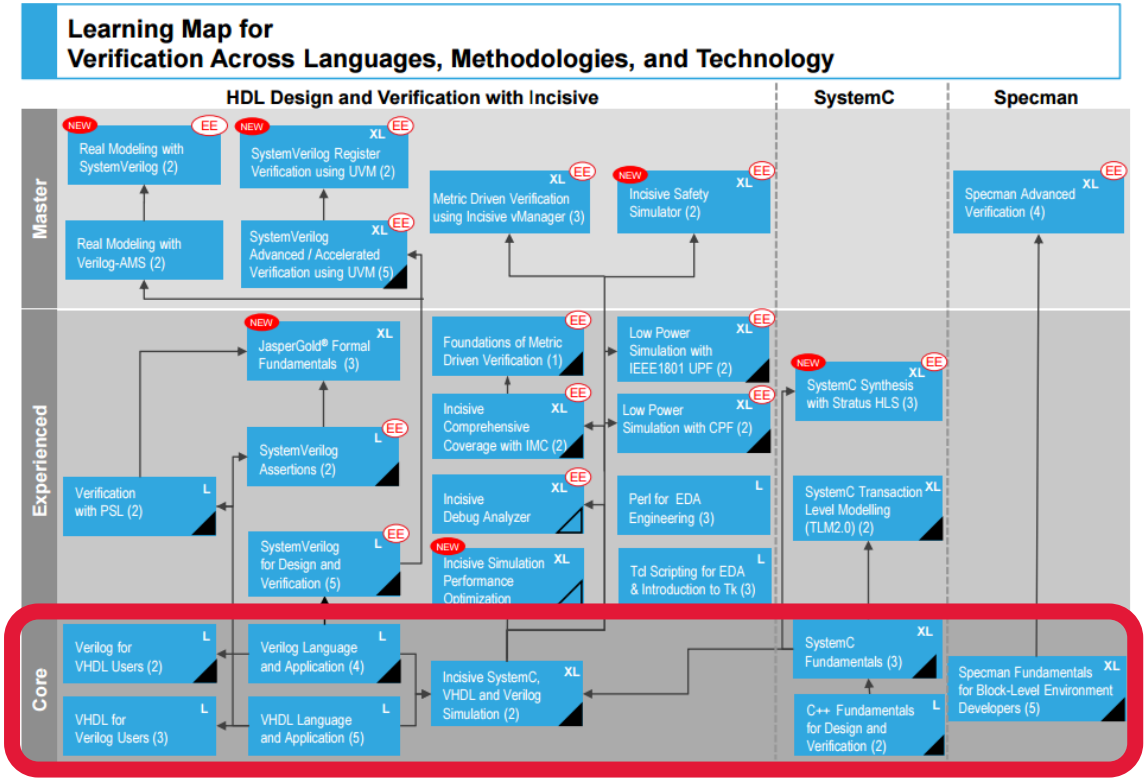
SystemC

C++ Language Fundamentals for Design and Verification: This course provides an introduction to the C++ programming language for design and verification engineers, covering classes, variables and functions, constructors, destructors, inheritance and polymorphism.

SystemC Language Fundamentals: This course teaches the IEEE standard 1666-2005 SystemC language and explores how it can be used for system, hardware, and verification modeling.

Specman

Specman Fundamentals for Block-Level Environment Developers: This course is an introduction to the e language and the Incisive Enterprise Specman Elite Simulator. The course is based on a coverage-driven verification methodology, which is applicable for a broad range of designs. The course shows how to create a reusable, block- level verification environment and then how to instantiate, customize, and write tests for this environment. The verification methodology taught by this class is compatible with the Universal Verification Methodology (UVM).



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The required sub topics for Allegro Technology

Course Descriptions

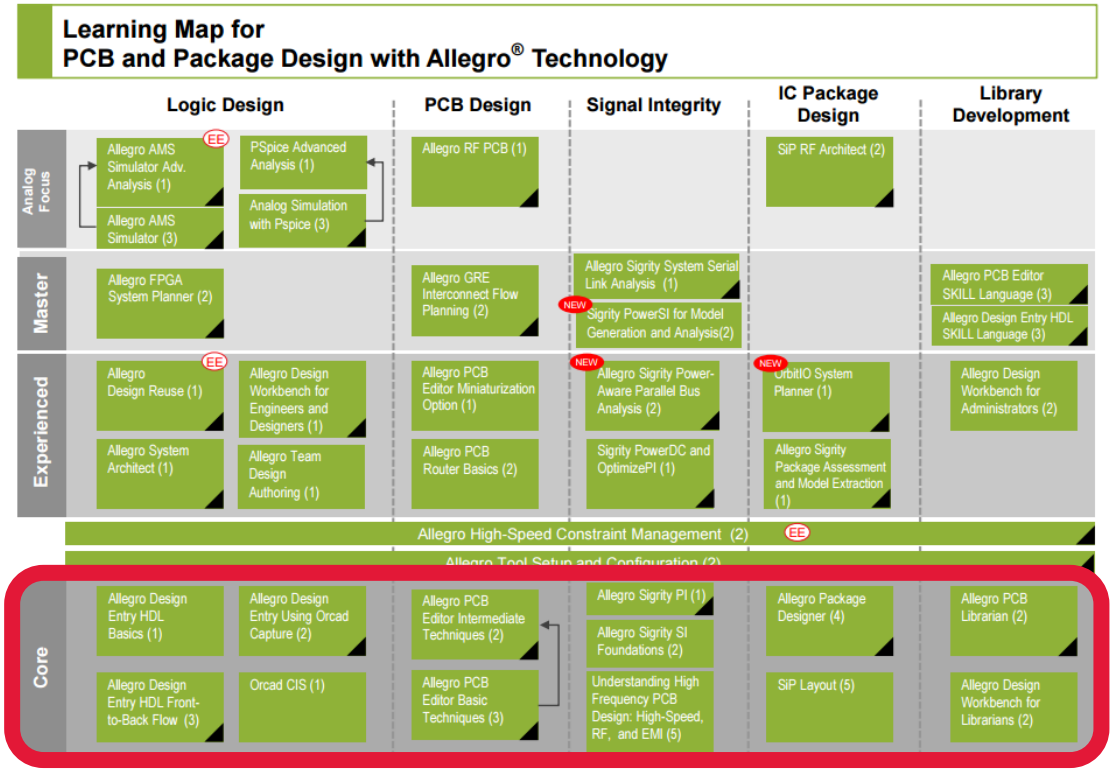
Logic Design

Allegro Design Entry HDL Front-to-Back Flow: This course teaches you how to create board-level schematic designs and demonstrates the integration between Design Entry HDL and other tools in the design flow, including the PCB Editor.

Allegro Design Entry Using OrCAD Capture/OrCAD Capture CIS: This course covers front-end design processes such as setting up design templates, creating a netlist for board layout, and part management. The OrCAD® Capture CIS class covers the CIS database, adding parts to the schematic, and modifying part properties.

PCB Design

Allegro PCB Editor Basic Techniques: This course covers all the necessary steps for designing a PCB, from loading logic and netlist data, through producing manufacturing/NC output. This course is a prerequisite to the Allegro PCB Editor Intermediate Techniques course.



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The required sub topics for Allegro Technology

Course Descriptions

Signal Integrity

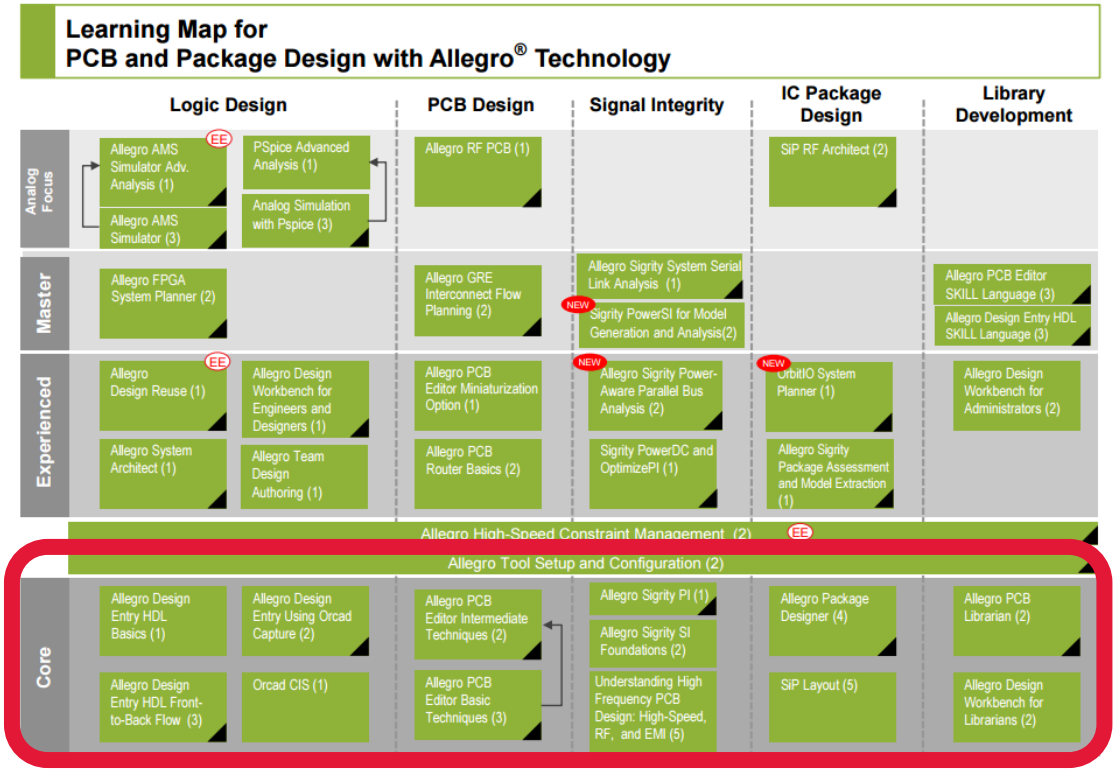
The Allegro® Sigrity™ PI: This course covers the Allegro Sigrity PI product, which provides an integrated solution for power delivery analysis, and features integrated Sigrity technology for DC analysis and a Power Feasibility Editor to drive the creation of Power Integrity Constraint Sets. In this course, you run a DC analysis on a PCB to determine the voltage drop seen by the power consuming components on a PCB. You also use the Power Feasibility Editor to select and analyze a set of capacitors and create a decoupling strategy for ICs on the board. This strategy is then captured in a power integrity constraint set and is passed back to the design and managed in the Constraint Manager. You also use these power integrity constraint sets to provide placement guidance for placing the decoupling capacitors on the board.

IC Package Design

Allegro Package Designer: This course discusses the Allegro Package Designer system. It covers the design and specifications for manufacturing single-chip modules for single-, double-, or multi-layered analog and digital packages.

Library Development

Allegro PCB Librarian: In this course, you are introduced to the Library Explorer, the Part Developer, and PCB Editor. Next, you learn how to create a development and testing area for new Allegro Design Entry HDL (DE-HDL) and PCB Editor parts.



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The required sub topics for Virtuoso Technology

Course Descriptions

IC CAD

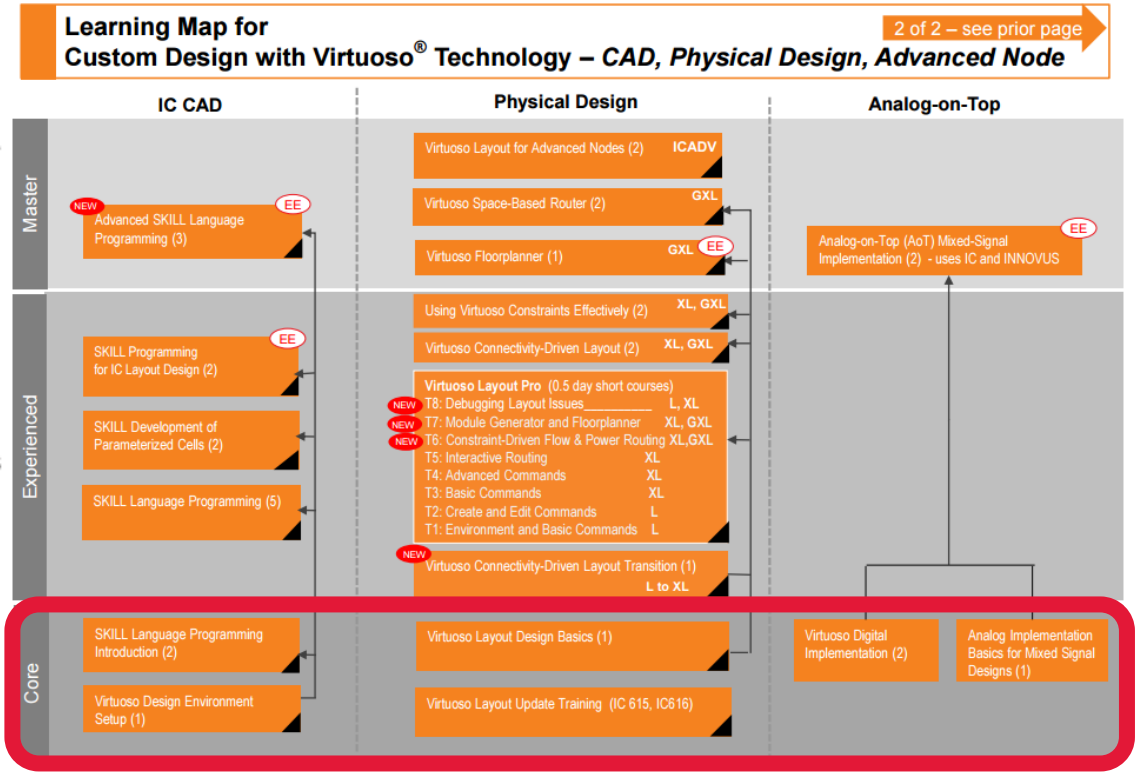
Virtuoso Design Environment Setup: Learn to install the software, manage licenses, and troubleshoot file-locking issues.

SKILL Language Programming Introduction: Get the basic SKILL language foundation to write and debug SKILL procedures in just two days.

Physical Design

Virtuoso Layout Design Basics: Learn the basic techniques for working with Virtuoso Layout Suite L. Create and edit cell-level designs utilizing design assistants, and place instances to build hierarchy for custom physical designs.

Virtuoso Layout Suites Update Training: Get detailed explanations of the new features in the IC 6.1.6 release for VLS L, XL, and GXL. View embedded demos that highlight and describe many of the new and improved features. There are extensive notes for clarity and ease of understanding.



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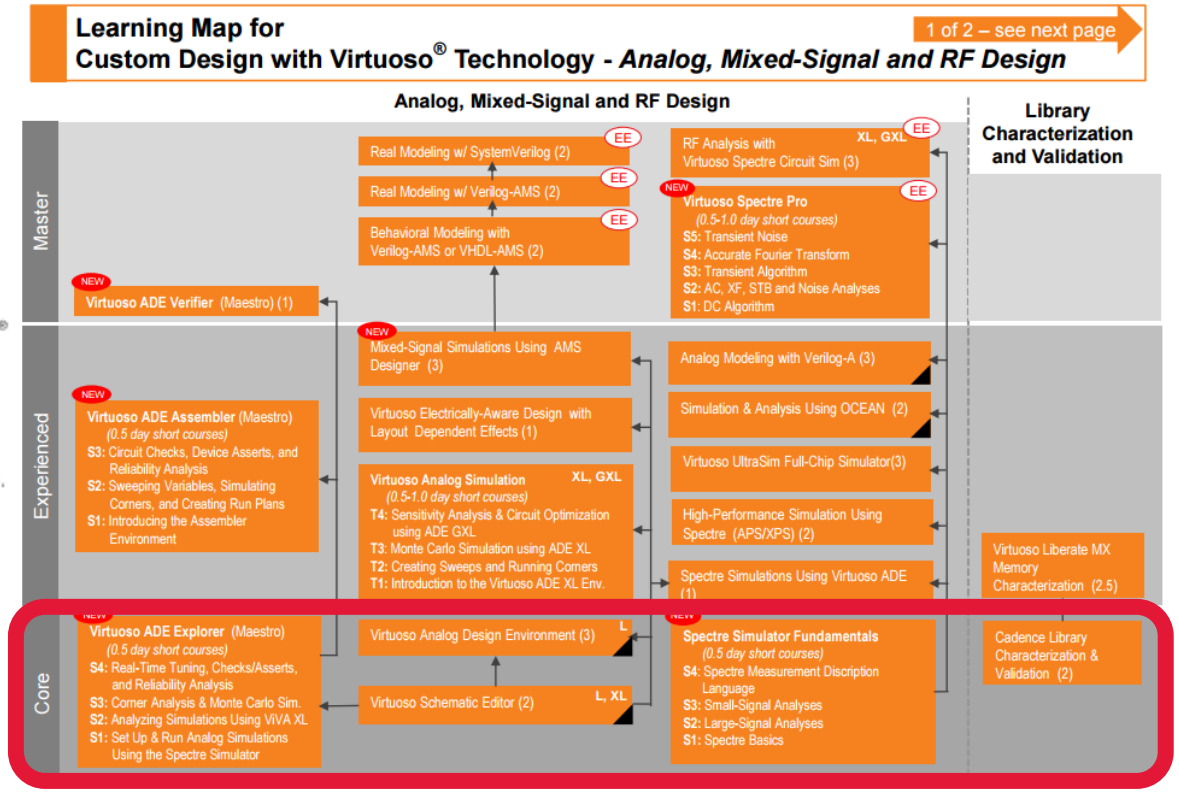
The required sub topics for Virtuoso Technology

Course Descriptions

Analog, Mixed-Signal and RF Design

Virtuoso Schematic Editor: Learn how to create schematics, their corresponding symbols, and navigate a design hierarchy. Create design constraints using the Constraint Manager and the Circuit Prospector, and learn to use inherited connections.

Virtuoso Analog Design Environment: Learn how to simulate analog circuits in the ADE-L environment using Spectre® and APS Simulators. Use the ViVA XL Waveform Viewer and analyze simulation results. Modify the CDF for an instance. Perform device checking and run parametric sweeps. Use the Hierarchy Editor to switch between multiple design views. Use Virtuoso Power System to evaluate IR drop and electromigration.



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The required sub topics for Sign-Off and Verification

Course Descriptions

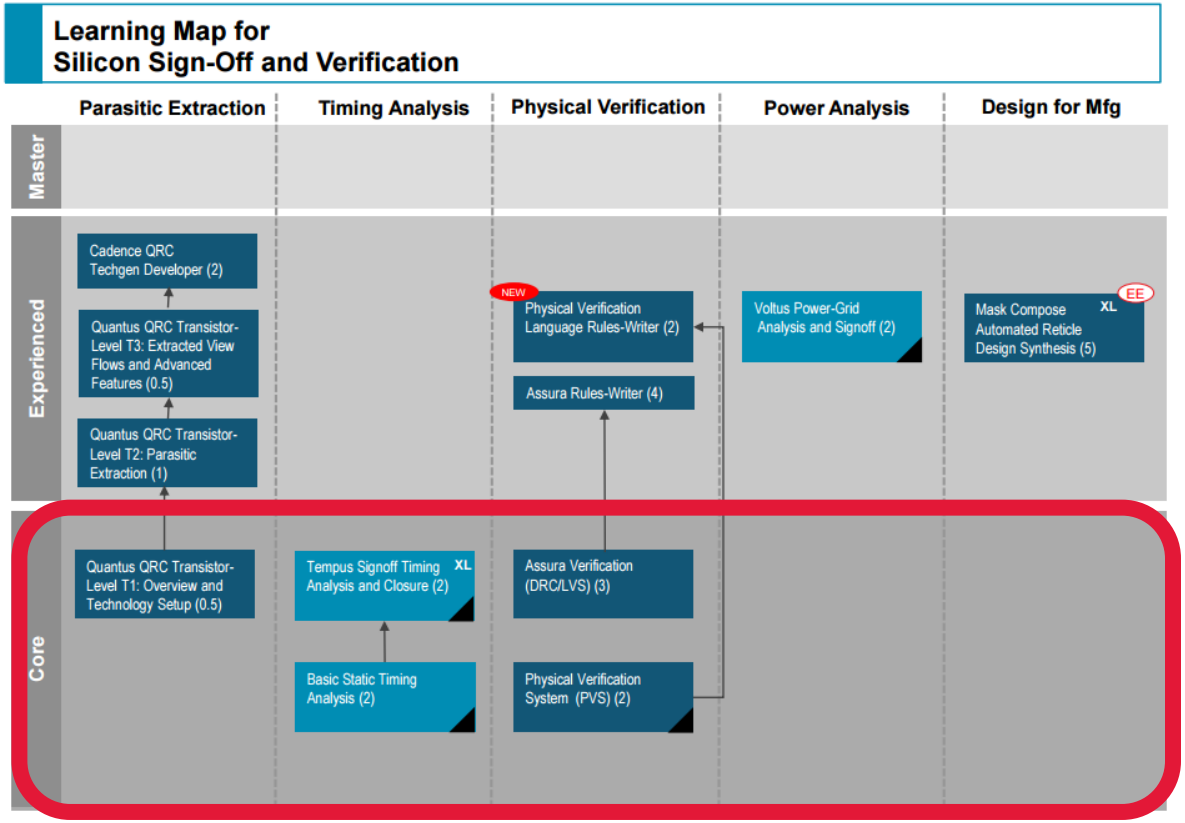
Timing Analysis

Basic Static Timing Analysis: In this course, you learn the basic concepts of static timing analysis and apply them to constrain a design.

Tempus Signoff Timing Analysis and Closure: This cours is a detailed exploration of the timing, IR drop, and signal integrity analysis capabilities of the Tempus™ Timing Signoff Solution software.

Physical Verification

Cadence Physical Verification System: Learn practical methods of running and debugging DRC, ERC, and LVS. Use the powerful PVS debugging environment to locate errors and fix real problems quickly.



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The required sub topics for Encounter Technology

Course Descriptions

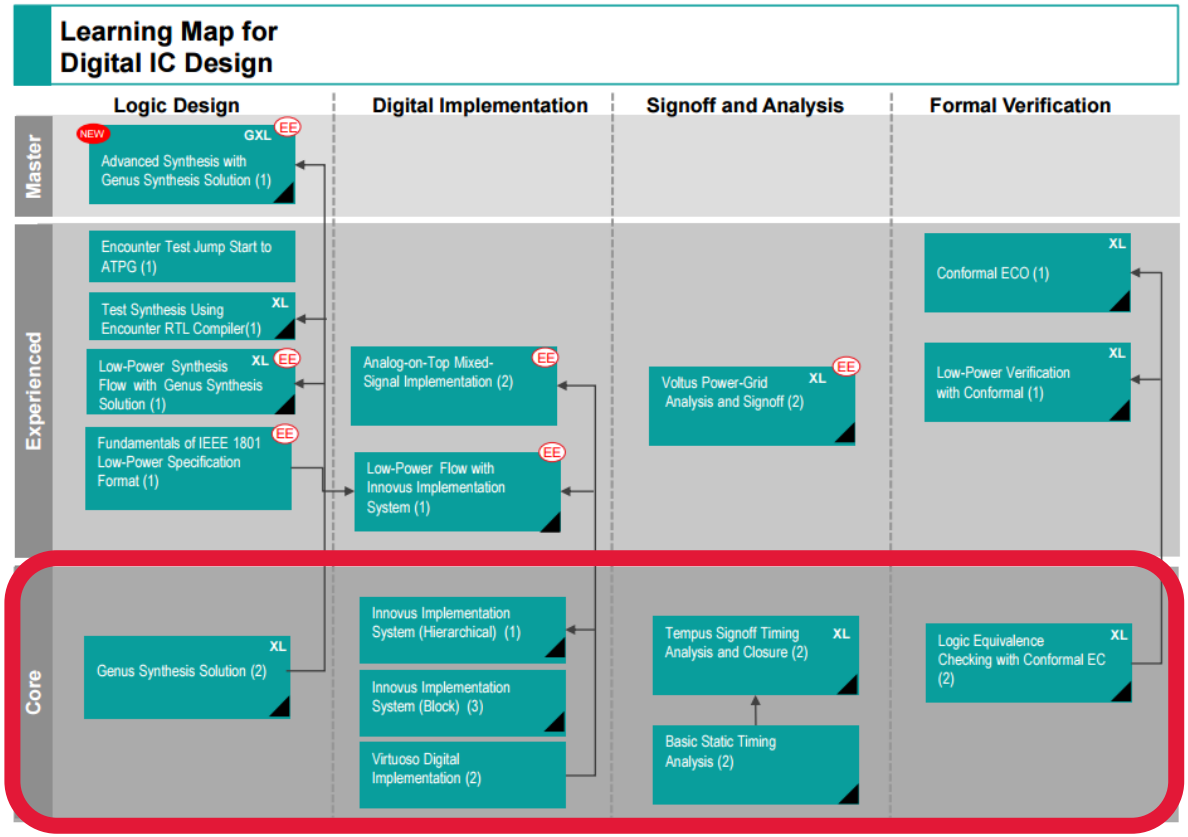
Logic Design

Genus Synthesis Solution: In this course, you learn about the features of the Cadence® Genus™ Synthesis Solution with next generation synthesis capabilities (massively parallel, tight correlation, RTL design focus and Architecture level PPA) and how SoC design productivity gap is filled by Genus. You learn several techniques to constrain designs, run static timing analysis, evaluate datapath logic, run physical synthesis, optimize for low-power structures, analyze DFT (design for testability) constraints, and interface with other tools. You will be able to identify the steps required to perform logic optimization for digital design and generate various input and output files. You also learn to run complete synthesis flow on a design with the given specifications and optimize it for area, timing, and power.

Digital Implementation

Innovus Implementation System (Hierarchical): In this course, you explore the features of the Innovus™ Implementation System for creating and implementing a hierarchical design. You learn several techniques to floorplan your design, create partitions (hierarchical blocks), run place and route, and optimize the design (at the block level and top level) to close timing. You learn techniques to reduce the memory-size and run time by using interface logic models (ILMs).

Innovus Implementation System (Block): In this course, you learn how to use the Innovus® Implementation System software to achieve the best power, performance and area (PPA) for your design. You learn several techniques for floorplanning and placement using the GigaPlace solver-based placement while implementing timing closure strategies with a multi-threaded, layer-aware timing- and power-driven optimization engine to reduce dynamic and leakage power. You will learn how to set up and run the concurrent clock and datapath optimization engine to enhance cross-corner variability and boost performance with reduced power.



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The required sub topics for Encounter Technology

Course Descriptions

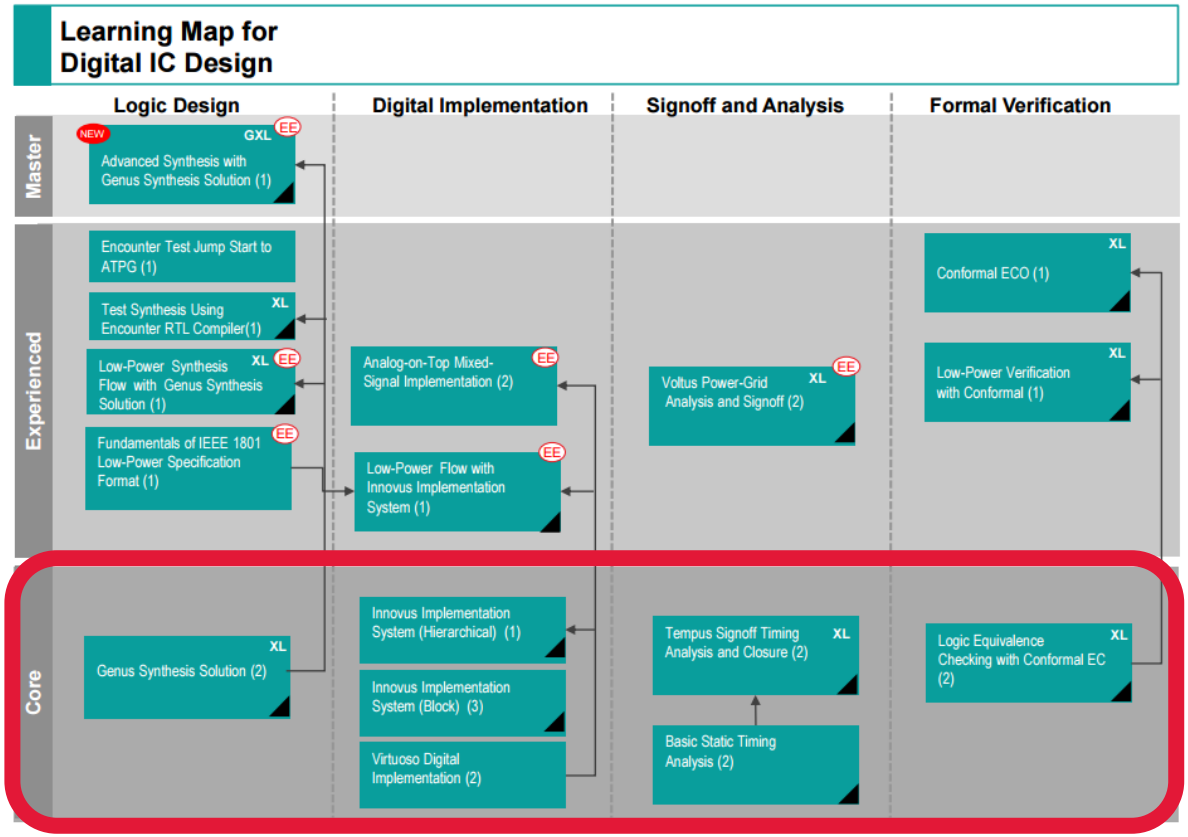
Signoff and Analysis

Basic Static Timing Analysis: In this course, you learn the basic concepts of static timing analysis and apply them to constrain a design.

Tempus Signoff Timing Analysis and Closure: This course is a detailed exploration of the timing, IR drop, and signal integrity analysis capabilities of the Tempus™ Timing Signoff Solution software.

Design Verification

Logic Equivalence Checking with Encounter Conformal EC: In this course, you use the Encounter Conformal® Equivalence Checker to perform functional verification. You learn the basic flow of equivalence checking and how to run hierarchical comparison of designs.



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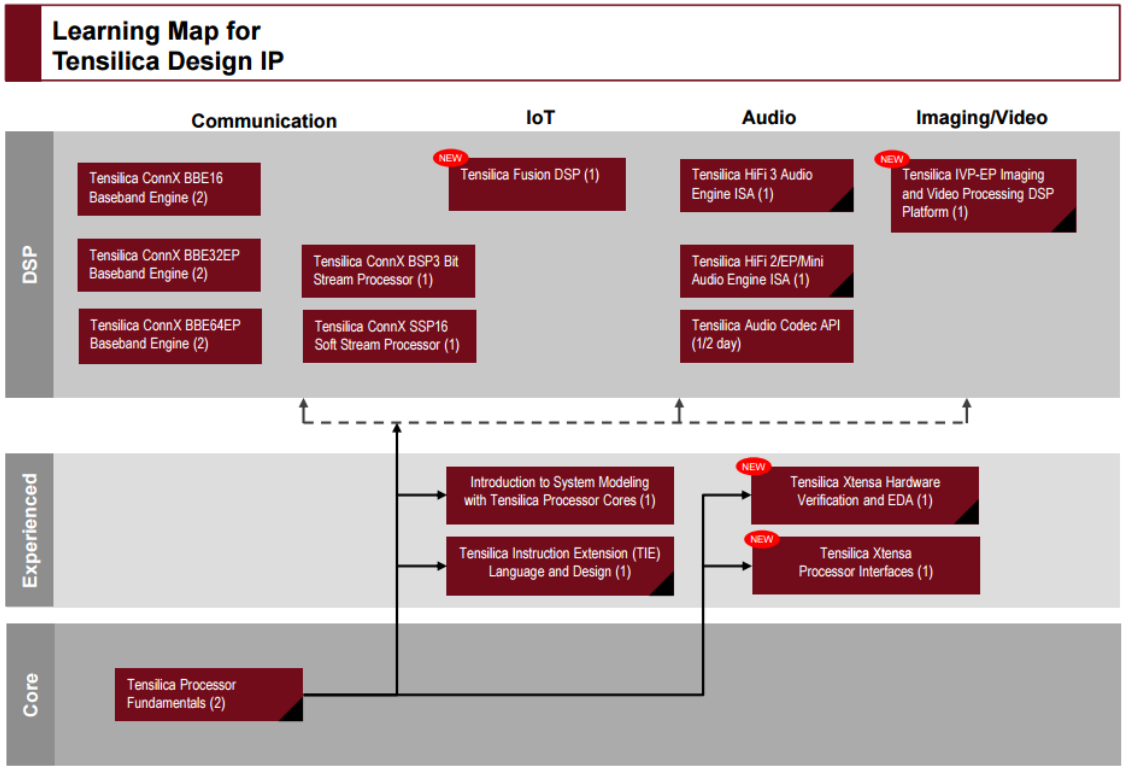
The required sub topics for Tensilica-IP

In order to be certified in **Tensilica IP** technology you need to attend and pass **all the required trainings** that are available through iLS.

- Tensilica Xtensa Hardware Verification and EDA v6.1 (iLS)
- Tensilica Processor Fundamentals v6.1 (iLS)
- Tensilica Instruction Extension Language and Design v6.1 (iLS)
- Tensilica HiFi 2/EP/Mini Audio Engine ISA v5.0 (iLS)
- Tensilica HiFi 3 Audio Engine ISA v5.0 (iLS)
- Tensilica IVP-EP Imaging and Video Processing DSP Platform v6.1 (iLS)



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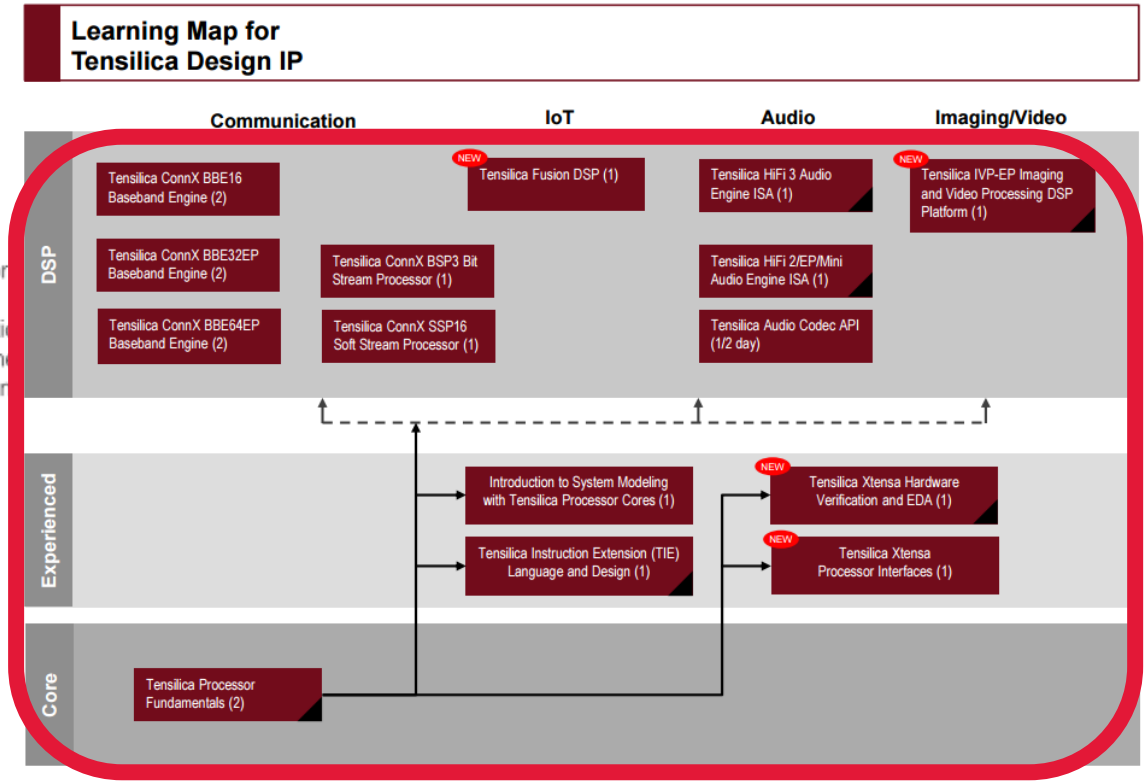
The required sub topics for Tensilica-IP

Course Descriptions

Tensilica Processor Fundamentals

This two-day course provides basic information about Tensilica processor technology and how to use Tensilica's product deliverables for your SoC design. Topics in processor architecture are discussed, and the configurable options of the Xtensa® LX series processors are outlined. You will practi working with the Xplorer Integrated Development Environm (IDE), working with Tensilica software tools, and programmi Xtensa processors in the four lab exercises that are part of this course.



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The required sub topics for Tensilica-IP

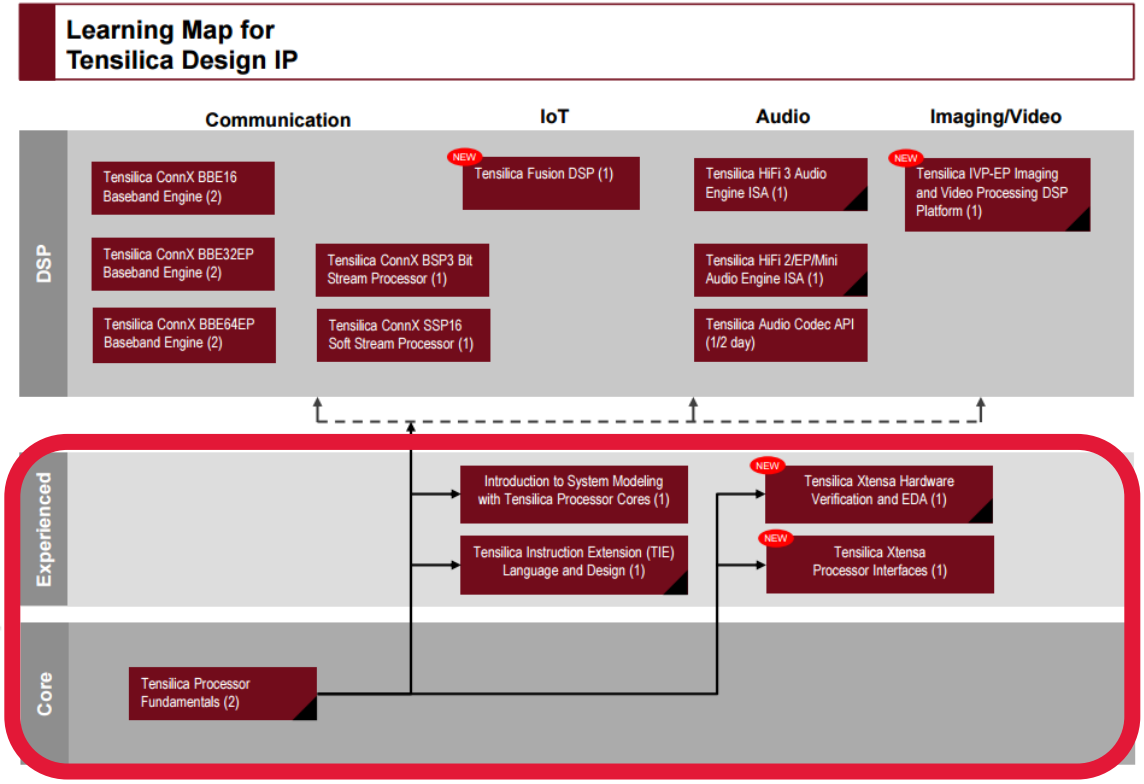
Course Descriptions

Tensilica DSP Courses

Training is available for several Tensilica DSP processor cores that are optimized for audio, baseband and imaging/video applications respectively. The HiFi family of DSPs are optimized for audio signal processing, the ConnX family of DSPs are optimized for baseband signal processing and the IVP DSP is optimized for imaging/video signal processing as illustrated in the learning map above.

The training class for each DSP provides an overview of the architecture and the instruction set of the DSP. The class covers the programming model in detail, teaching you how to write and optimize C code for the DSP. Most of these DSP's include specialized instructions relevant to the application domain, and these are illustrated in the training class. Demonstrations and labs used in the class will give you practical and hands-on experience in programming the DSP. The training class for the vector DSPs also teach techniques for programming VLIW/SIMD machines, and teach you how to write C code that can be vectorized by the C/C++ compiler.

Each training class provides the software developer or firmware engineer the essential skills necessary to develop and optimize code for a particular DSP. For more details on each class, please refer to the course description on the online course catalog at www.cadence.com/training.



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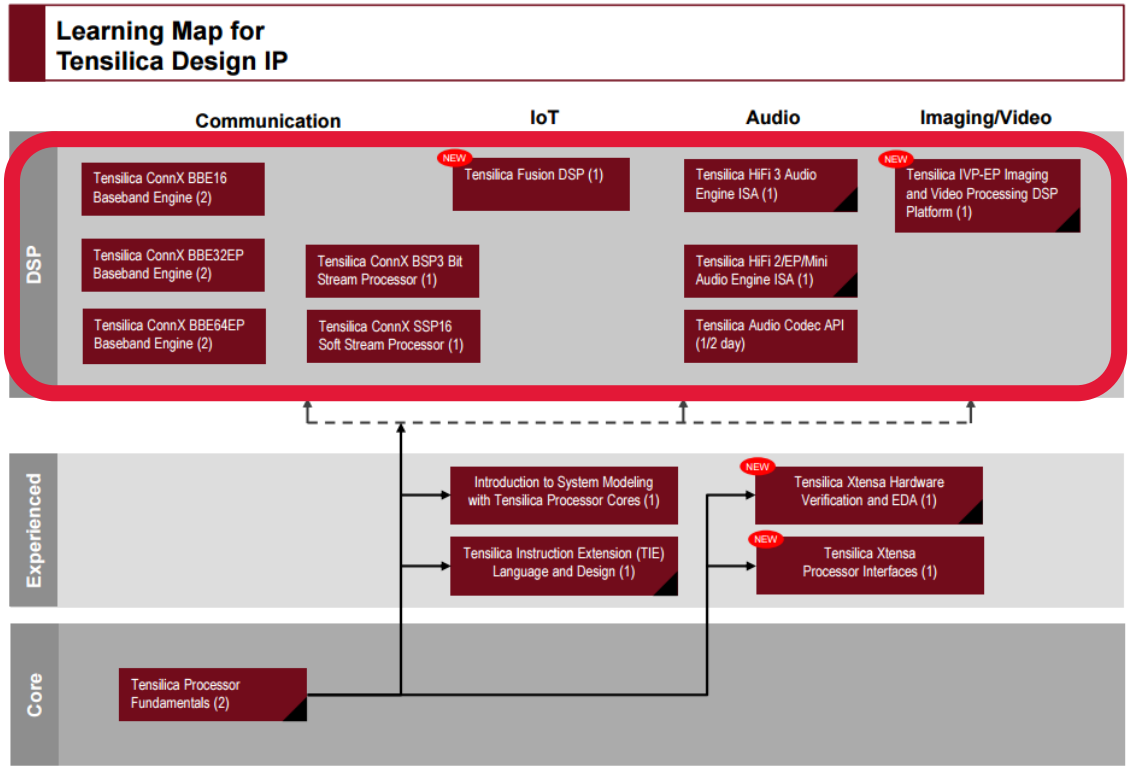
The required sub topics for Tensilica-IP

Course Descriptions

Specialized Courses

Tensilica Instruction Extension Language: This course covers how to create processor extensions that improve processing performance as well as data bandwidth for your application code. The class also teaches basic optimization and estimation techniques. Five labs covering different topics will provide hands-on experience in writing TIE code.

Tensilica Xtensa Hardware Verification and EDA: This on-line course provides information about Tensilica® processor technology and how to use Tensilica product deliverables for your SoC design. You explore topics regarding installation of the Xtensa processor and hardware package. You will understand the verification environment provided with the Xtensa processor. This will allow you to modify the testbench and extend the testing of your complete SoC. You will also understand the implementation flow of the Xtensa processor. This includes configuring and running the EDA scripts provided for Synthesis, Place and Route, Power Analysis and Formal Verification. The solid fundamentals taught in this course enable you to quickly become productive in the use of Xtensa processors for your SoC design.



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Get access to the Internet Learning Series

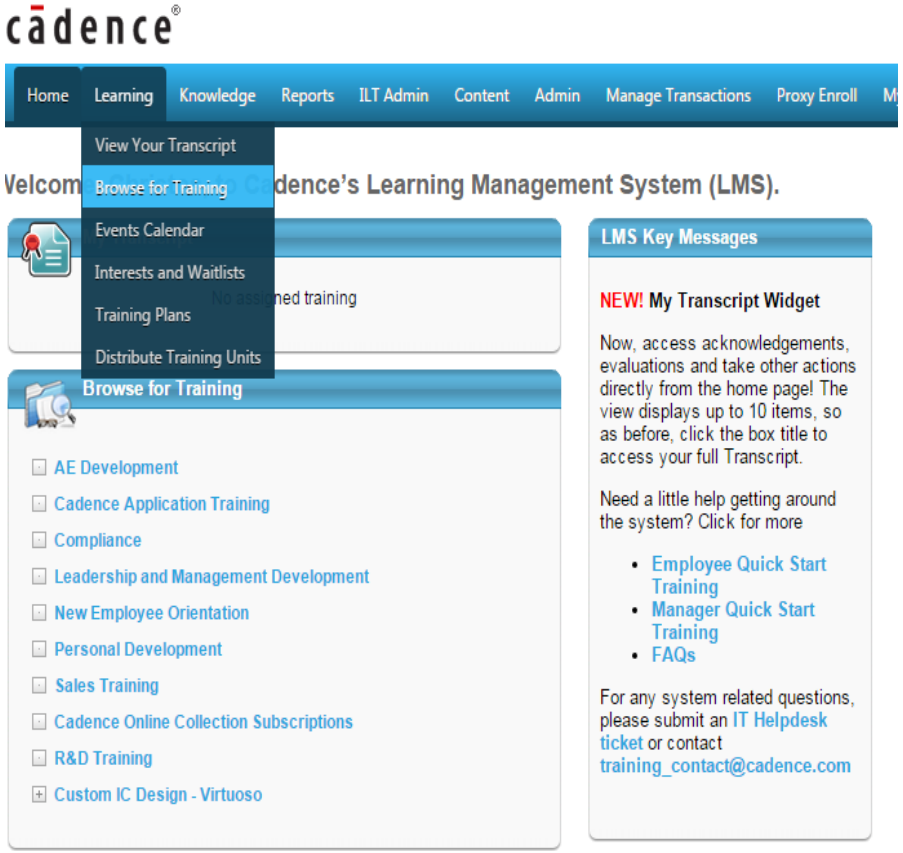
- For universities based in **Americas**:
  Contact Cheryl Mendenhall (cherylm@cadence.com)
- For universities based in **EMEA**:
  Contact Anton Klotz (aklotz@cadence.com)
- For universities based in **China**:
  Contact Eva Sun (sfang@cadence.com)
- For universities based in **Indian region:**
  Contact Piyush Sharma (piyushs@cadence.com)

Get access to the Internet Learning Series

After you got notification about your booked iLS courses:

- Log in to your Learning Management System (**LMS lms.cadence.com**)
- Go to Learning

  > View Your Transcript



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Get access To The Internet Learning Series - Europractice

For the members of **EUROPRACTICE** program:

- Visit Europractice's main page:

http://www.europractice.stfc.ac.uk/welcome.html

- Go to **Packages -> Cadence -> Cadence iLS course catalog -> Go to EUROPRACTICE/Cadence iLS booking portal.**

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Get access To The Internet Learning Series - Europractice

- Select the technology you want to enable
- Select the courses you want to book
- Wait for confirmation email
- Log in to your Learning Management System (**LMS lms.cadence.com**)
- Go to Learning

  > view your transcript

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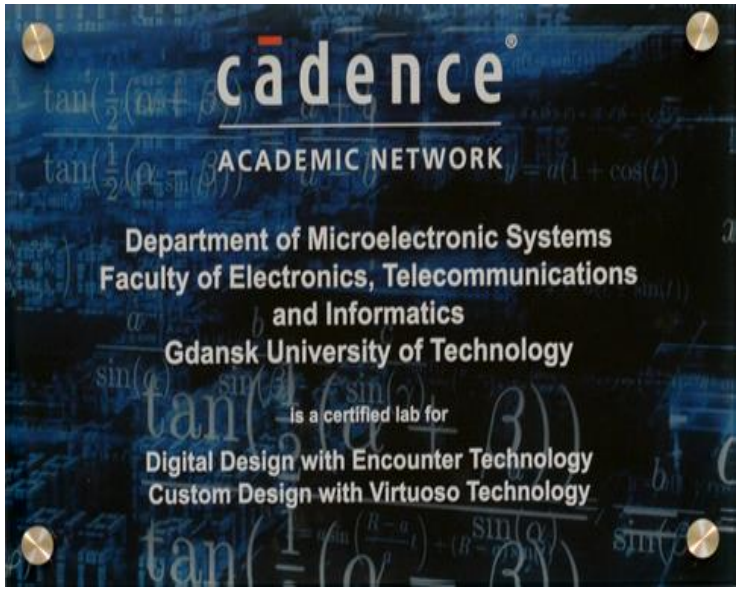
STEP 4: Get Certified

After completing the iLS courses, the university laboratory gets certified with a Cadence Certification Plaque, while the lab instructors receive individual certificates. Every lab instructor has to be certified in order for the lab to be certified



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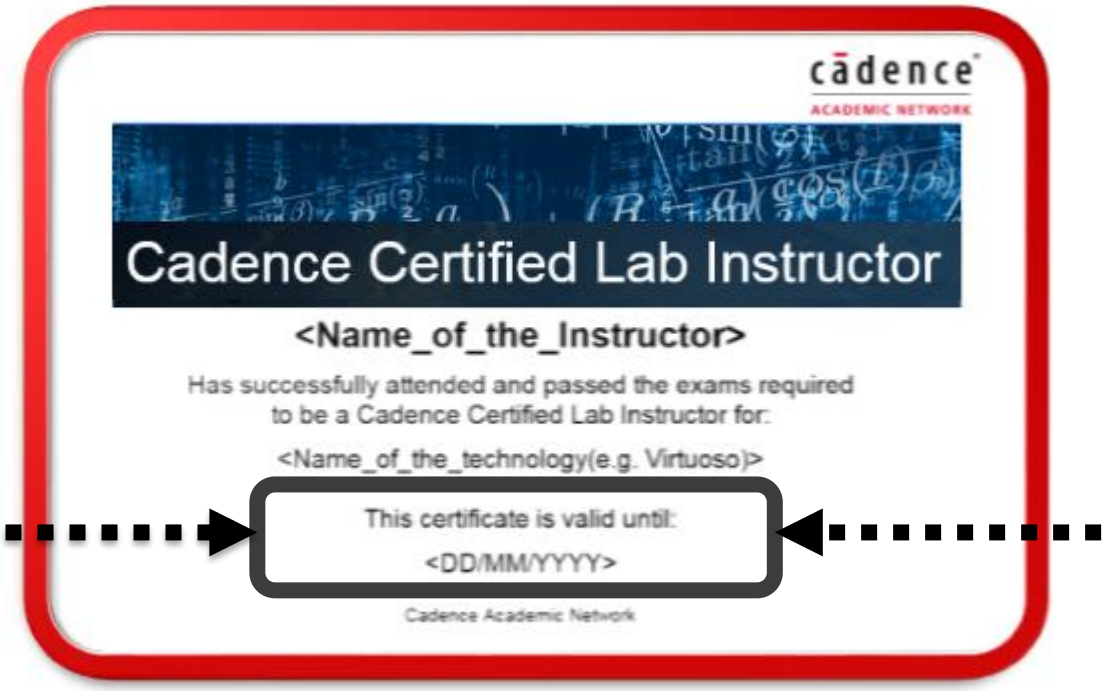
STEP 5: Stay Updated

- The certification will be valid for one year.
- To renew the certification you will need to fulfill all new core iLS courses that have become available in the year of your certification.



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Summary Of The Rules

I. For the University to receive certification, at least one of the available Cadence Technologies must be completed.
II. The most recent version of the available Cadence software must be used.
III. The group of examiners should attend and pass all the core iLS courses for the specific Cadence Technology relevant to each examiner.
IV. Every lab instructor has to be certified in order for the lab to be certified.
V. The Certification has to be renewed after one year. To renew the certification you will need to fulfill all new core iLS courses that have become available in the year of your certification.

Universities that have participated in the Certification Program

- Gdansk University of Technology, Poland

Professors certified:

- Prof. Jacek Jakusz
- Prof. Waldemar Jendernalik
- Prof. Bogdan Pankiewicz
- Prof. Marek Wójcikowski

Certification on:

Custom Design with Virtuoso Technology

Digital Design with Encounter Technology

Certified Universities

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Universities that have participated in the Certification Program

- Ruhr University of Bochum, Germany

Professors certified:

- Prof. Michael Huebner
- Prof. Diana Goehringer
- Mr. Jens Rettkowski

Certification on:

Tensilica IP

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Certified Universities

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Frequently Asked Questions

1. ***How can my lab sign up for the Certification Program?***
   - Contact academicnetwork@cadence.com and you will be provided with all the information and support you need to achieve Certification
2. ***Are the lab materials in the certified lab reviewed by Cadence?***
   - No, but Cadence is highly interested that the certified instructors teach courses which use the latest Cadence tools and flows.
3. ***Are the iLS courses free?***
   - This can vary depending on the Cadence contract, so please contact your regional manager as defined in the contact slide.
4. ***Can I use iLS courses for student education?***
   - Please contact your regional manager as defined in the contact slide.
   - iLS courses can be a useful addition to courses lead by Certified Professors.
5. ***How do I renew my certification?***
   - Contact academicnetwork@cadence.com for information about which new iLS courses have to be completed in order to renew the certification.

Frequently Asked Questions

7. ***Can students get a certificate?***

- iLS courses can be part of the lecture. After accomplishment of the iLS courses, the student gets a certificate.

8. ***Can the iLS courses for a technology be divided between the examiners?***

- No, each examiner should take all the iLS courses needed for certification in the technology. When renewing your certification, all examiners will need to take all the new elements of the iLS training required.

9. ***How will students and other academics know that our lab is certified?***

- When you are successfully certified, your achievement will be announced via our communication channels, you will be added to a dedicated web page listing certified labs and you will be sent a plaque to display in your lab.

Universities committed to Certification

❑Europe

- AGH University of Science and Technology
- Aristotle University of Thessaloniki
- Technical University of Lodz
- University of Pittsburgh at Bradford
- Universidade Do Porto

Universities committed to Certification

❑United Arab Emirates

- Khalifa University of Science Technology and Research
- Abu Dhabi University

❑United States Of America

- Purdue University

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