Design Reuse (Capture Allegro PCB Editor Flow)

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Purpose

Capture boosts schematic editing efficiency by enabling sub-circuit reuse. Using hierarchical blocks, designers can simply reference the same sub-circuit multiple times. Also, the automatic creation of hierarchical ports eliminates potential design connection errors. Ports and pins can be updated dynamically for hierarchical blocks and underlying schematics.

Audience

This document is intended for Capture Allegro users who want to reuse their designs and create reuse modules in Allegro PCB Editor

Design Reuse (Capture Allegro PCB Editor flow)

A reuse module in Capture is either a library (OLB) part or schematic design (DSN) that is externally referenced. An externally referenced design is a complete physical PCB design laid out on a board. Also, the corresponding schematic design is converted to a reuse module in Capture by choosing the Generate Reuse Module option in the Allegro Reuse tab of the Annotate dialog box.

In PCB Editor, the source of a design reuse module is the Capture netlist. This netlist contains a set of REUSE properties that identify each of the packages within these modules. After placing and routing a board, you can save it as a reuse module by creating an MDD file. You can now create modules for reuse in your design.

The creation of design reuse modules and their use in Capture follows the general procedure outlined in these steps:

1. Build the Capture schematic of a reuse design.
2. Perform a design rules check (DRC)., Then annotate the design. If you do not plan to make any design changes in Allegro that would affect the netlist, skip to step 6. Otherwise, proceed to the next step.
3. Netlist the design to PCB Editor, then import the netlist into PCB Editor or open a BRD design during netlisting.
4. Place and route the design in PCB Editor.
5. Export logic to Capture, then back annotate the changes to Capture.
6. In Capture, generate a reuse module from the design using the PCB Editor Reuse tab of the Annotate dialog box.
7. Netlist the design to PCB Editor, and create an MDD reuse module from the schematic reuse design.
8. Repeat steps 1 through 7, as necessary, for multiple levels of design in a design reuse hierarchy.
9. Use the reuse module in a Capture design, either as a library part or a hierarchical block.

IMPORTANT: Except for occurrence properties, the schematics of externally-referenced libraries and designs should not be edited. You should view them as read-only designs. Editing these designs from within your schematic can introduce errors such as duplicate reference designators.

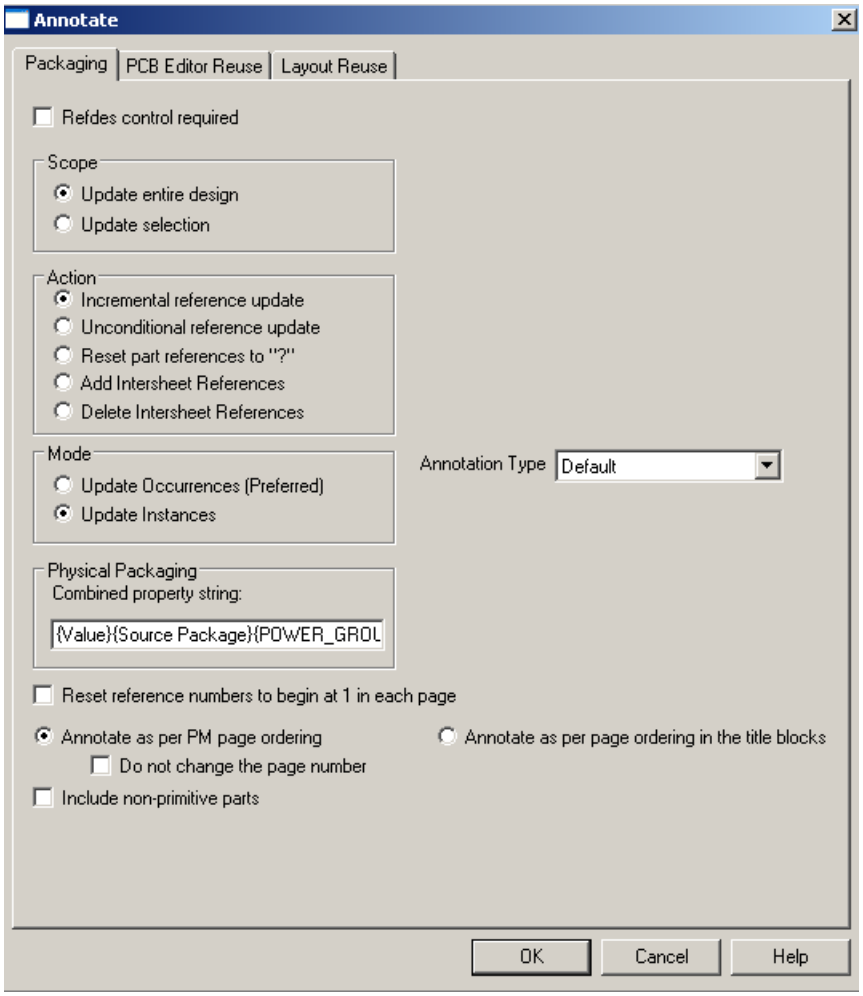
Building the Capture schematic of a reuse design

1. In Capture, create a schematic design that will become your reuse design.

   You can use the project wizard to set up your schematic and build the design from scratch or use library components.

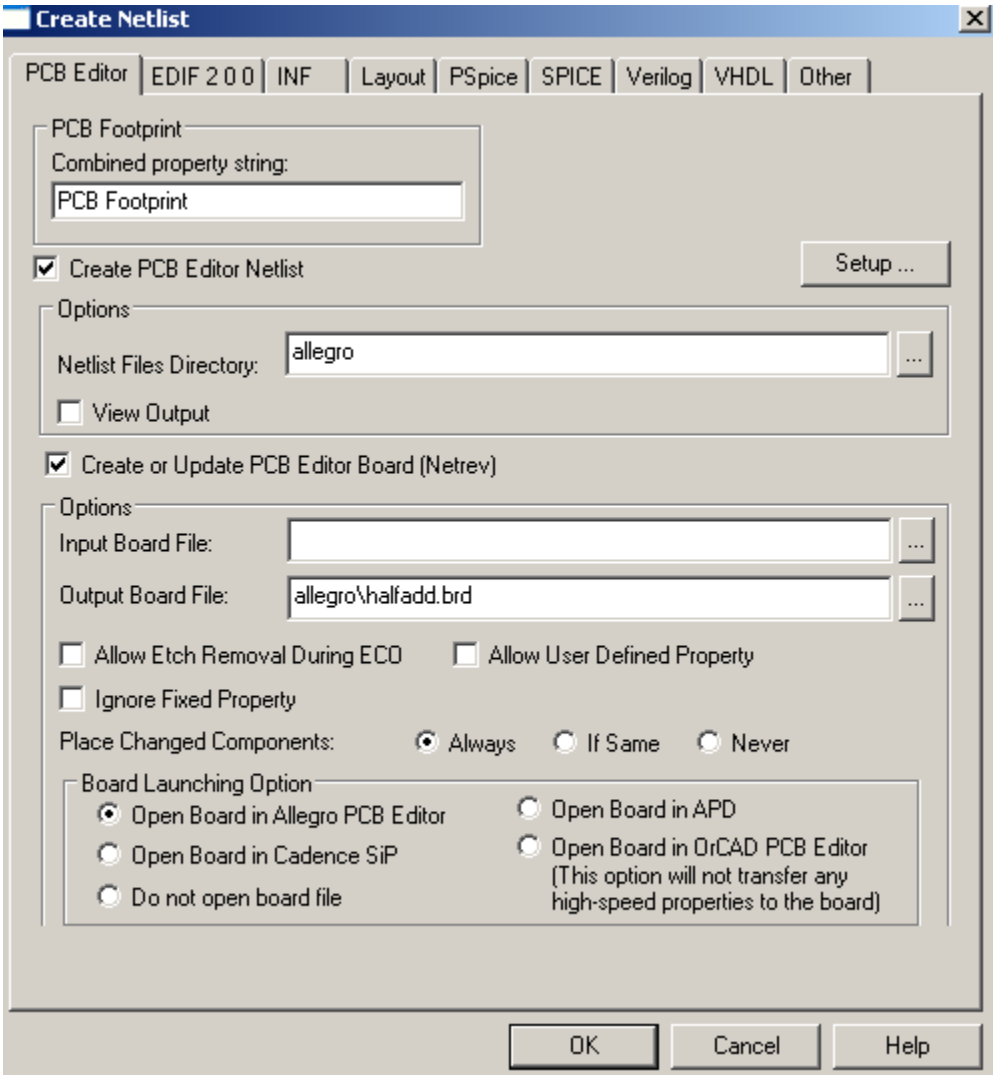
2. Check for design errors by selecting the DSN file in the project manager then choose **Tools > Design Rules Check**. This checks for disconnected nets, errors such as no connects, off-grid objects, packaging and duplicate part references.

3. Annotate the design by choosing **Tools > Annotate**, and selecting the Packaging tab.

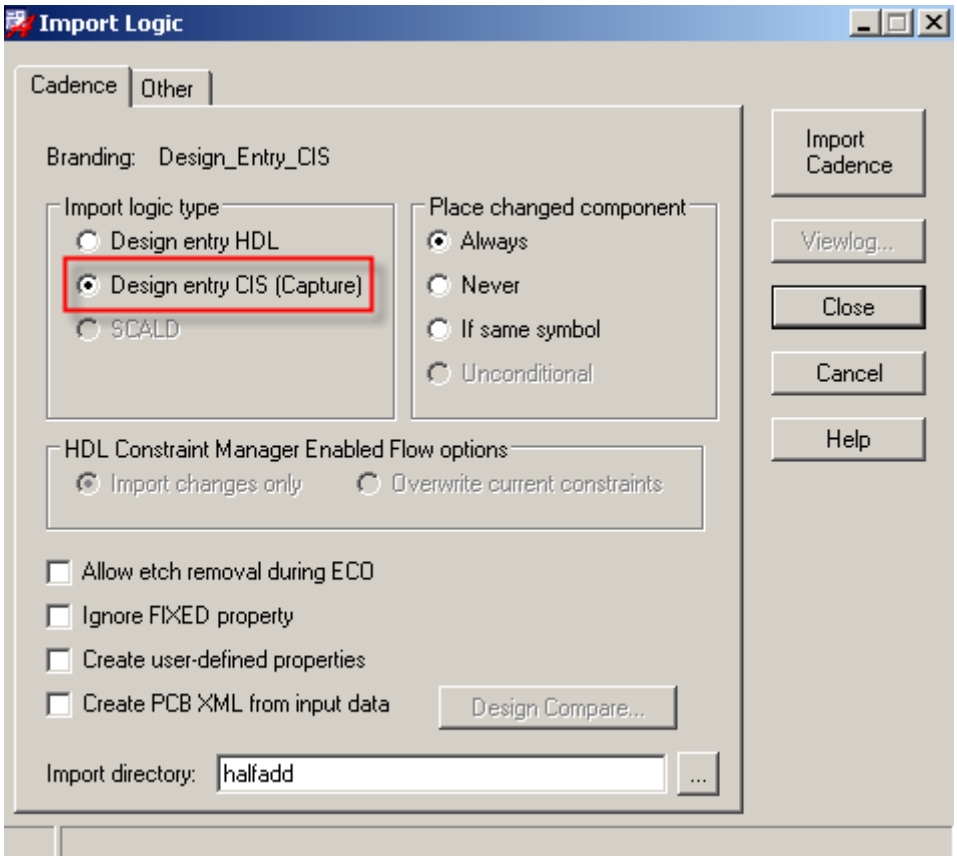


The Packaging options shown in the figure are generally appropriate at this stage of reuse module creation. You use the PCB Editor Reuse tab to generate a reuse module or to annotate a hierarchical design that uses reuse modules.

4. Generate a PCB Editor netlist by choosing **Tools > Create Netlist**. Then select the PCB Editor tab in the Create Netlist dialog box. Complete the appropriate options in the dialog box.



5. If you do not generate a board during netlisting by enabling the Create or Update PCB Editor Board (Netrev) option in the Create Netlist dialog box, you need to import the schematic logic into PCB Editor using the **File > Import > Logic** command.

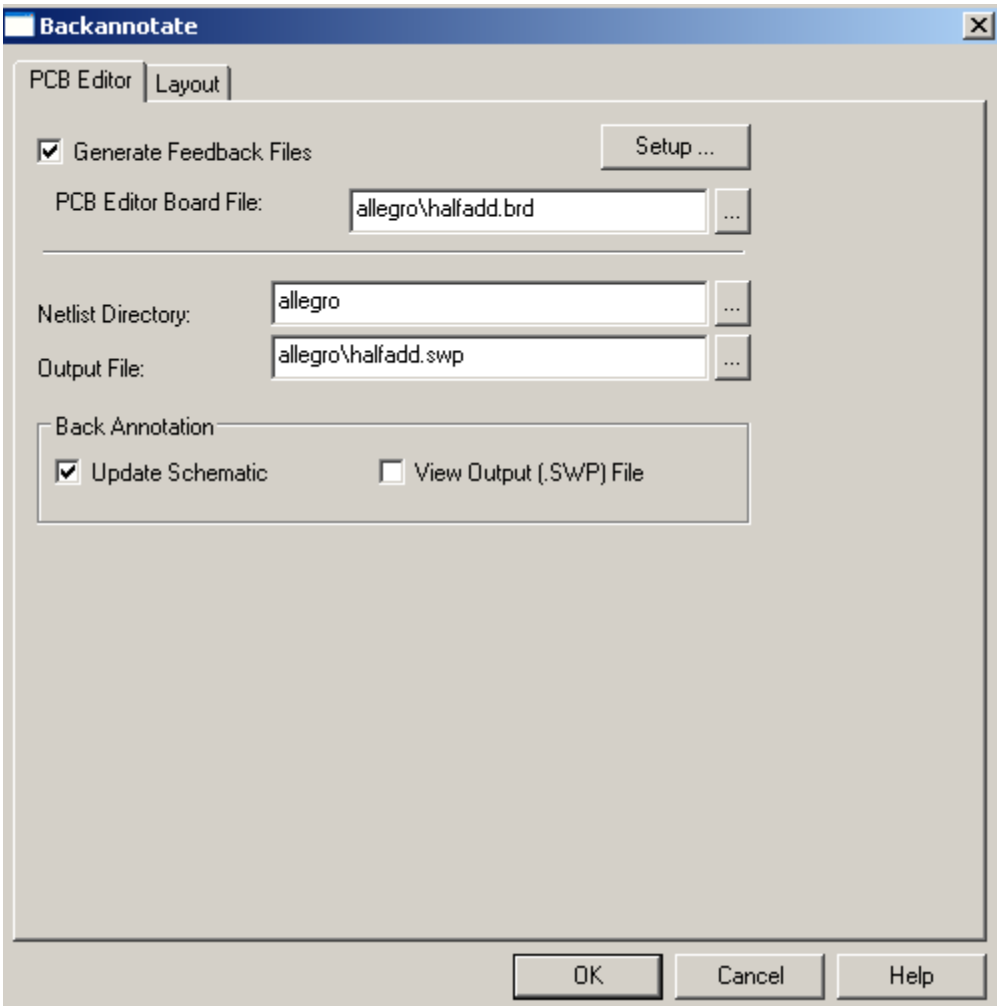


6. In PCB Editor, place and route the physical design.

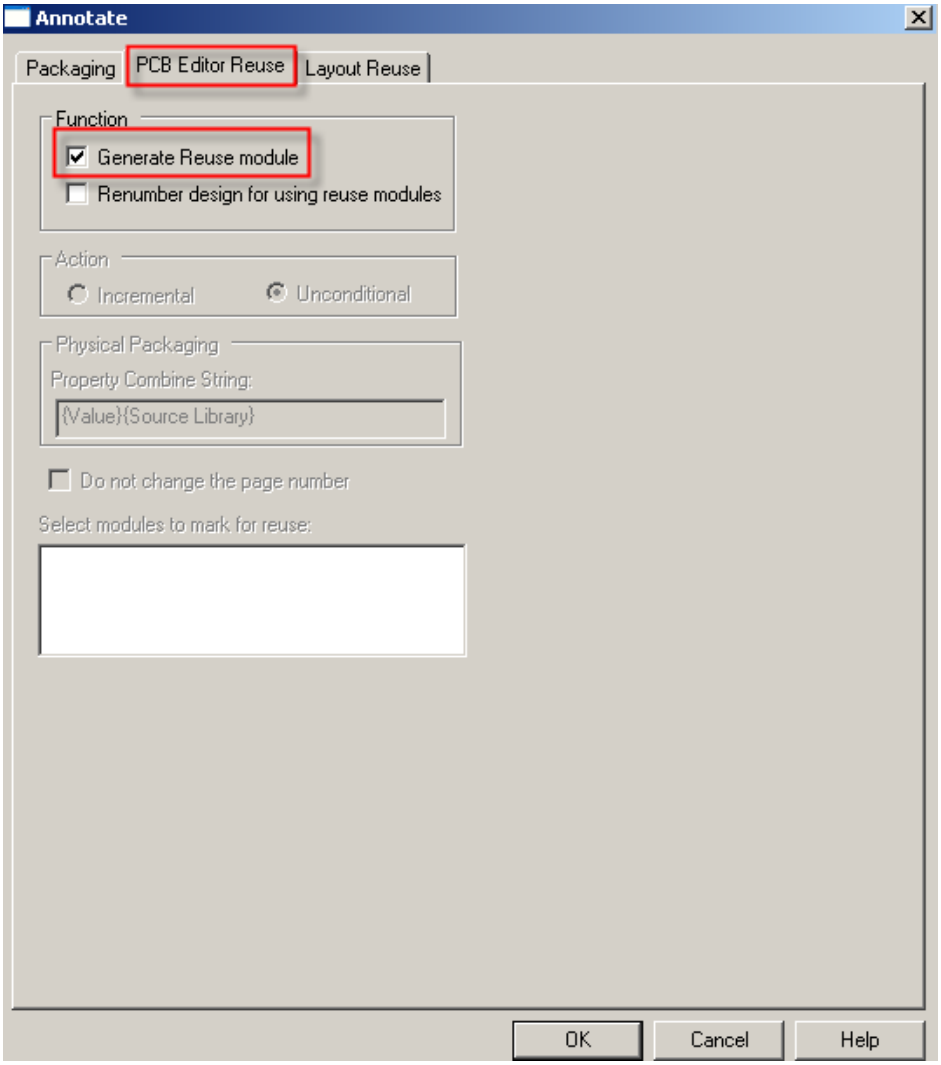
If your PCB Editor footprint symbols are located somewhere other than in the Cadence default directory, set the psmpath and padpath variable to point to the proper location.

7. If changes affecting the netlist have been made in PCB Editor, back annotate the design using the **File > Export > Logic** command in PCB Editor.

8. Synchronize the physical design with the logical design by back annotating in Capture. To do this, choose the **Tools > Back Annotate** command in Capture and select the appropriate options in the Backannotate dialog box.



9. Convert the design into a reuse module by choosing **Tools > Annotate**, selecting the PCB Editor Reuse tab, and enabling the Generate Reuse Module option.



This adds a unique REUSE_ID property for each unique package. This property can be viewed in the Property Editor spreadsheet.

Creating a physical reuse module in PCB Editor

1. In Capture, netlist the design (containing REUSE_ID properties) and import logic into PCB Editor.

   The netlist must contain the reuse properties for PCB Editor to treat the design as a reuse module. This implies that the netlisted design must have first gone through the Generate Reuse Module function in the PCB Editor Reuse tab of the Annotate dialog box (step 9 of the previous section).

2. If you do not generate a board during netlisting by enabling the Create or Update PCB Editor Board (Netrev) option in the Create Netlist dialog box, then you can import the schematic logic into PCB Editor using the **File > Import > Logic** command.

3. In PCB Editor, place and route the reuse design.

4. Create the reuse module in Allegro PCB Editor by selecting **Tools > Create Module**.

5. You are prompted to enter the selection point. To select multiple elements, click the right mouse button and select Temp Group from the pop-up menu.

6. Select the physical entities or draw a window around the module definition. If you are using Temp Group, then click the right mouse button and select Complete from the pop-up menu after you have made all your selections.

7. Click on a point to select the origin of the module definition. This origin will be used when the module is being placed.

8. Enter a file name and select a location at which the file will be saved. Now, you have defined an Allegro Module Definition File (MDD).

NOTE: The module file name must be a concatenation of the Capture design name and schematic name, like this: <DesignName>_<SchematicName>. It must also be saved in the same directory as the Allegro PCB design (*.BRD) that will use this reuse module

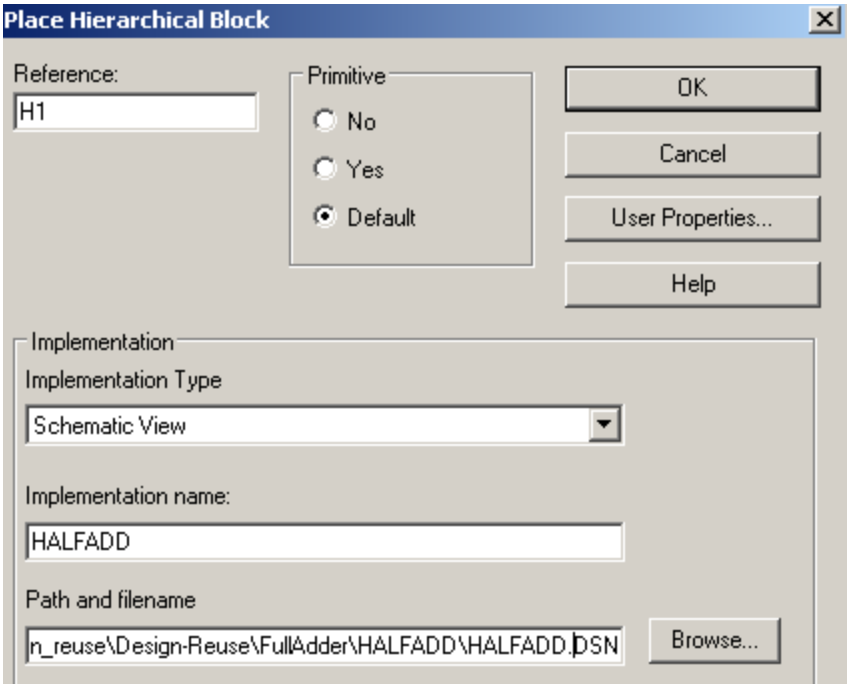
Using a design reuse module in Capture

After you have generated the reuse module in Capture, you can use the module in one of two ways:

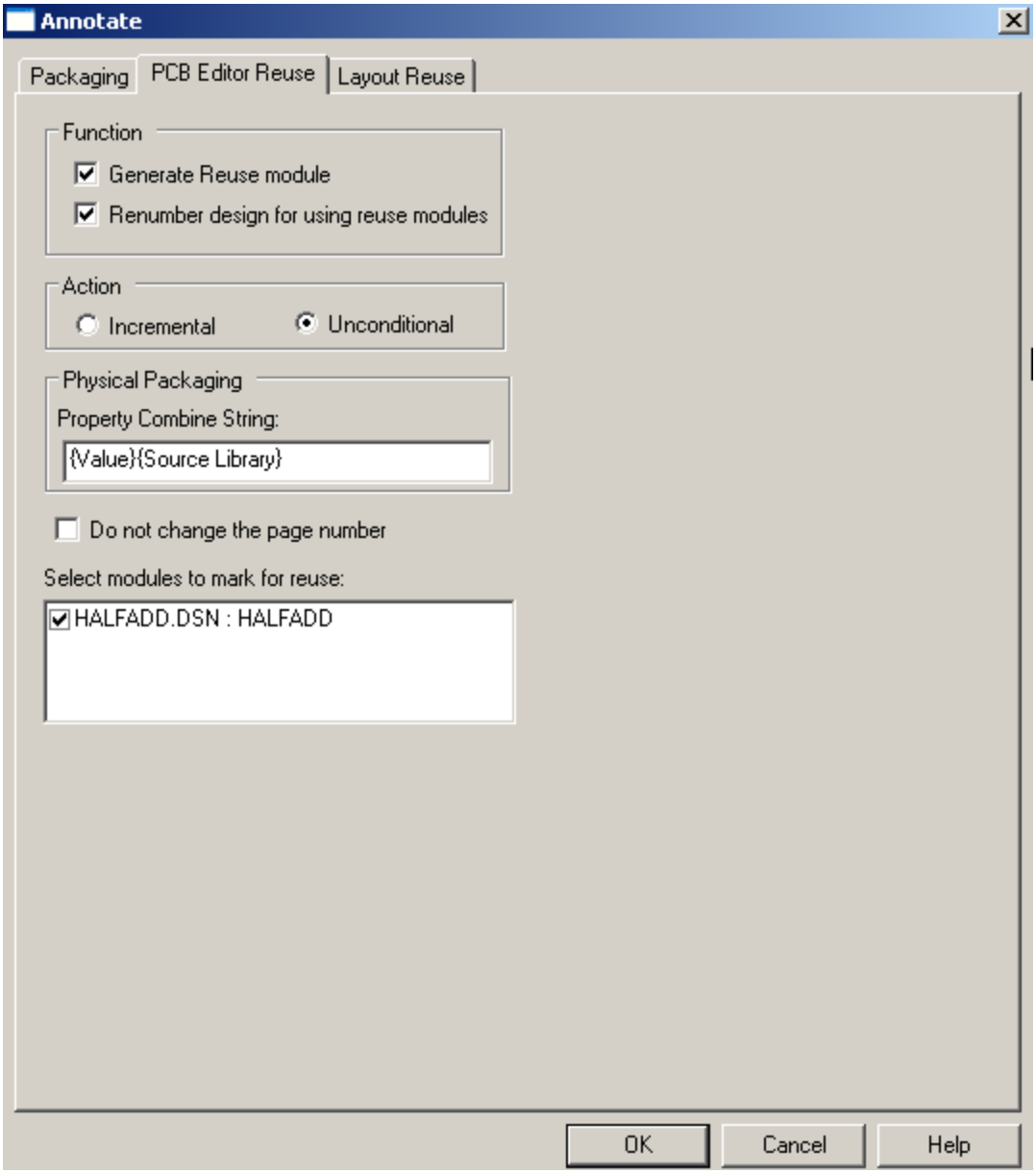
- Placing the module as an external design schematic (DSN file) using the **Place > Hierarchical Block** command;
- Coverting the module into a library part (.OLB file) by using the **Generate Part** feature in Capture.

Placing a reuse module as a hierarchical block

1. In Capture, create a new project and place a hierarchical block referencing the new external reuse design by selecting **Place > Hierarchical Block**.



Annotate the design by choosing **Tools > Annotate**, selecting the PCB Editor Reuse tab, and enabling the Renumber Design For Reuse Modules option.

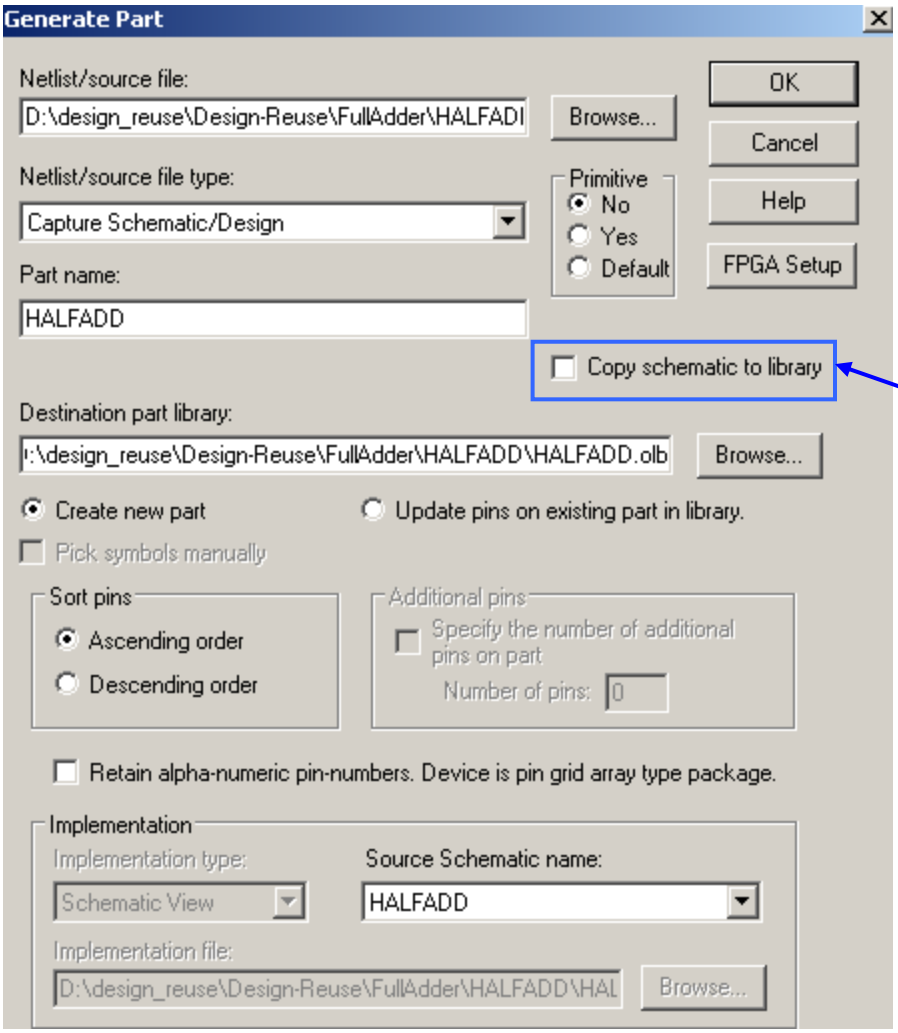


Generate an PCB Editor netlist by choosing **Tools > Create Netlist**. Then select the PCB Editor tab in the Create Netlist dialog box. This process generates the REUSE_INSTANC**E, REUSE_NAME, and REU**SE_PID properties in the netlist for all reuse instances in the design.

After creating the reuse module, if you want to synchronize your Capture schematic with its corresponding Allegro PCB Editor mdd equivalent, you must regenerate an Allegro PCB Editor netlist. You can either update the PCB Editor board or re-import the netlist onto the PCB Editor board. This ensures the REUSE properties are incorporated into the physical reuse module. The module can now be used in any design as a reuse module.

Converting a reuse module into a library part

1. In Capture, select the DSN file in the project manager and choose the **Tools > Generate Part** menu option.



CAUTION: *Do not check* this Copy Schematic to Library option. If you do, you will lose occurrence properties that are critical in design reuse modules.
Also, checking this option will overwrite the custom library, so make sure to specify an unused name unless you want an overwrite.

2. Complete the selection of options in the Generate Part dialog box.
   - For Netlist/Source File, locate the DSN file you converted to a design reuse module.
   - For Primitive, check No.
   - For Part Name, specify the root schematic of the Netlist/Source file.
   - For Designation Part Library, you may use the same design directory where your DSN file is saved or navigate to a library directory where you want to store the new part.
3. Click OK.

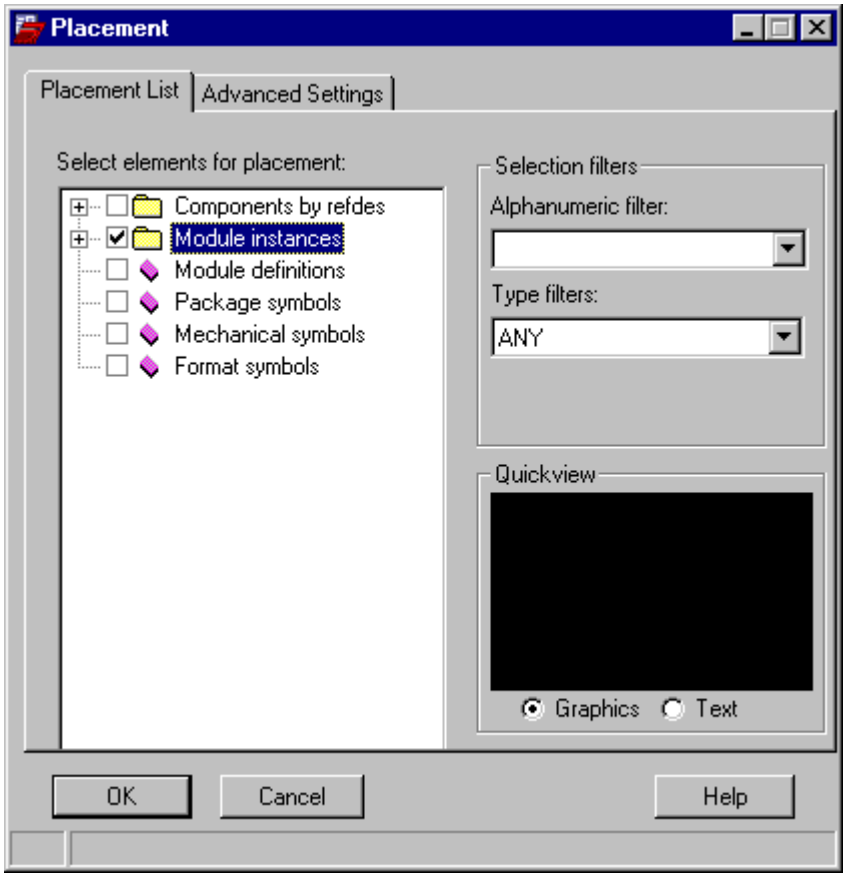
Placing physical reuse module in PCB Editor

1. In Capture, netlist the design (containing REUSE_ID properties) and import logic into Allegro PCB Editor.

   Ensure the Allegro Module Definition File (MDD) is in the same directory as the Allegro PCB design (*.BRD) that will use this reuse module.

2. In PCB Editor, select **Place > Manually.**

3. Select module instances under the Placement List tab in the Placement dialog box.

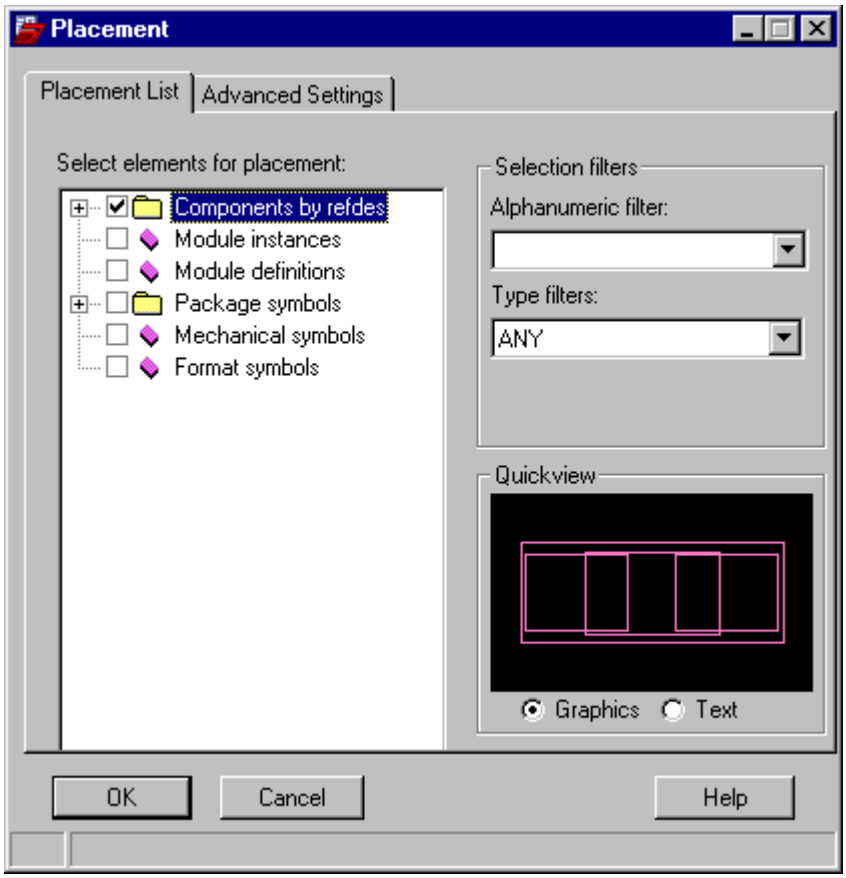


4. Move the cursor to the Allegro PCB Editor window and place all the reused modules on the board.

5. Click OK to close the Placement dialog box.

6. Select **Place > Manually** to place other components.

7. Select Components by refdes. If you have the correct **psmpath and padpath**, you can view the footprint symbol within the Quickview window.



8. Move the cursor to the Allegro PCB Editor window and place all the components on the board.

Reuse properties

This section defines reuse properties that are added to the components in reused modules.

REUSE_ID:

This property is added to every part in a reuse design. Within a reuse design there are as many values of this property as there are packages so that each package has a unique REUSE_ID. All parts in a package have the same REUSE_ID value. Capture assigns these property values when you enable the Generate Reuse Module in the Allegro Reuse tab of the Annotate dialog box.

REUSE_PID:

If a reuse module contains another reuse module as part of its external design, then the netlister assigns a REUSE_PID value to every component in each package of the external design. The value of the REUSE_PID is the same as the value of the component's previous REUSE_ID. A new REUSE_ID value is then assigned to each module. This way, occurrences of the same module will have different REUSE_IDs on them, but the same REUSE_PIDs for corresponding components. Using REUSE_IDs, makes it possible for Capture to propagate changes to lower levels of a reuse module.

REUSE_NAME:

The default value of the REUSE_NAME property, assigned by the netlister, is a concatenation of the design name and the schematic name coupled by an underscore character. Here is an example:

<testmodule>_<schematic1>

The REUSE_NAME property is propagated down throughout the design hierarchy to all parts below.

REUSE_INSTANCE:

This value is computed by the netlister and added to the netlist. The value of this property is unique for each usage, or instance, of a reuse module. A design may have one REUSE_NAME value but many REUSE_INSTANCE values.

The REUSE_INSTANCE property is obtained from the name of the referencing hierarchical part. If a REUSE_INSTANCE property is not present, is created as follows:

< REUSE_NAME >_<document ID of the referencing hierarchical part>

Like the REUSE_NAME property, the REUSE_INSTANCE property is propagated down throughout the design hierarchy to all parts below.

REUSE_MODULE:

Allegro PCB Editor assigns this property as a unique name to identify a physical reuse module. The property corresponds to placed and routed board in Allegro PCB Editor (.brd file) which has been saved as an .mdd file. If this property is user-defined in Capture, it specifies the reuse module to use in PCB Editor.