# APPENDIX

use a toroidal or shielded inductor. See Table 5 for a list of inductor manufacturers.

Table 5. Inductor Manufacturers

| | | |
|---|---|---|
| Coilcraft | MSD7342<br>XAL6060 Series | www.coilcraft.com |
| Vishay | IHLP-2020BZ-01<br>IHLP-2525CZ-01<br>Series | www.vishay.com |
| WÜRTH | WE-PD<br>WE-DD<br>WE-TDC Series | www.we-online.com |
| Cooper Bussman | Octa-Pac Plus<br>DRQ-125<br>DRQ-74 Series | www.cooperbussmann.com |
| Sumida | CDR6D28MN<br>CDR7D28MN<br>Series | www.sumida.com |
| Taiyo Yuden | NR Series | www.t-yuden.com |
| TDK | VLF, SLF, RLF<br>Series | www.tdk.com |

### Minimum Inductance

Although there can be a trade-off with efficiency, it is often desirable to minimize board space by choosing smaller inductors. When choosing an inductor, there are three conditions that limit the minimum inductance: (1) providing adequate load current, (2) avoiding subharmonic oscillation and (3) supplying a minimum ripple current to avoid false tripping of the current comparator.

### Adequate Load Current

Small value inductors result in increased ripple currents and thus, due to the limited peak switch current, decrease the average current that can be provided to the load. In order to provide adequate load current, L should be at least:

$$L_{BOOST} \quad \frac{DC\ (V_{IN}-V_{CESAT})}{2\ f_{OSC}\ \left(I_{PK}-\frac{V_{OUT}\ I_{OUT}}{V_{IN}}\right)} \Bigg\} \text{Boost Topology}$$

or

$$L_{DUAL} \quad \frac{DC\ (V_{IN}-V_{CESAT})}{2\ f_{OSC}\ \left(I_{PK}-\frac{|V_{OUT}|\ I_{OUT}}{V_{IN}}\right)\ I_{OUT}} \Bigg\} \text{SEPIC or Inverting Topologies}$$

where

$L_{BOOST}$ = L1 for boost topologies (see Figure 5)

$L_{DUAL}$ = L1 = L2 for coupled dual inductor topologies (see Figures 6 and 7)

$L_{DUAL}$ = L1 || L2 for uncoupled dual inductor topologies (see Figures 6 and 7)

DC = Switch duty cycle (see Power Switch Duty Cycle section in Appendix)

$I_{PK}$ = Maximum Peak Switch Current; should not exceed 3A for a combined SWA + SWB current, or 1.7A if only SWA is being used.

$\eta$ = Power conversion efficiency (typically 88% for boost and 82% for dual inductor topologies at high currents)

$f_{OSC}$ = Switching frequency

$I_{OUT}$ = Maximum load current

Negative values of $L_{BOOST}$ or $L_{DUAL}$ indicate that the output load current $I_{OUT}$ exceeds the switch current limit capability of the LT8582.

### Avoiding Subharmonic Oscillations

Subharmonic oscillations can occur when the duty cycle is greater than 50%. The LT8582's internal slope compensation circuit will avoid this, provided that the inductance exceeds a certain minimum value. In applications that operate with duty cycles greater than 50%, the inductance must be at least:

$$L_{MIN} > \frac{(V_{IN}-V_{CESAT})\bullet(2\bullet DC-1)}{1.7A\bullet f_{OSC}\bullet(1-DC)}$$

where

$L_{MIN}$ = L1 for boost topologies (see Figure 5)

$L_{MIN}$ = L1 = L2 for coupled dual inductor topologies (see Figures 6 and 7)

$L_{MIN}$ = L1 || L2 for uncoupled dual inductor topologies (see Figures 6 and 7)