NOTE This document contains references to Agilent Technologies. Agilent's former Test and Measurement business has become Keysight Technologies. For more information, go to www.keysight.com.

CAUTION You should be logged in the space to access Advanced Design System 2017 documents and links to more detailed information. Please login using your Knowledge Center login credentials.

Advanced Design System 2017 Update Release Notes

ADS 2017 Update 0.2 Release Notes

Release: Feb 27, 2018

Version

470.update0.2

Install Instructions

Unlike other ADS minor updates, ADS 2017 Update 0.2 is not an addon but a full installer. Before installing ADS 2017 Update 0.2 it will uninstall any previously installed ADS 2017 (ship or update 0.1) and then perform a fresh installation for Update 0.2. For more information refer to ADS 2017 Update 0.2 installation instructions document.

Platform Support

- **Supported Platforms**: Windows and Linux 64-bit.

Issue Addressed

ADS 2017 Update 0.2 addresses issue related to Circuit Simulation, Data Display, Design Editing, Design and Technology Management, EM Integration, IC Design Flow, and SIPro/PIPro.

Circuit Simulation

- HiCUM v2.33 model is now re-evaluated when sweeping a design parameter.
- Fixed the result mismatch issue in SP and SP noise (nfmin) between ADS and Spectre.
- Fixed the issue where removing SnP file closes the Touchstone Combiner window.
- You can now open the AMI tab on the Tx_AMI and load the AMI file, and see all of the AMI parameters.
- Fixed the crash that occurred when importing an IBIS Model file.
- An incorrect message "[Algorithmic Model] Sub parameter (null) is not allowed for ..." is no longer shown.
- Netlist based simulation which includes a Global Foundries device now reports non zero value for NFmin.
- Fixed the issue were ADS parser reported unsupported operators and syntax errors for GF 22nm V1.2.0 models.
- Circuit envelope simulation is now more accurate and fast, it can simulate a circuit with both timesteps.
- Corrected the behavior for HiSIM HV in Hspice netlist mode.
- Added the Disable button to Data Display window.

Data Display

- New custom toolbar is now visible even after restarting the ADS session.
- Disable toggle button is added back on the Zoom toolbar.

Design Editing

- **Improvements to snapping to vertical, horizontal, and diagonal lines** - ADS 2017 snaps the mouse to a position on vertical, horizontal, or diagonal (45 degrees) from the previous click in layout. Previously this could interfere with snapping to a pin, vertex, midpoint, etc. In this update, the mouse will snap to pins, vertices, midpoints, circle/arc centers, and intersections in accordance with snap preferences, even if these points are not on a vertical, horizontal, or diagonal line from the previous mouse click. The mouse will snap to edges and centerlines (if that preference is set) provided the snap point is on a vertical, horizontal, or diagonal line from the previous mouse click.
- Fixed the crash While deleting the length of the Edge Pin in layout window.
- Added APIs to check and set the Library Technology interoperability mode.
- Removed the warning message "Antipad SameAsKeepout not implemented" while closing the Via Definition dialog box.
- Fixed the Manufacturing grid error where after setting the Manufacturing Grid to 0.05um, the path moved 0.075um distance where as the shape was supposed to move to 0.05um distance.

Design and Technology Management

- For interoperable components, the search for SimInfo based on the view name will now assume spectre simulation by default. If the chosen view name does not have a matching SimInfo section in the CDF, we look for a spectre SimInfo section. If you want to override this behavior, you can set the variable DefaultSimInfoName in the $HOME/hpeesof/config/de_sim.cfg file. If you don't want any default, then set the name to None (something that doesn't match any SimInfo name).
- Substrates are now listed in the Folder view of the ADS Main window.
- Fixed the crash when EditStackupDialog retrieves info from a referenced library that has no technology.
- Added an AEL API to check and set the library technology interoperability mode.
- Added the *dm_get_formset_form_names()* function that works for custom formsets.

Examples and DesignGuides

- Fixed the license issue of the shipped example 'VAMS_Examples_wrk' under **$HPEESOF_DIR\examples\Behavioral_Models\Verilog-A_and_AMS.**

EM Integration

- Fixed the port setup in the interoperable Circuit/EM cosimulation flow. In the auxiliary cellview that is to be EM simulated ('..._emCosim:layout'), all pins connecting to the same circuit component term will be grouped together in the corresponding port setup. That reduces the number of ports in the EM simulation without impacting the accuracy.

FEM

- Fixed the incorrect (open circuit) results when an edge pin is slightly larger than the geometry's edge.
- Improved and enhanced the distributed FEM simulation.
- Reduced the memory consumption for large designs with many ports, this can have an possible impact of increased simulation time up to 10-15% depending on the machine and design.

Via Designer

- Fixed an issue where the geometry did not update correctly.

IC Design Flow

- LVS
  - Improve the net mapping for complex un-synchronized designs.
  - Run Batch LVS with option component mapping parameter values.
  - Run Batch LVS with option "Check net names" off.
  - Improve error messages for invalid setup.
- DRC
  - Load results when technology is read-only without triggering version control activity.
  - Highlight errors without modifying the master layout design.
  - Show the results for the specified job when displaying the dialog.
  - Extend the chip area to include oversize and compensate values.
  - Job name pull down now lists jobs that have a dot in the job name.
  - Default circle resolution is now set to 5 degrees.
  - Display fixed errors under a different header.
  - Add the Auto select check box.
- Assura DRC Link
  - Group DRC errors by error message and output layer.
- IP Encoder
  - Fixed the issue where encoding netlist gives the "view name not specified" error.

Signal Integrity/Power Integrity (SIPro/PIPro)

- PIPro schemaitc test bench creation now works properly with newly updated newly update Murata adslibrary version1707.
- SIPro/PIPro setup now opens properly if the *lib.defs* contains the invalid path of ADS design kits.
- SIPro/PIPro cell names does not allow special characters such as *()[]{}/<>?!,;:'"|.
- Fixed the special character treatment with SIPro/PIPro schematic.
- Reduced the memory consumption for SIPro or PIPro-AC simulations for large designs with many ports and components, this can have an possible impact of increased simulation time up to 10-15% depending on the machine and design.

ADS 2017 Update 0.1 Release Notes

Release: Dec 20, 2017

Version

470.update0.1

Platform Support

- **Supported Platforms**: Windows and Linux only.

Issue Addressed

ADS 2017 Update 0.1 addresses issue related to Design Editing or Platform.

Design Editing

- Fixed the crash when a named wire is deleted from a schematic design.

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