Allegro FPGA System Planner User Guide

Product Version 17.2-2016 April 2016

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Synchronizing With FPGA Tools

Overview

FPGA design and PCB design have become increasingly parallel. In FSP, FPGA designer generate the top level design and constraints. Then designer run it through synthesis, place and route and simulation in other FPGA tools. Once the logic design meets all the timing and performance criteria, it is passed to PCB designer for symbol generation schematic entry and layout.

Here FPGA design starts with the pin constraints generated by FSP. However the logic designer may want to change the FPGA pin constraints at later stage to meet the logic timing.

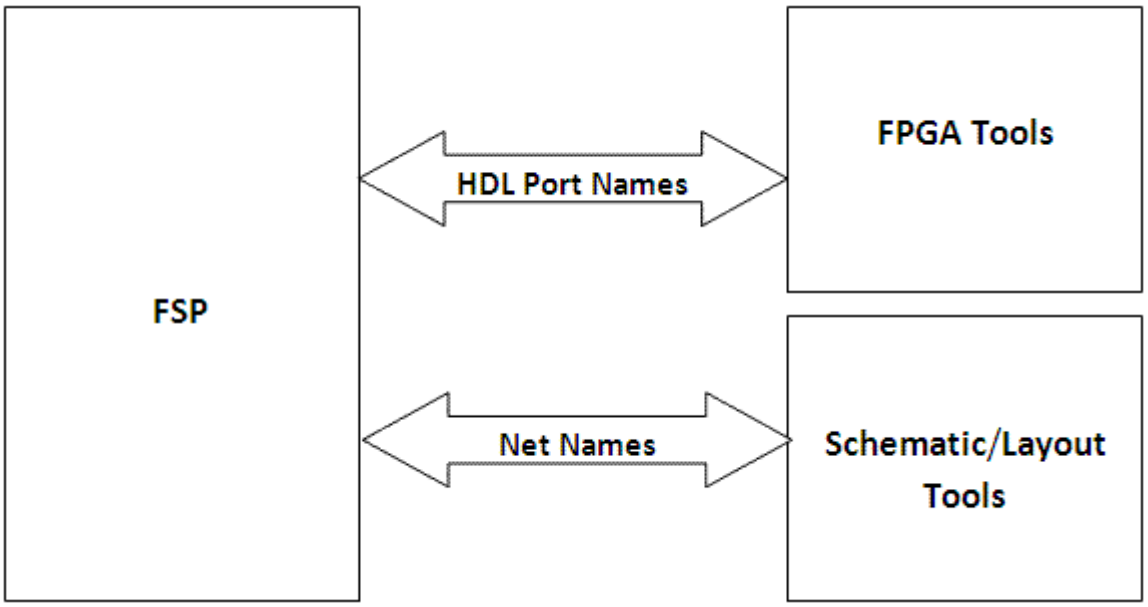
Synchronizing with FPGA tools is a flow that enables you to modify and update pin constraint and design files at any stage. An important advantage of the Synchronizing with FPGA tools flow is you can modify and update the pin constraint and design files until you meet your logic timings. You can do synchronization with various FSP features. The feature level details of synchronizing with FPGA tools flow are covered later in this chapter.

Net Name Convention

Net names for all signals are different in FPGA design and PCB design flow. For example in FPGA tools span of the net is till FPGA and in schematic/layout tool span of the net is throughout the entire design. If you are using the FPGA tool, you can use the same logic multiple times for different FPGA's in a single board. In such cases, nets connecting two different FPGA's can have a common name. However, to avoid editing constraints manually and ensuring that nets that are logically correct have different names, it is necessary to generate net names in two levels. The two levels are:

- FPGA Port Names
- Net Names

The figure below displays different net name flows supported by FSP.



FPGA Port Names

In FSP, FPGA Port names are applied to the FPGA ports level and are generated in constraint and verilog files. Further the generated constraint and verilog file are used to synthesis the design in other FPGA tools. Port names are useful while importing and exporting constraints and port mapping. When synchronizing with FPGA tools following are the different features where you use FPGA Port names:

- Mapping FPGA Port names and Use pins.
- Import Constraints
- Export Constraints

Design flows you use FPGA port names while synchronizing with FPGA tools process are listed below:

- Design Flow starts with FSP
- Design Flow does not start with FSP

Design Flow starts with FSP

- Initialize a design in FSP
- Generate full constraints or partial constraints. See Exporting Constraints section.
- Take the files to FPGA tools with RTL design. Run design and PAR for the design.
- Generate the constraints from FPGA tools.
- Import constraints in FSP and optimize it. See Importing Constraints from an External File and Optimizing with Constrained Settings section.
- Generate the constraints files.
- Map the ports with existing net names/port names and optimize it again. See Mapping FPGA Port Names and Use Pins section.

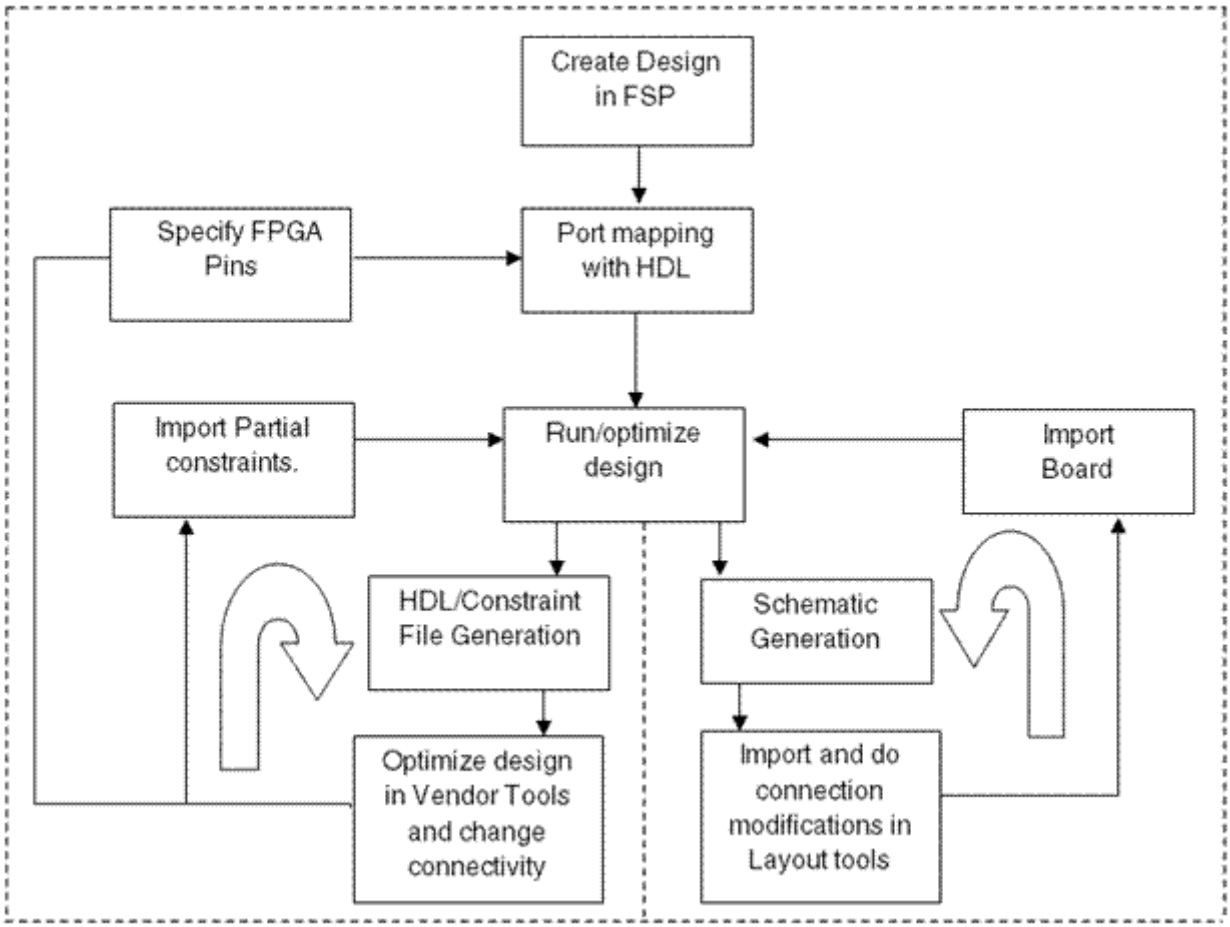
Design Flow does not start with FSP

In some cases, you may not want to create a design with FSP library interfaces. In these cases, you can create a virtual interface as per your preference by using FPGA files. After creating virtual interface follow the above Design Flow starts with FSP topic steps from two.

Net Names

Net names are applied to the design at the schematic level and are generated in schematics and design net list. These net names are then imported to Cadence Allegro FPGA (Concept), and Cadence Allegro CIS (OrCAD) tools.

The figure below describes how the FPGA Port names and Net names flow through the FSP, FPGA tools, and Schematic Tools.



Defining FPGA Port Names for FSP Nets

FSP generates constraint, Verilog and VHDL files that you can use to optimize design. FPGA port names are used as ports for each component used in the design to generate the constraint files. For each component pins you can define the port names as ports. These FPGA port names are saved as ports in constraints files and Verilog entity declaration file.

You can define FPGA port names through following form:

- Interface Instance Configuration form
- Device Instance Configuration form

- Edit Protocol form
- Virtual Interface form

You can specify the FPGA port names by:

- Manually entering the names under the FPGA port name column
- Mapping port names in Port Map form
- Importing Constraints

Defining FPGA Port Names for Interface Signals

To define port names for interface signals:

1. Right-click on the interface.

A pop-up menu with various options is displayed.

2. Select Configure Pins.

The Pin Property for Interface Instance dialog box is displayed.

3. Specify port names in the FPGA Port Name column.

Net names will be considered as port names if you do not define the port names here.

4. Click OK after specifying the port names.

Defining FPGA Port Names for Protocol Signals

To define port names for device signals:

1. Right-click on the FPGA.

A pop-up menu with various options is displayed.

2. Click Create Protocol.

The Create New Protocol dialog box is displayed.

3. Click > to move the device instance names to left side pane.
4. Click OK.

The Edit Protocol dialog box is displayed.

5. Specify port names in FPGA Port Name column.

Net names will be considered as port names if you do not define the port names in FPGA Port Name column.

6. Click OK after specifying the port names.

Defining FPGA Port Names for Virtual Interface Signals

To define port names for virtual interface signals,

1. Right-click on the device instance.

A pop-up menu with various options is displayed.

2. Place the mouse cursor over Virtual Interface option.

A small pop-up menu is displayed.

3. Click Create New Virtual Interface.

The Define Virtual Interface for Device Instance dialog is displayed.

Note: The Define Virtual Interface for Device Instance form is same as like Edit Protocol dialog box.

4. Specify port names under FPGA Port Name column.

Net names will be considered as port names if you don't define the port names here.

5. Click OK after specifying the port names.

Mapping Resources

Before mapping of FPGA port names and use pins and Importing Constraint process you must understand about the mapping resources feature. Resource mapping feature is useful while importing the IP generated sources and mapping the existing resources with the design resources. You can lock the constraints or relocate while re optimizing. Resources mapping is available at the time of ports and use pins mapping and while importing constraints.

There are two types of resources

- Dependent resources
- Independent resources

Dependent resources are available at interface levels and independent resources are available at FPGA levels.

This section covers the following:

- About Resource Mapping Window
- Mapping Resources

About Resource Mapping Window

The Resource Mapping UI is divided into two panes:

- Resource Mapping
- Resources

Resource Mapping

Resource mapping pane is divided into two columns:

- Group Name: Displays the name of the Device Instance name, Interface Instance name and interface groups in tree view. Click + in front of interface instance name to expand the hierarchy.
- Mapped Resources: By default the field is empty. You drop the resources from right pane to this column.

Note: You can add more resources in Mapped Resource column.

Resources

Displays all the used resources in FPGA after you import constraint files in first page both in FPGA Ports and Use Pin mapping and Import Constraints wizard. Resource pane has the following options:

- Hide Identical Resources: Select this option to hide the identical resources.
- Hide Comments: Select this option to hide the comments

Rules for Mapping Resources

Improper resource mapping is not checked by FSP in this wizard. FSP swaps the entire connections and resources of the complete group based on the following rules:

- Group Constraint should be identical
- Pin properties should be identical
- Number of pins should be identical
- Types of resources should be identical

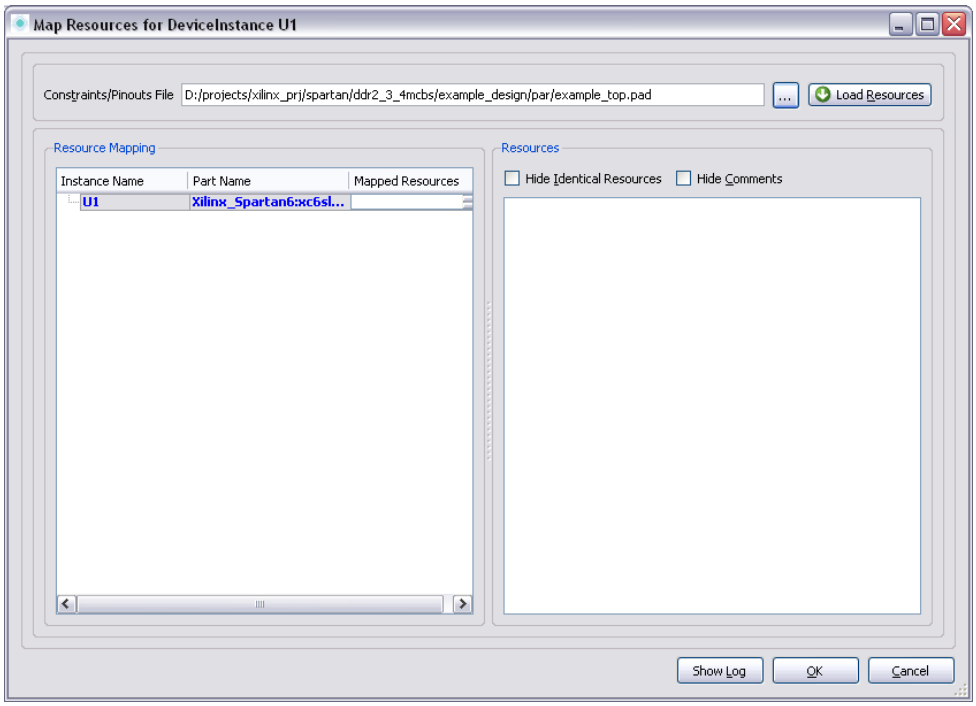
Steps to map the resources,

1. Right-click on the device instance and choose Constraints - Map FPGA Resources.

The Select Constraints File dialog box is displayed.

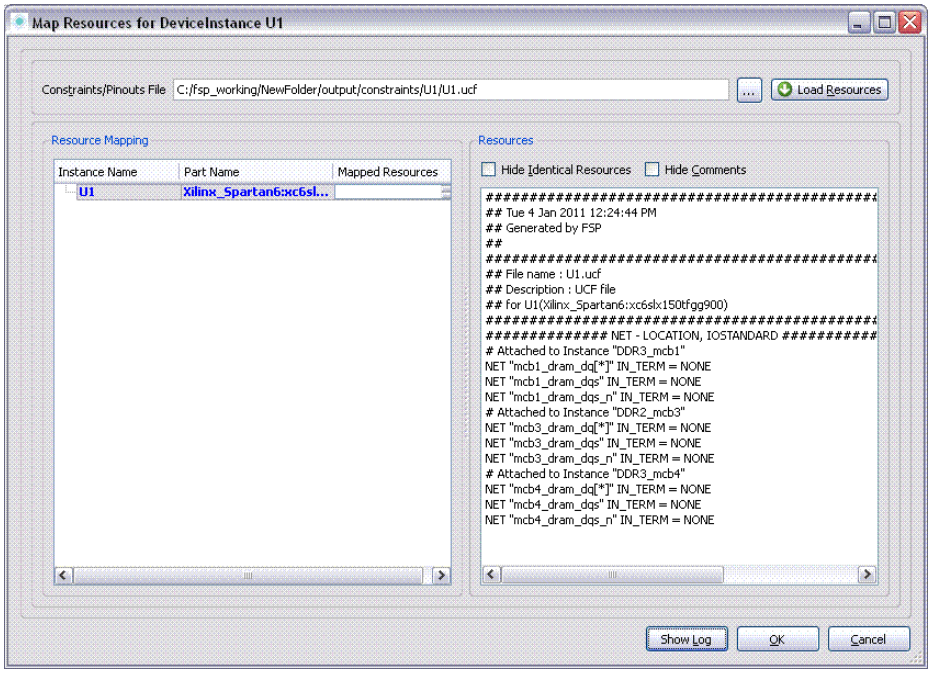
2. Browse to the file, select the file, and click Open.

The Map Resources For DeviceInstance dialog box is displayed.

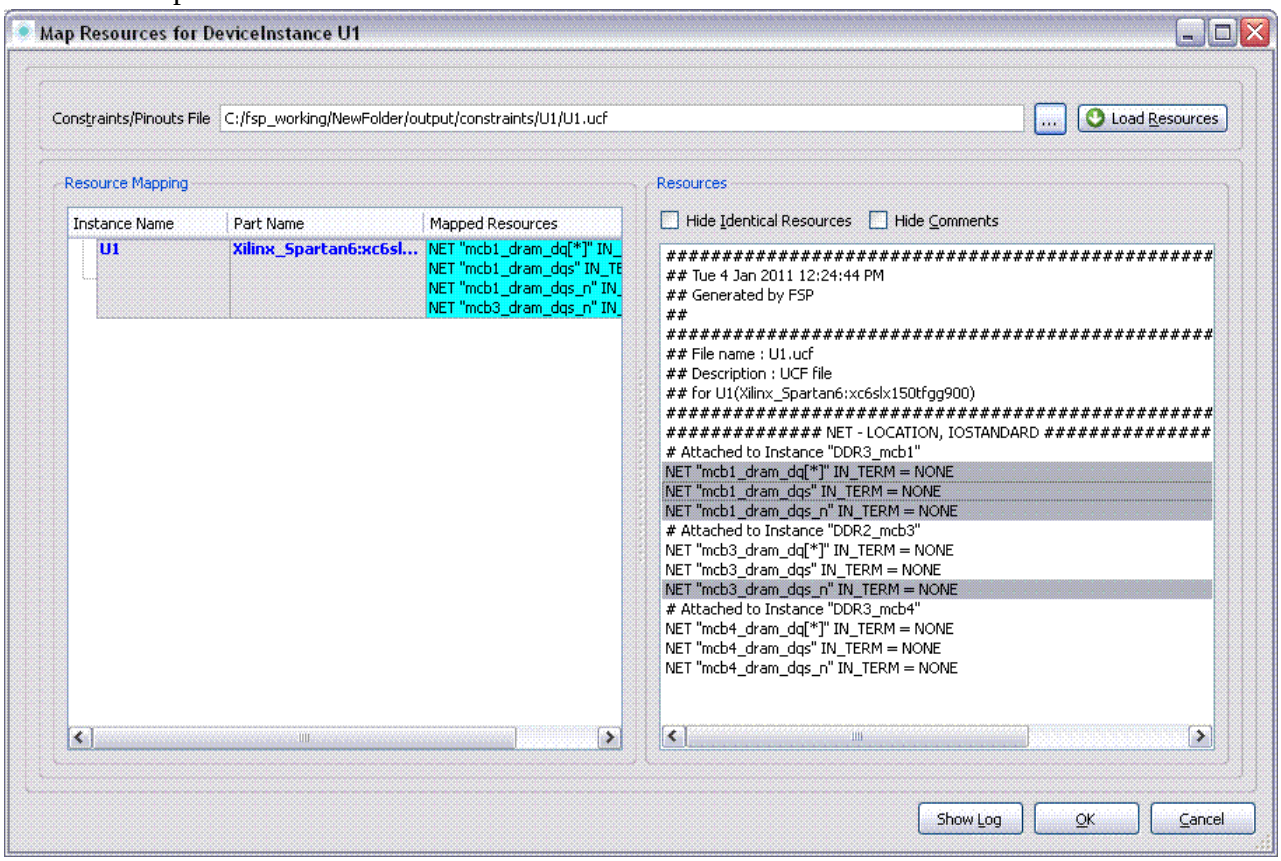


3. Specify the path to the constraints file in Constraint File field. Or click ... to browse to the constraints file location.
4. Click Load Resources.

The Resources is displayed in Resource pane.



5. Select Hide Identical Resources option to hide the resources which are identical.
6. Select Hide Comments option to hide the comments in Resource pane.
7. Select resource in Resource pane with mouse pointer.
8. Drag the resource from Resource Mapping pane and drop it in Mapped Resource column of Resource pane.



9. Click Show Log to see the reports.
10. Click OK.

Mapping FPGA Port Names and Use Pins

You can map FPGA port names from FPGA files for all signals connected to a device by using the Port Mapping window. This window also enables you to map the FPGA pin location constraints to the FPGA ports from constraint files. Port mapping window allows you graphically map FPGA port names and pin locations to the FPGA pins.

Understanding different Mapping Port names and Use Pins Scenarios

Before you start importing the files you must understand following scenarios:

- Having FPGA file but no Constraint file

You can use this form to map port names to nets.

- Having Constraint file but no FPGA file

You can use this form to set use pin constraint for FSP nets.

- Having both FPGA and UCF files

You can use this form to map both FPGA ports and use pin locations.

Step by Step Instruction for Port Mapping

Mapping of FPGA Ports and Use Pins are done on following basis:

- Existing Net Names
- Pin Names

Mapping Port Names and Use Pins with Existing Net Names

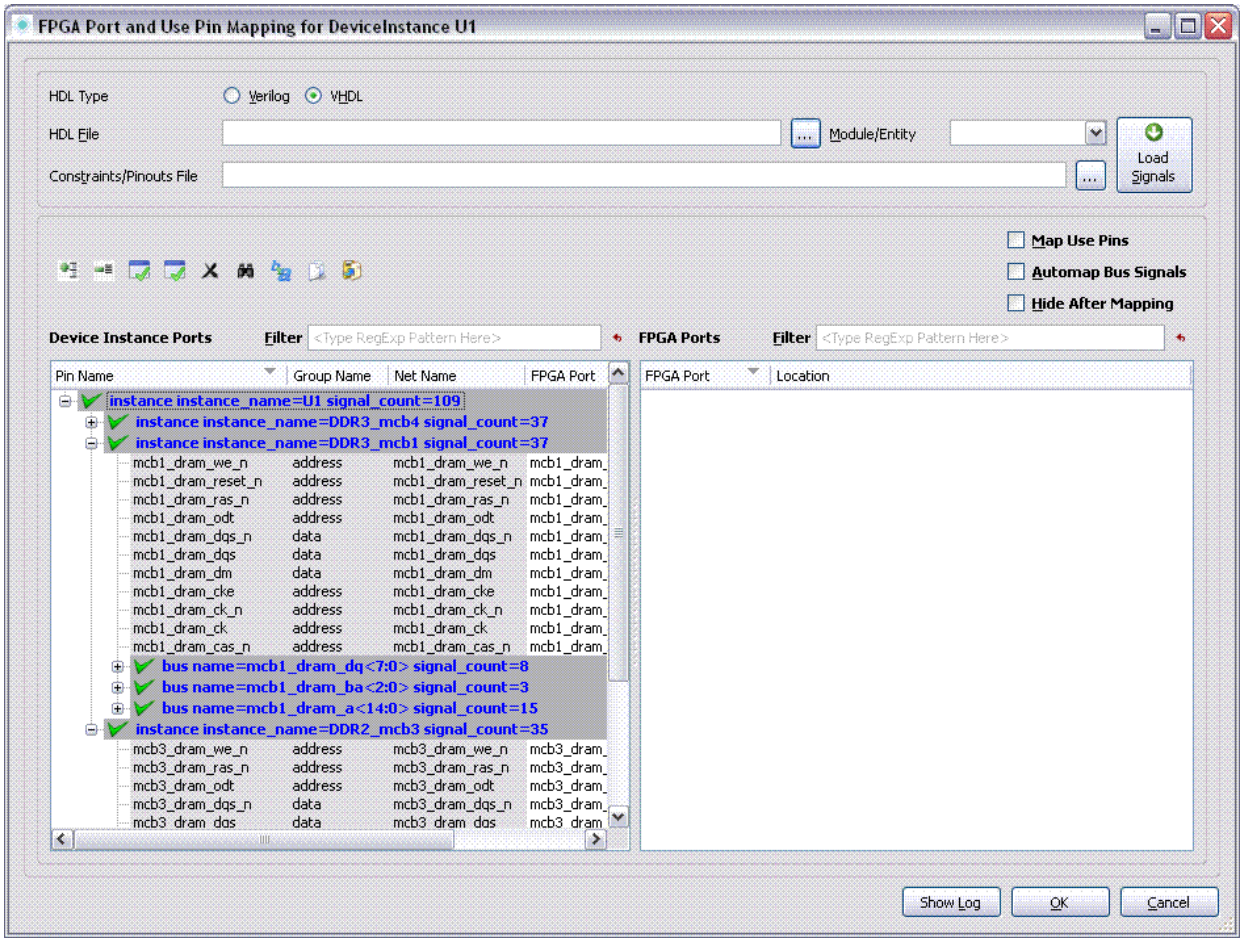
The Existing Net Name scenario is used to demonstrate the steps in mapping the port names and use pins.

The FPGA Port Mapping Wizard wizard guides you through a series of steps that you need to perform for FPGA port names and use pin mapping.

Importing Constraints and FPGA files

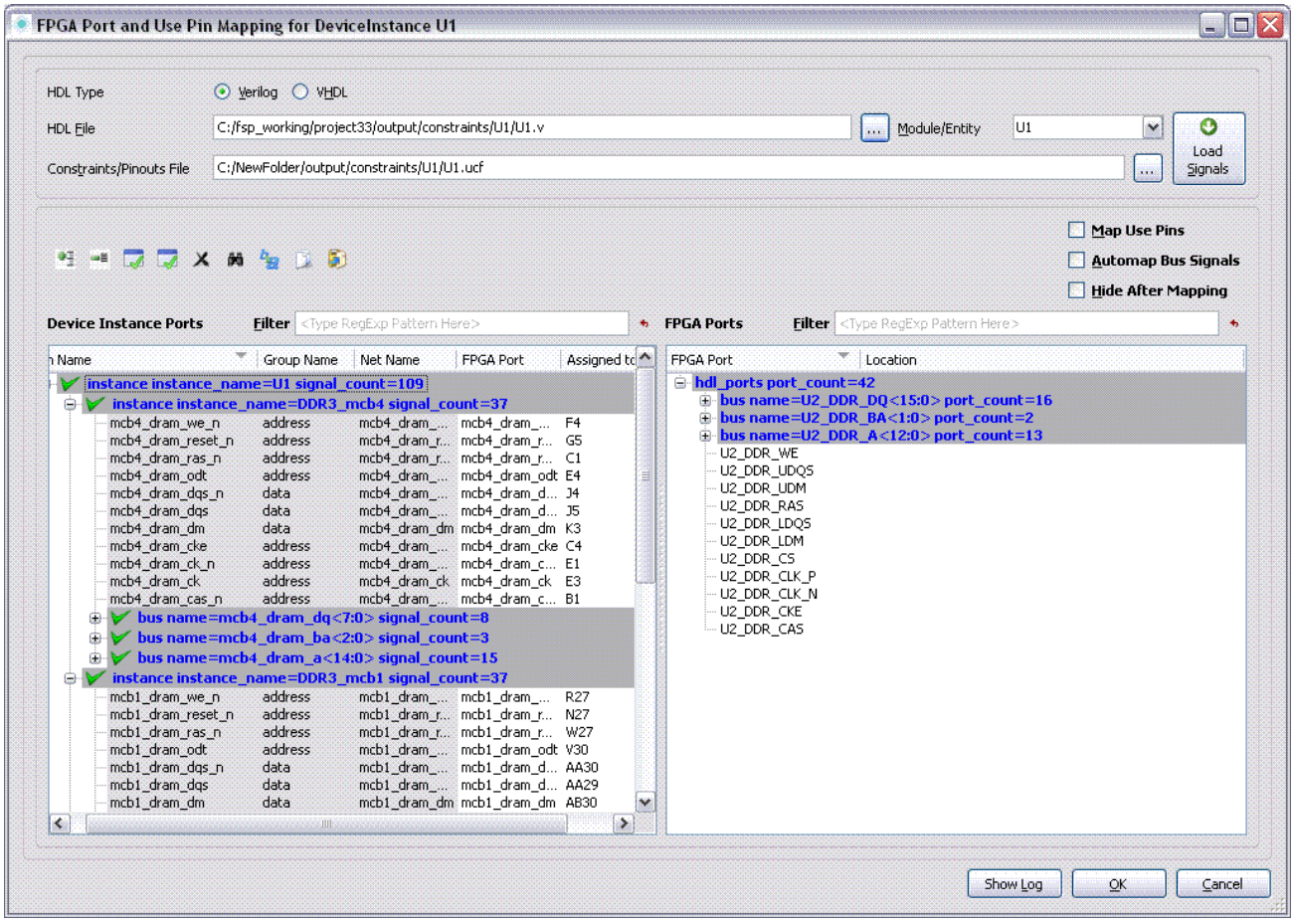
If connection exists in your design follow the below steps

1. Right-click device instance and choose Constraints - Map FPGA Port and Pins.
The Select Constraints File dialog box is displayed.
2. Browse to the file, select the file, and click Open.
The FPGA Port and Use Pin Mapping dialog box is displayed.

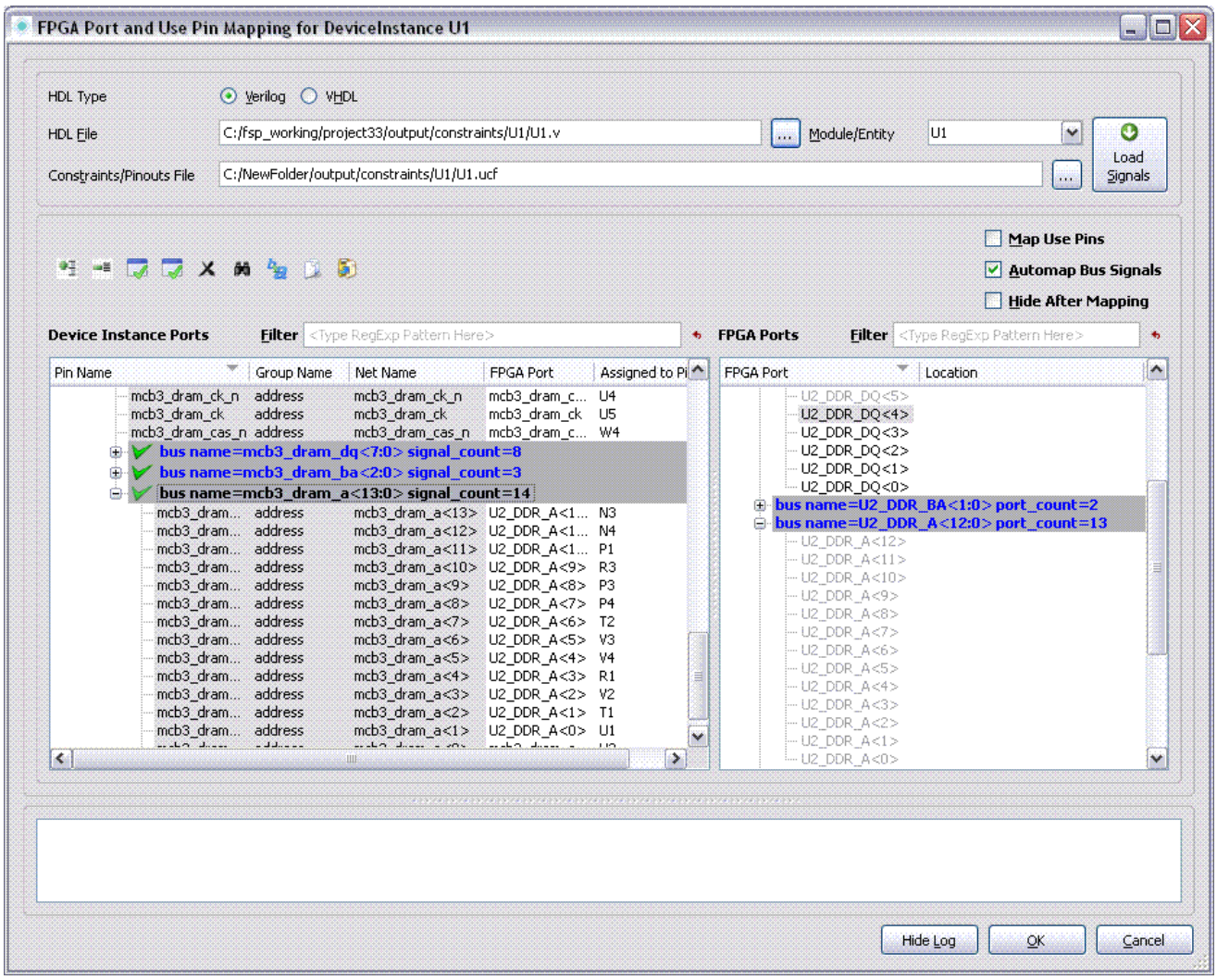


3. Select the type of file to import in HDL Type options field.
4. Select the appropriate Verilog or VHDL module in Module/Entity Field.
5. Specify the path to the verilog file in HDL File field. Or click ... to browse to the verilog file location.
6. Specify the path to the constraints file in Constraint File field. Or click ... to browse to the constraints file location.
7. Click Load Signals to display the FPGA Ports and Use Pin information in FPGA Ports pane.

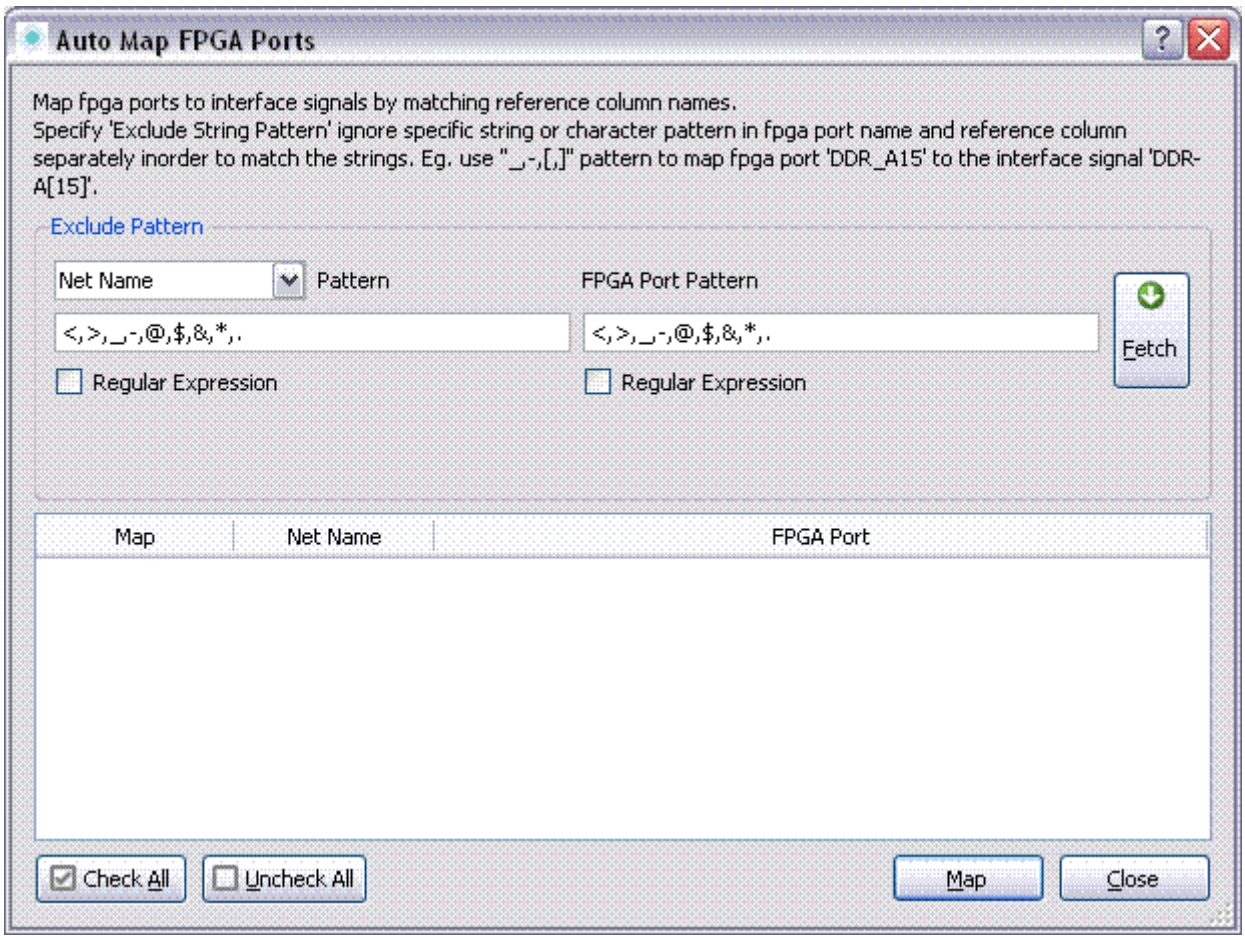
The FPGA Ports and Use Pin information is displayed in FPGA Ports pane.



8. Select Hide After Mapping option to hide the FPGA Ports and Use Pin in FPGA Port pane after mapping.
9. You can do the port mapping by using one of the following methods:
   - Select one or two FPGA ports in FPGA Ports pane to map the ports on pin level basis . Drag and drop to the required net under FPGA Port column of Device Instance Ports pane.
   - Select Automap Bus Signals option to map all the bits of a bus when mapping a single bit. Select a FPGA port in FPGA Ports pane. Drag and drop to the required net under FPGA Port column of Device Instance Ports pane.
   - Select the bus header item in FPGA Ports pane. Drag and drop to the appropriate bus item in Device Instance Ports pane to map the complete bus.



10. Click Auto Map FPGA Ports icon to auto map all the ports with single click.
The Auto Map FPGA Ports dialog box is displayed.



11. Specify the necessary options and patterns to match the FPGA ports to interface signals.

Note: For detailed information on regular expressions and field and buttons of Auto Map FPGA Ports dialog box see Auto Map FPGA Ports section.

12. Click Map to automap the FPGA Ports.

13. You can do the use pin mapping by using one of the following methods:

- Select one or two Use Pin names in FPGA Ports column to map the use pins on pin level basis. Drag and drop to the required net under Use Pin column of Device Instance Ports pane.
- Select Map Use Pins option to map the Use Pin when mapping FPGA Ports.
- Click Auto Map Use Pins icon to auto map all the use pins at single step.

After clicking the icon, a confirmation dialog box is displayed, Do you want to auto map use pins for mapped port names? Click Yes to complete the operation.

14. Click OK.

Note: If you design has connections, you may be prompted to remove the connections. Click Yes to remove the connections.

Note: After clicking Yes, entire group is deleted if any of the used pin updated in the group.

Mapping Port Names and Use Pins with Pin Names

If your design does not have connections follow the steps:

1. Follow the Mapping Port Names with Existing Net Names topic steps till step10.
2. Invoke Auto Map FPGA Ports Confirmation dialog box and select Pin Names option in Select Reference Column combo box and click OK.
3. Follow rest of the steps.

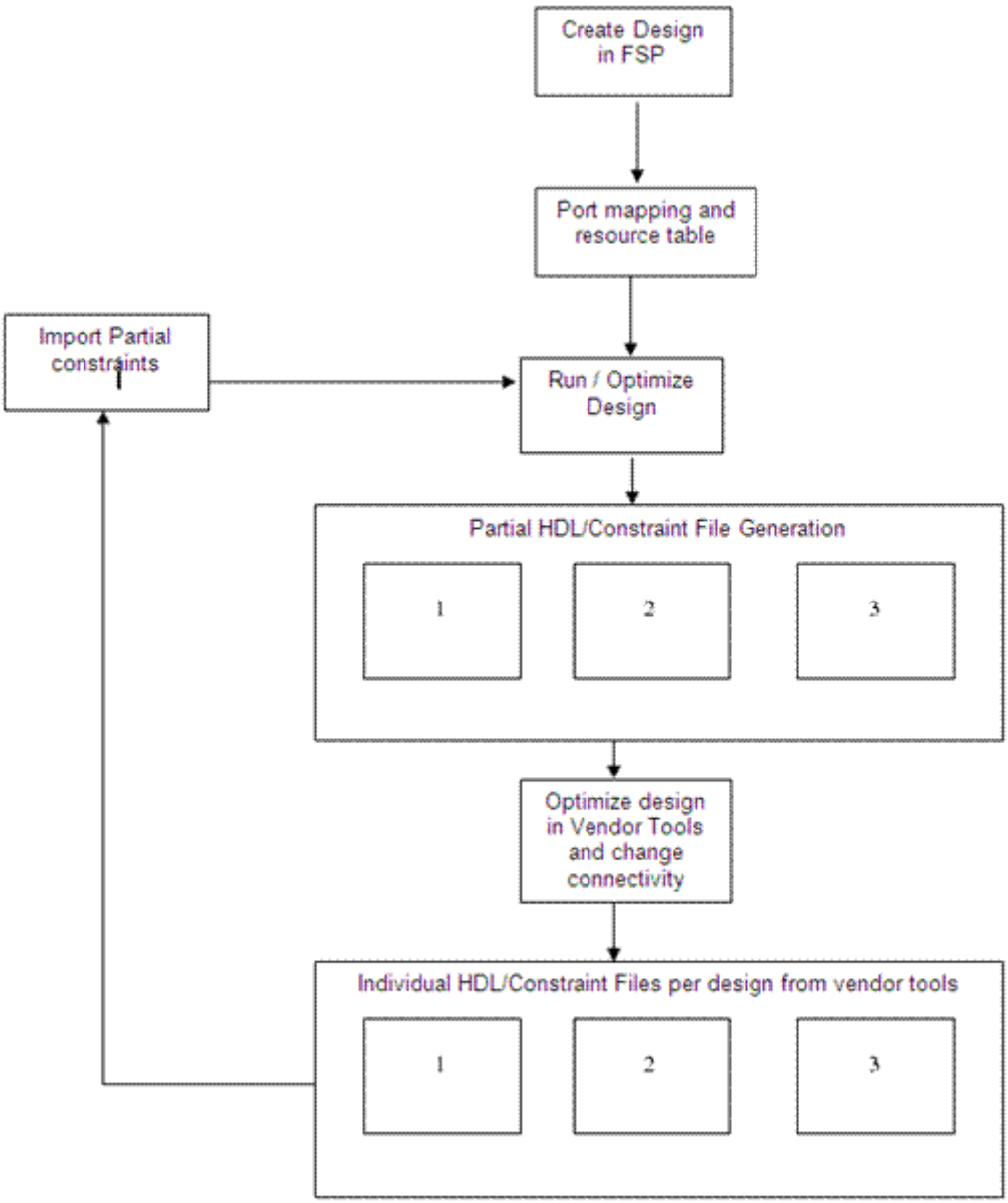
Importing Constraints from an External File

FSP helps you to re optimize the design based on inputs (for example port names and locations) available in constraint files. These constraints and inputs are present in the constraint files. In FSP and other FPGA tool design flow, you can design and optimize each partition and later integrate with the top level design. FPGA designers may develop their FPGA logic and pin assignments periodically. For example from the whole design designer starts working on High Speed Interfaces first and validates those pin assignments before moving to other part of the design.

To import constraints partially from the whole FSP design, you import partial constraints files individually and merge the constraints with rest of the FSP design.

Note: For Altera FPGAs, you can import constraints from the <file name>.pin file.

Following figure shows the functional relationship between the FSP and other FPGA tools for logic design and optimization analysis.



The following list describes the above flowchart Import and export flow process from FSP to other FPGA tools:

1. Creating a design in FSP.
2. Do port mapping, if you have constraints/FPGA files.

Or

Run the design.

3. Generate partial constraint files.
4. Import constraint files in other FPGA tools, optimize it and change connectivity as per your need.
5. Generate constraint/FPGA file individually from FPGA tools.
6. Perform the port mapping again and re optimize the design.

Note: In Step 7, if FPGA ports are not mapped you should perform port mapping. Or if FPGA ports are mapped you can always do import constraints.

About Constraint File

The Import Constraint feature allows you select the constraints individually. The constraint file that is read into FSP is a file that will typically have one or more of the following information:

- Port Name
- Pin Location
- IO standard
- Bank Number
- Resources

Import Constraints feature is available after or before running the design.

Note: For Altera FPGAs, you can import the constraints from an external file of format .pin; however, you cannot export the constraints to .pin file.

Step by Step Instruction for Importing Constraints

This section guides you through a series of steps required that you need to perform while Importing Constraints.

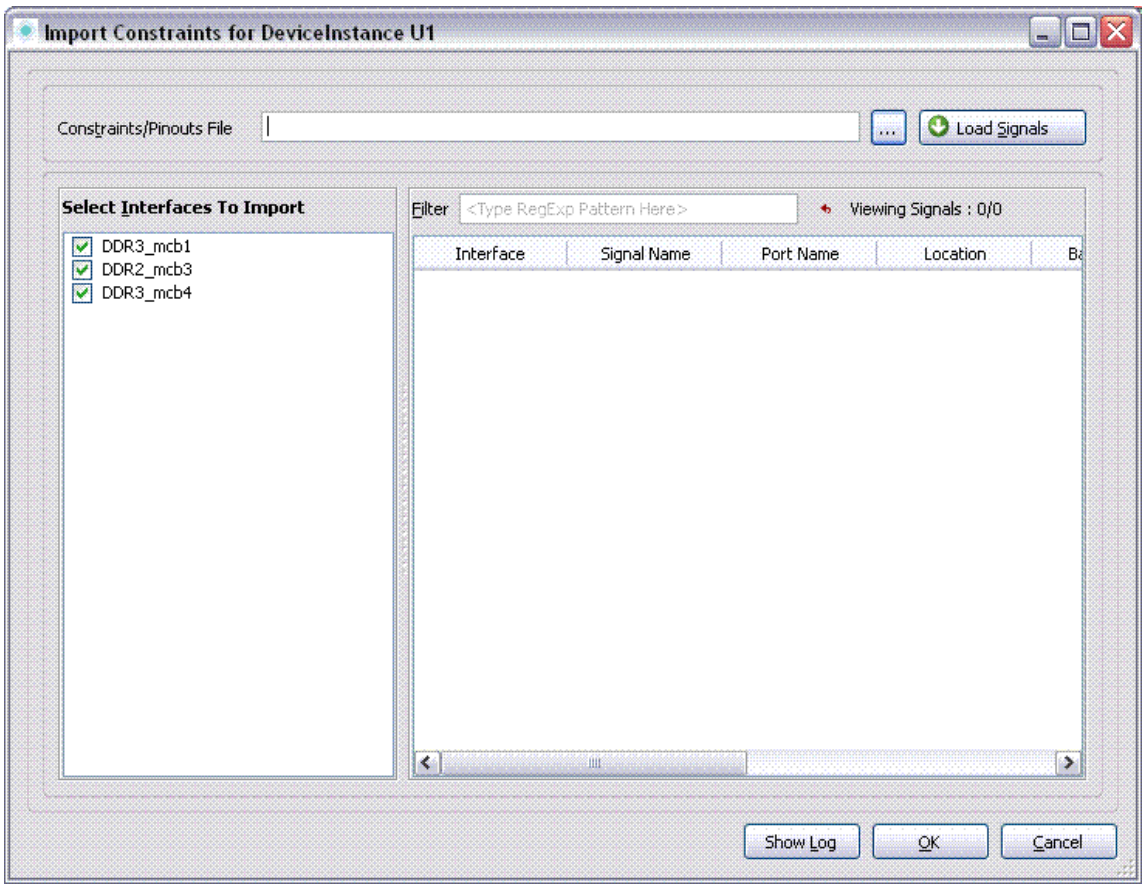
To Import Constraints follow the steps:

1. Right-click device instance and choose Constraints - Import Constraints.

The Select Constraints File dialog box is displayed.

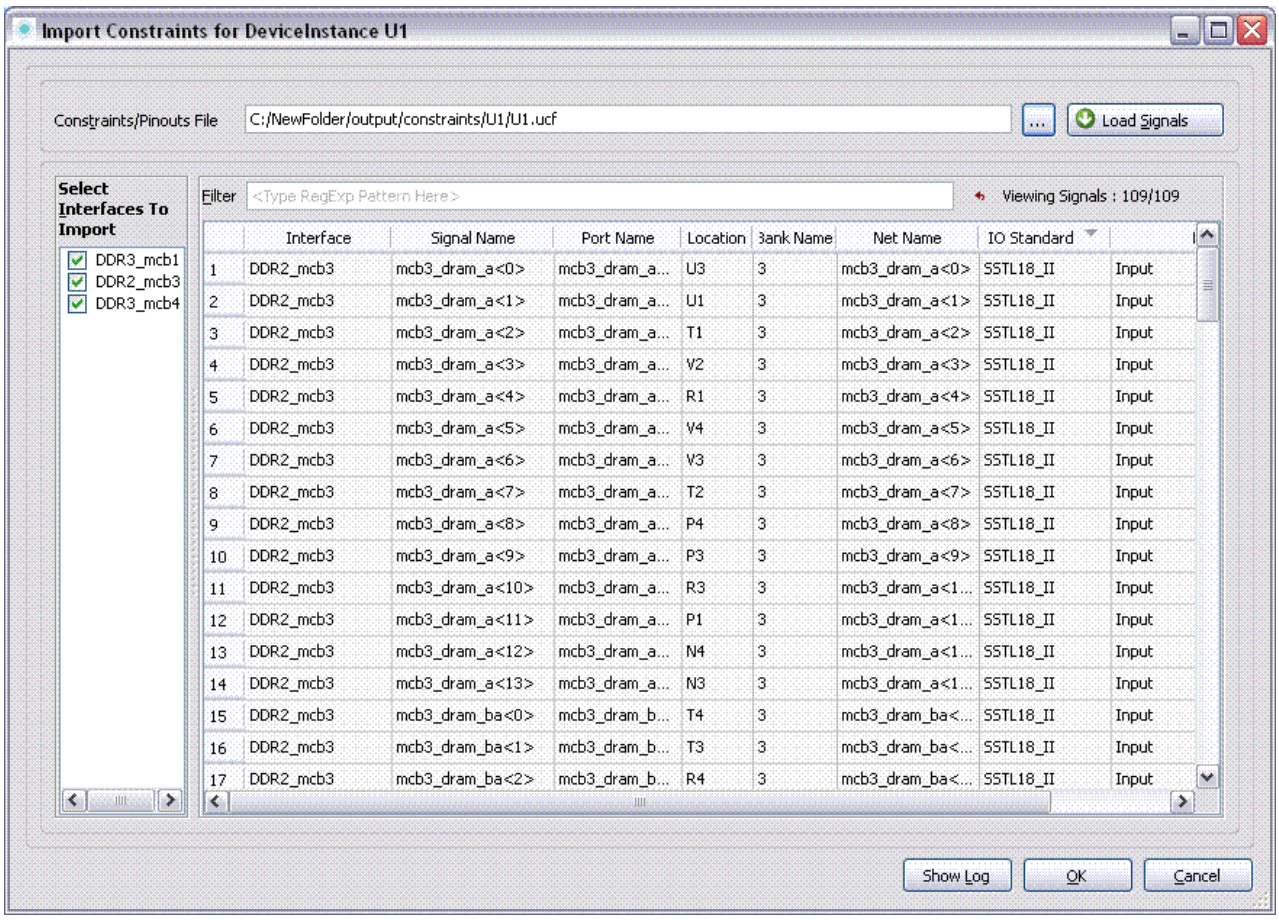
2. Browse to the file, select the file, and click Open.

The Import Constraints dialog box is displayed.



3. Specify the path to the constraints file in Constraint File field. Or click ... to browse to the constraints file location.
4. Click Load Signals.

The Constraint signals are displayed.



5. Select one interface and click OK to import the constraints of the selected interface.
6. Select all the interfaces and click OK to import the constraints for complete design.

Importing Details

After clicking Import, if the connectivity already exists, FSP updates the connectivity instantly based by checking all the DRC and connectivity defined in the model definition. FSP prompts you with an error message if do not find any pin information for all the pins in the group.

Points to Remember when Importing Constraint Files

The below figure describes the scenarios that you need to remember before or after importing constraints:

Scenario	Item
Net connected in FSP and present in UCF/QSF file	Updates the connectivity as per constraint file. FSP doesn't change the schematic net name when you import the constraints. Use pin will be set for all imported constraint signals.
User constraint signals present in both design and UCF/QSF.	Updates the connectivity

Use pin and connections exist in design.	FSP check the standard DRC's rules.
Prohibit Constraints	You need to map in resource section.

Importing Incomplete Constraints Files

Most of the times, other FPGA tools do not always generate complete constraints in files. For example:

- In Xilinx generated UCF files, IO standards are not generated for those pins which uses the default IO standard LVCMOS25.
- In Altera generated QSF files, pin locations are not generated for N side of the differential pairs, the assumption being made that the N side of the signal must connect to the N pin of N/P pairing of the FPGA.

When you import the constraints files, FSP reads the incomplete and defined constraints files and execute them properly by gathering all the missing and necessary information's.

Optimizing with Constrained Settings

Optimizing design is a key part of the design. Reducing compilation, improving timing performance, reducing resource usage are some of the key part of optimizing design. FSP provides you method for design optimization.

With the use of this feature you import IP design and use the same pin outs or you optimize them with different constrained optimization options. After optimizing you can check the connectivity in other FPGA tools and re import it. You can follow this process until you get satisfied with your pin outs for design.

Constrained Optimization

Constrained Optimization enables you optimizing pin connections in defined scope. This feature provides you with set of options to define the scope for optimization for set of pins. If the design does not fit into the device you want, you can try to optimize using the various options and settings. This feature is available only if the design has Use Pin information.

Points to Remember when working with Use Pin

When working with Use Pin following are the scenarios:

- Connections do not exist.

FSP stores the use pin information in Pin Property of Interface Instance form. If your design does not have connections and you the map the FPGA pins for component.

- Connections exist.

FSP prompts you with a confirmation window about removing connections in the design, if your design has connections.

Start Optimizing Design

You can start optimizing design after following process:

- FPGA Ports and Use Pins Mapping
- Import Constraints

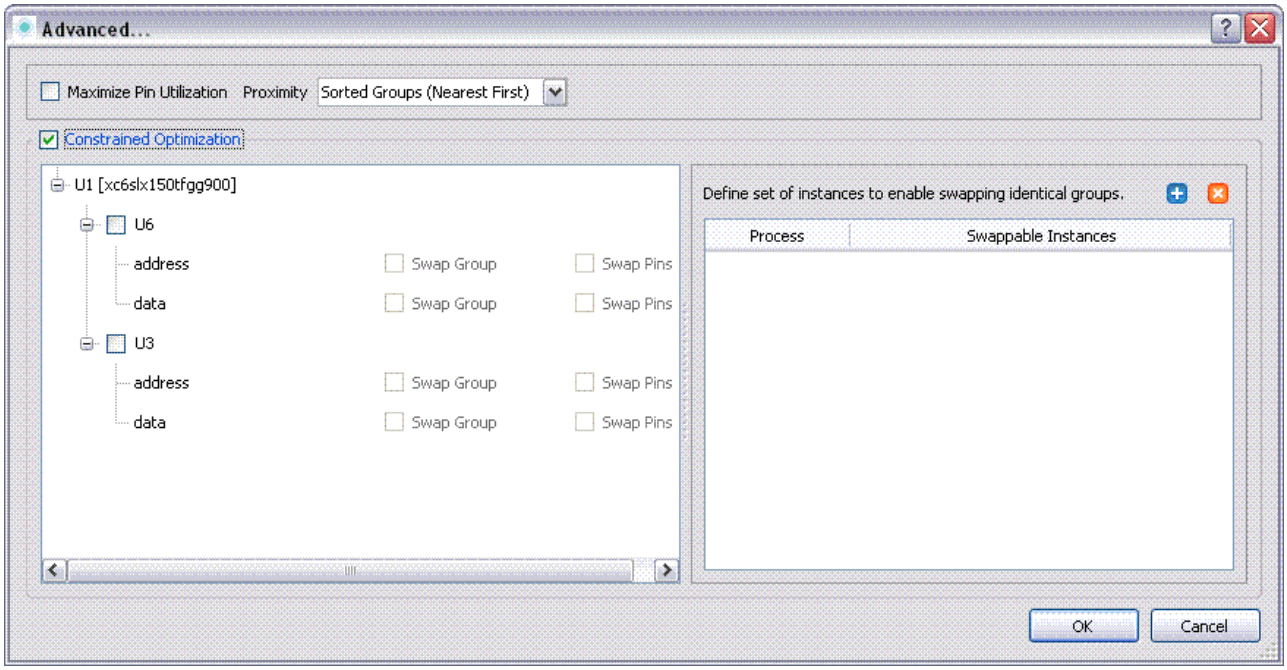
To optimize a design:

1. Choose Design - Run Design.

The Process Option Editor dialog box is displayed.

2. Click Advance of Device Instance.

The Constrained Optimization dialog box is displayed.



3. Click Constrained Optimization.

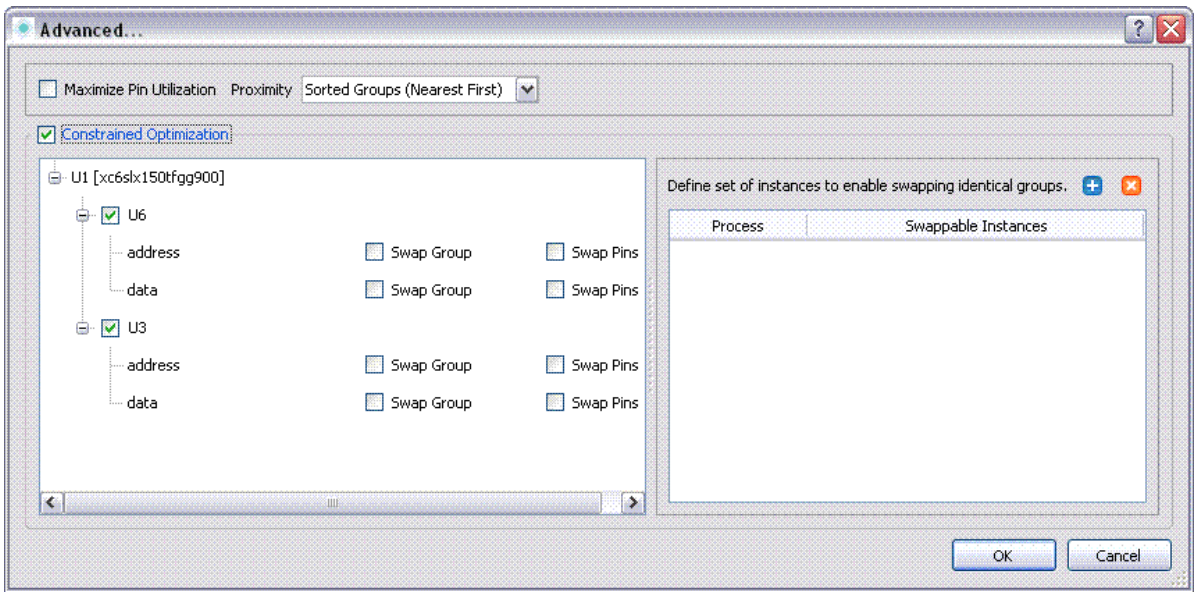
The Constrained Optimization pane gets enabled.

4. Select U3 to swap the U3 instance pins/groups within the instances.

Or

5. Select U3 and U6 if you want to swap the groups/pins within the two instances.

The Swap Groups and Swap Pins options get enabled.



6. Click Swap Groups check boxes to select the groups that need to be swapped.

Note: You cannot swap the Data group with Address group. See below for more information.

After selecting the Swap Groups, Swap Pins gets automatically selected and is in disabled mode.

Or

7. Unselect the Swap Groups to swap the pins across single group.

8. Click + icon.

A new row gets added in Define the Swappable Instance pane.

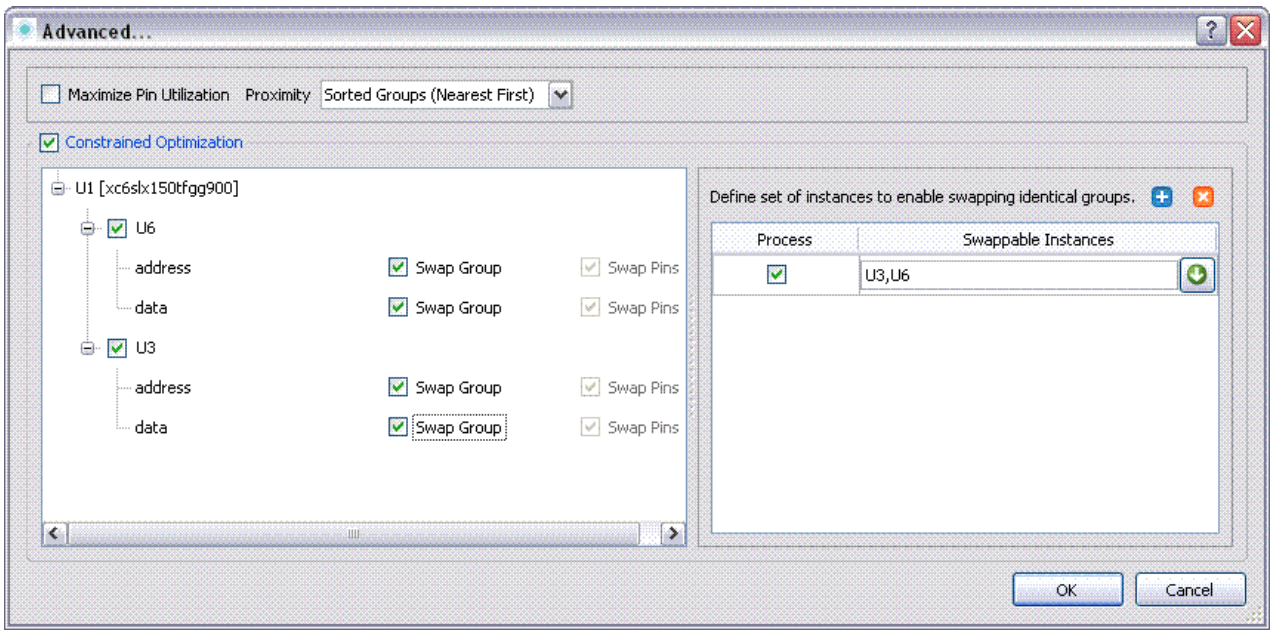
9. Select Process check box.

10. Click drop down button.

A pop-up menu with list of Instance names is displayed.

11. Select U3 and U6 to swap the pins between two interfaces.

Instance name gets added in the Swappable Instance text box.



Use X button to delete any row from the pane.

12. Click Run.

FSP checks following when optimizing at model level:

Action	Check
Swap pins in a group	If pin properties are same at model level
Swap all the pins of one group to other group	If number of pins in two groups and group properties are same
Swap all the pins of one interface to other interface	Both the interfaces should be identical logically.

Exporting Constraints

Designer working in top level designs can export their optimized project as a design partition. FSP provides you the option to export the partial constraints on interface basis. After taking these partial constraints to other FPGA tools, finally FSP lead designer take all these constraints and integrate with his design.

FSP enables you to export the partial constraints to a specific location. These option is helpful when FSP designer and FPGA designer work closely on same design. It may happen sometimes FPGA design files will not be located in same directory as the FSP design files.

Export Constraints dialog box allows you to export the partial or full constraints file at specified location.

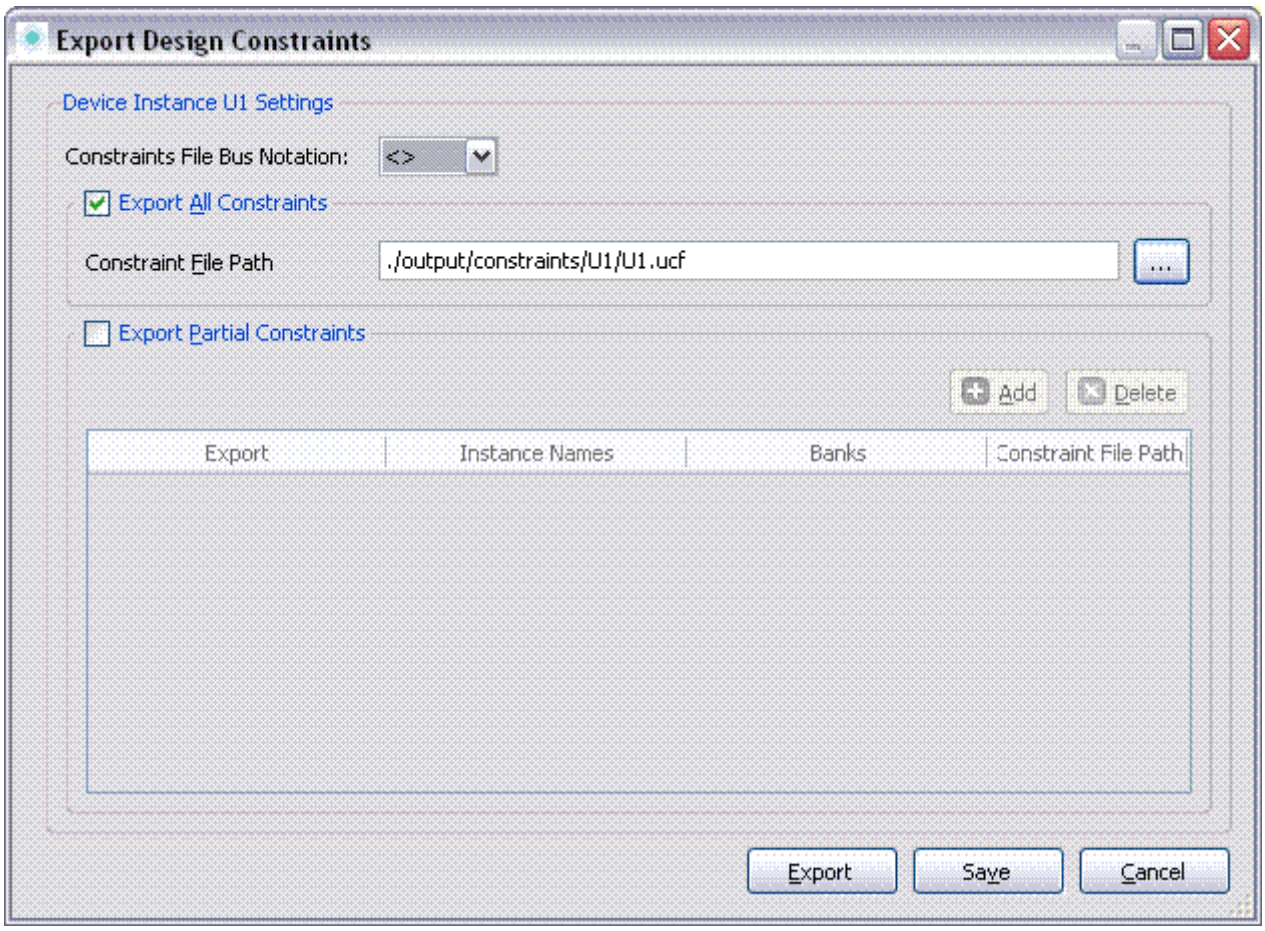
Before you start exporting the constraints you must understand following things:

- Use Export All Constraints- To generate the resources for complete design.
- Use Export Partial Constraints- To generate the resources at instance level and specify the instance generate constraints.

Exporting All Constraints

To export the constraints follow the below steps:

1. Right-click device instance and click choose Constraints - Export Constraints.
The Export Design Constraints dialog box appears.



2. Select the Bus Notation to output the signals with selected notation.
3. Click Export All Constraints if you want to export all the constraints.
4. Specify the directory in which to save the constraints file in Constraint File Path field. Or click ... to browse to the location of the constraint file.

Note: By default the project output folder directory is displayed.

5. Click Export.

Exporting Partial Constraints

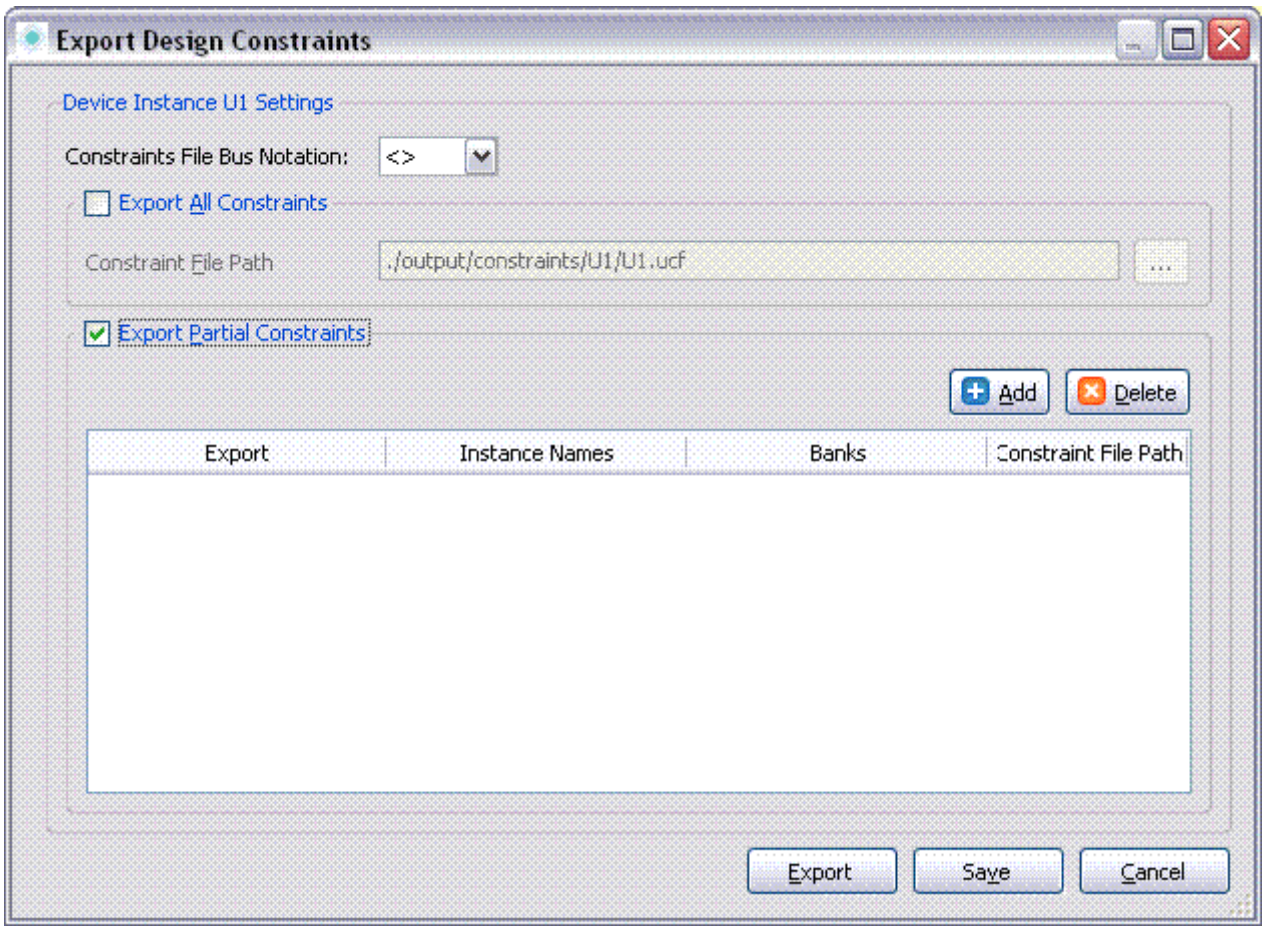
To export the constraints follow the below steps:

1. Right-click device instance.

A pop-up menu with various options is displayed.

2. Click Export Constraints.

The Export Design Constraints dialog box is displayed.



3. Select the Bus Notation to output the signals with selected notation.
4. Click Export Partial Constraints option to export constraints partially.
5. Click Add.

A new row gets added to the Export Partial Constraints grid.

6. Select Export option.
7. Click .

A pop-up menu with list of interfaces names is displayed.

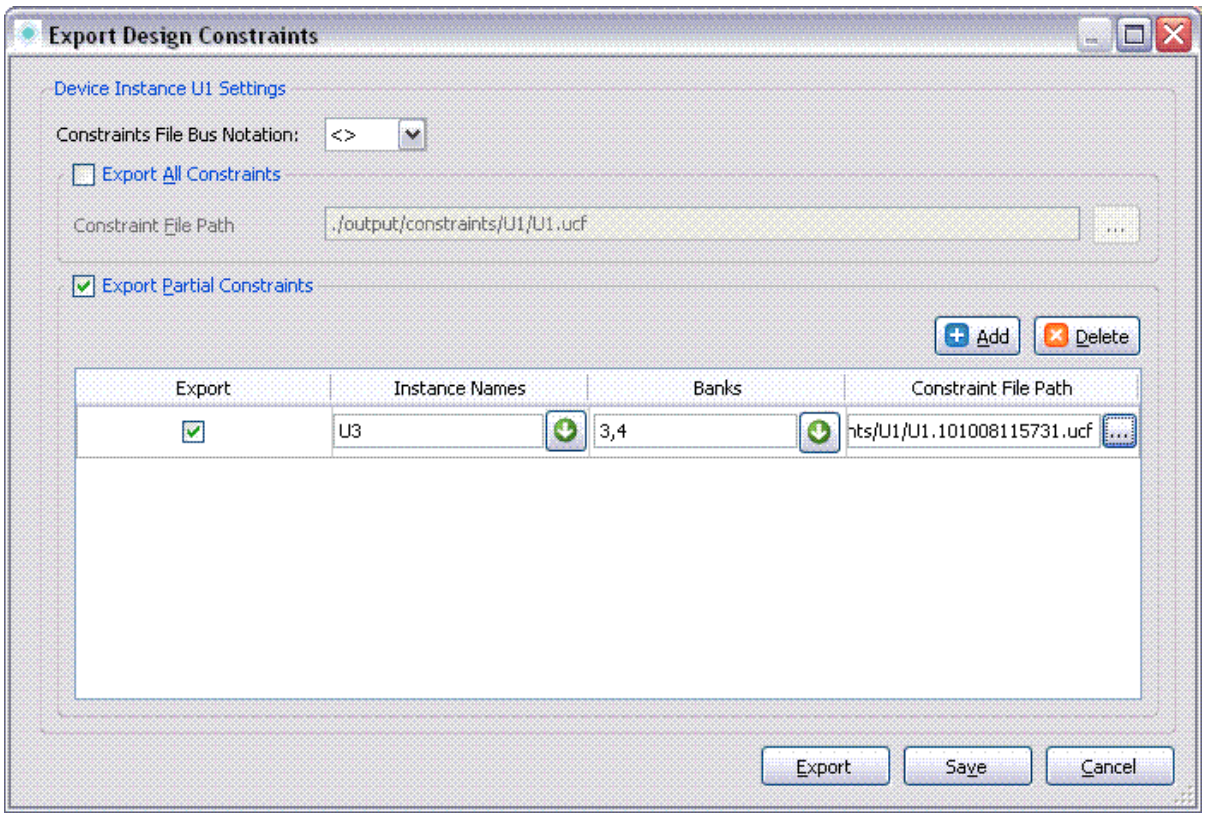
8. Select one or more interfaces.

Note: With this option you can generate single or multiple constraints files with multiple interfaces, protocols.

9. Click and select one or more banks.

The device view of the FPGA and list of banks is displayed.

10. Select one or more bank numbers and click OK.
11. Specify the directory in which to save the constraints file. Or click and select the location under Constraint File Path.



12. Click Export.
After clicking Export the constraints file with selected settings is generated in specified path. It generates both verilog,VFPGA and ucf files with same name.

13. Click Save to save the settings.

Swapping Groups

This topic describes the following:

- Overview of Swapping Groups
- Swapping Groups Within an Interface
- Swapping Groups Between Two Interfaces

Overview of Swapping Groups

You can use the FSP to swap the groups. You can perform the individual swap operations on the groups automatically to uncross the rats nest. The FSP enables you to optimize the swapping group process to achieve better rats nests. By swapping groups you can minimize the average rats nest crossings. The Swap group feature in the Design Connectivity, gains more significance for identical interfaces where all the groups are logically same. When using IP generated pin outs, make sure that the constraint optimization options are set appropriately while swapping groups.

Points to Remember Before Swap Groups

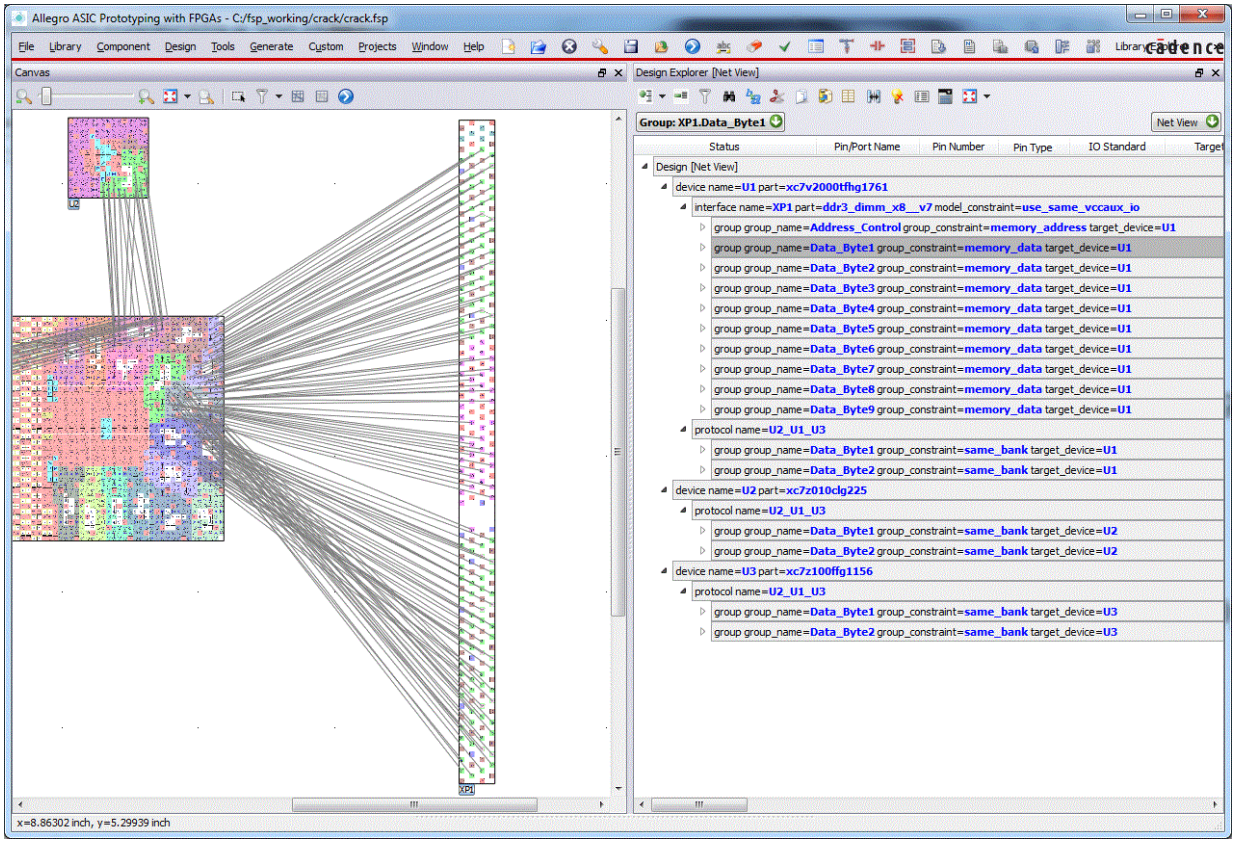
The following points you must remember before you start swapping groups:

- You are not allowed to manually swap interface groups when constrained optimization is not set.
- Irrespective of Constrained Optimization settings (On/Off) you are allowed to swap same logical groups (having Use Pin setting).

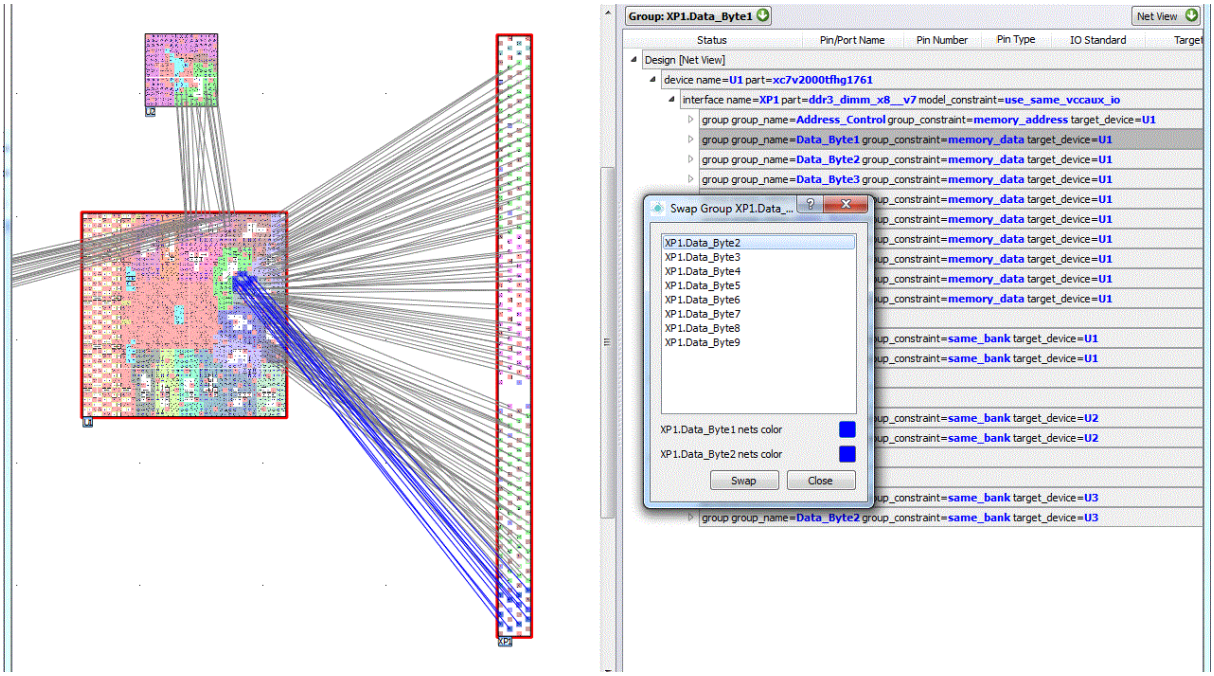
Swapping Groups Within an Interface

The following illustrates the steps to swap groups using an example.

1. Invoke the Design Connectivity.
The Design Connectivity is displayed.

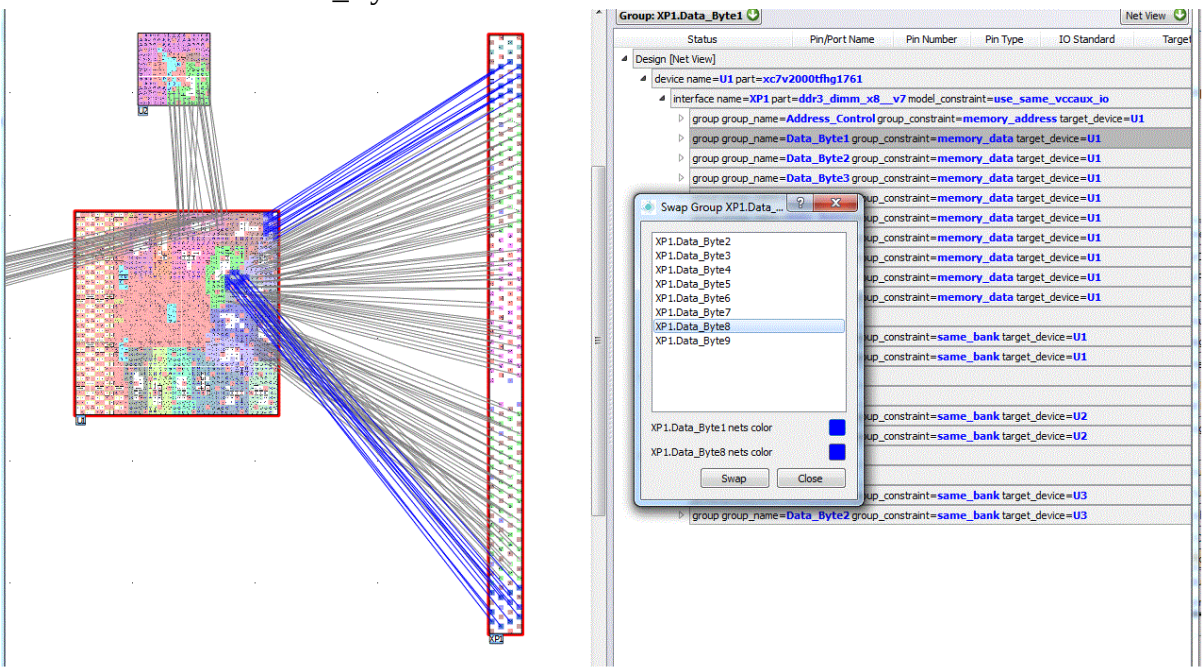


2. Right-click on the XP1.Data_Byte1 and choose Swap Groups.
The Swap Group <Inst_name><Group_name> dialog box is displayed. This dialog box lists all the names of the groups that are available in the selected interface.



Note: The selected group name, XP1.Data_Byte1 will not be listed in this list.

3. Click on the XP1.Data_Byte8 in the list.

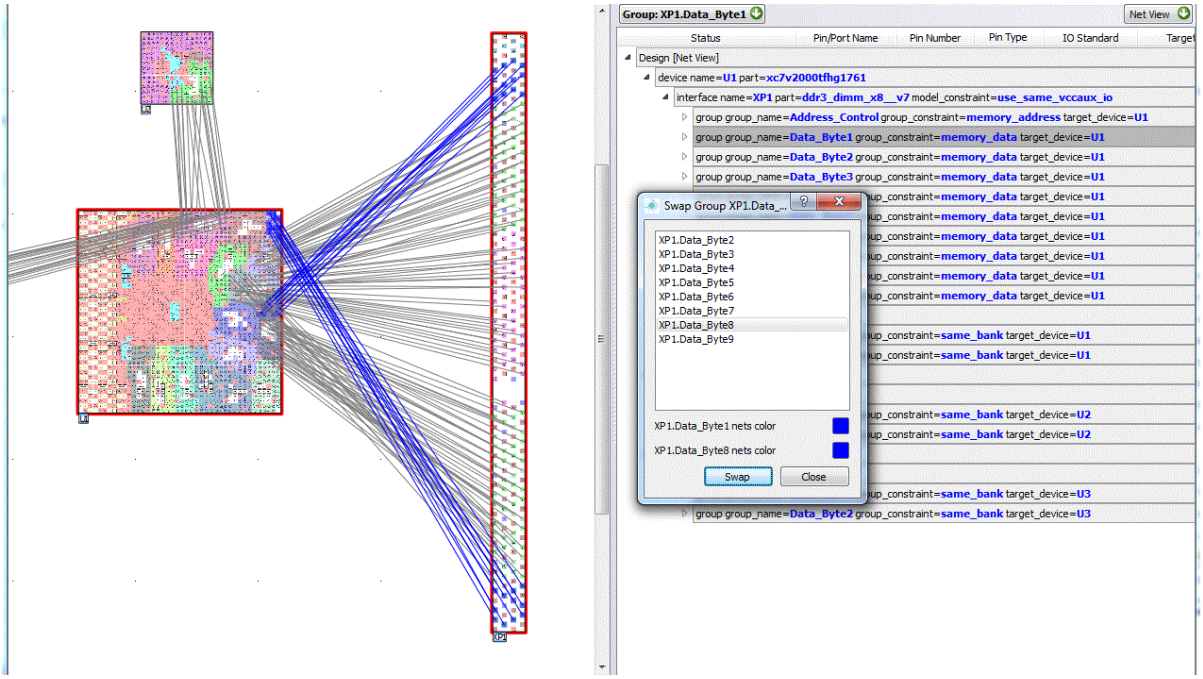


FSP displays the names of the selected groups, XP1.Data_Byte1 and XP1.Data_Byte1, at the bottom of the window as a confirmation.

4. Click Swap to swap groups.

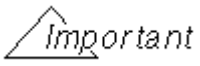
Note: After you click Swap, the Swap Group dialog box is continued to display. To close the dialog box click Close.

The two groups XP1.Data_Byte1 and XP1.Data_Byte8 are swapped.



Swapping Groups Between Two Interfaces

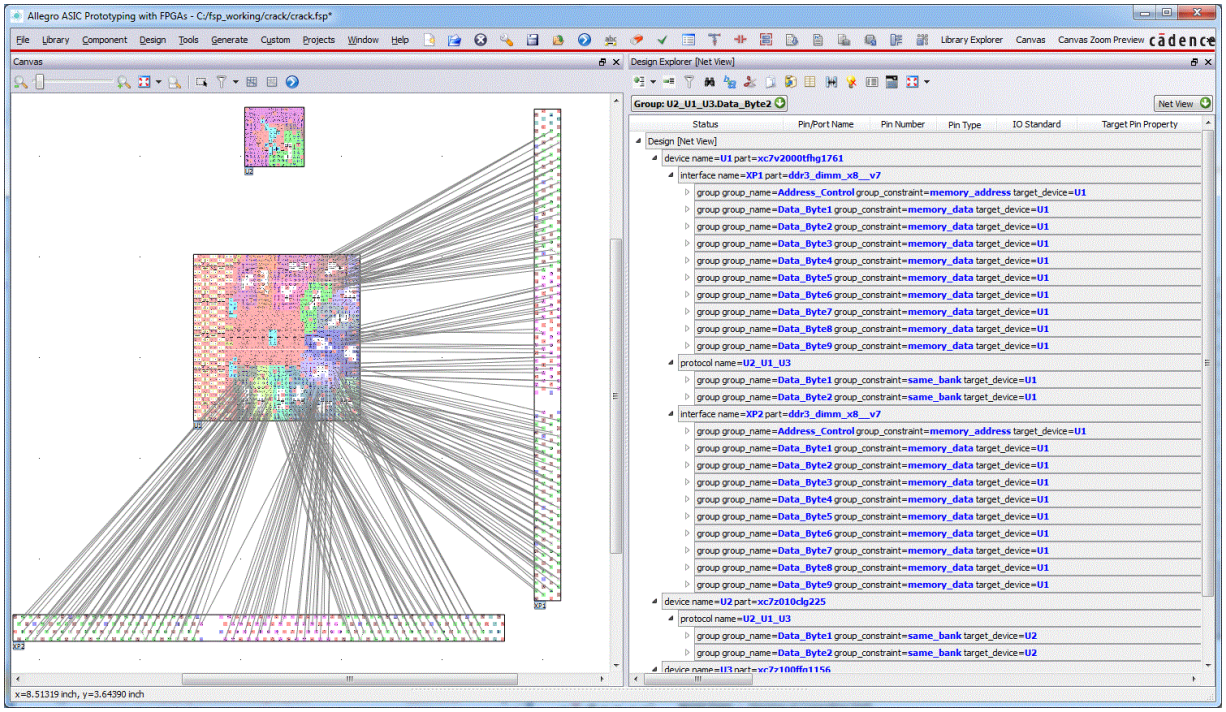
The following illustrates the steps to swap groups using an example.



You can swap the groups of two interfaces only when the two groups does not have any model constraints.

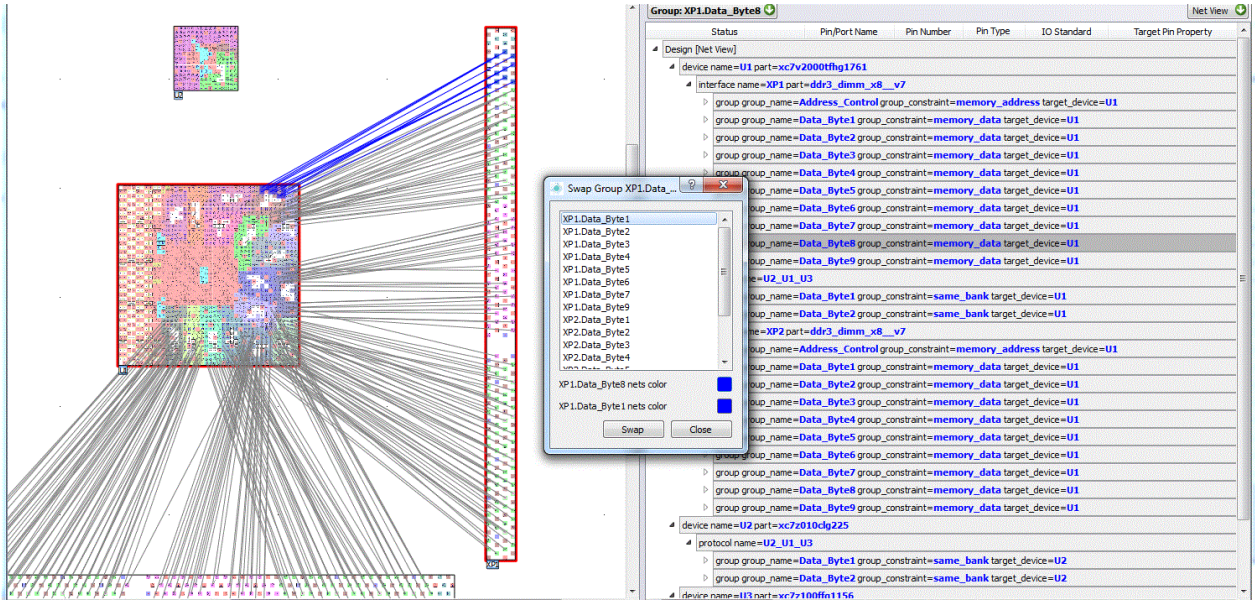
1. Invoke the Design Connectivity.

The Design Connectivity is displayed.

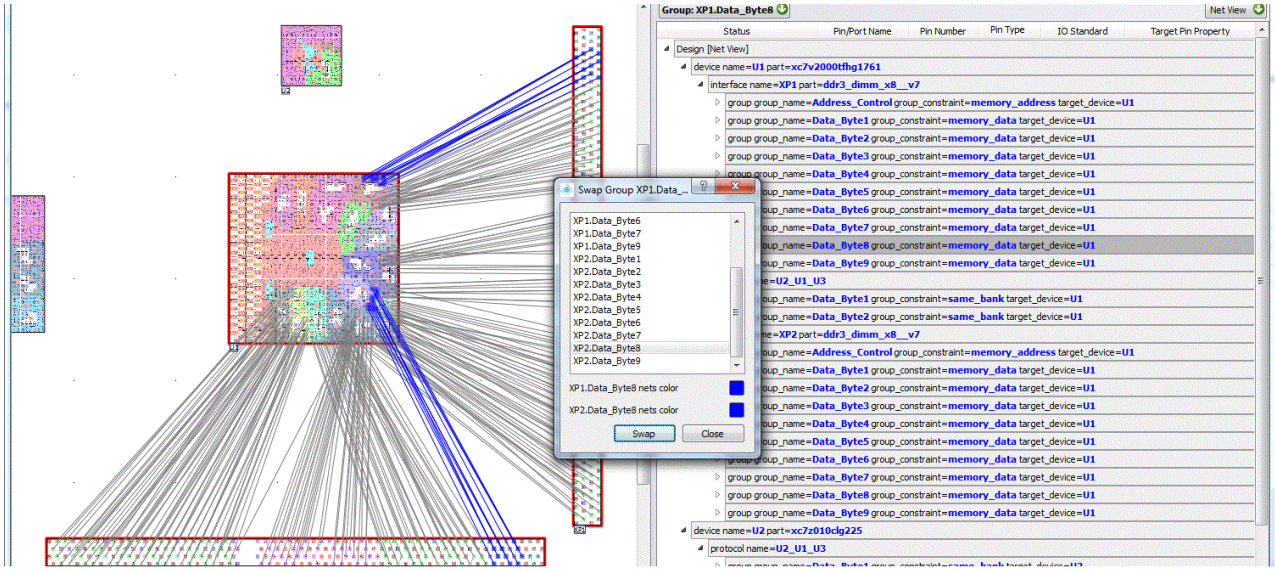


2. Right-click on the Data_Byte8 and choose Swap Groups.

The Swap Groups dialog box is displayed. The dialog box lists all the names of the groups of the two interfaces.



3. Click on the XP2.Data_Byte8 in the list.

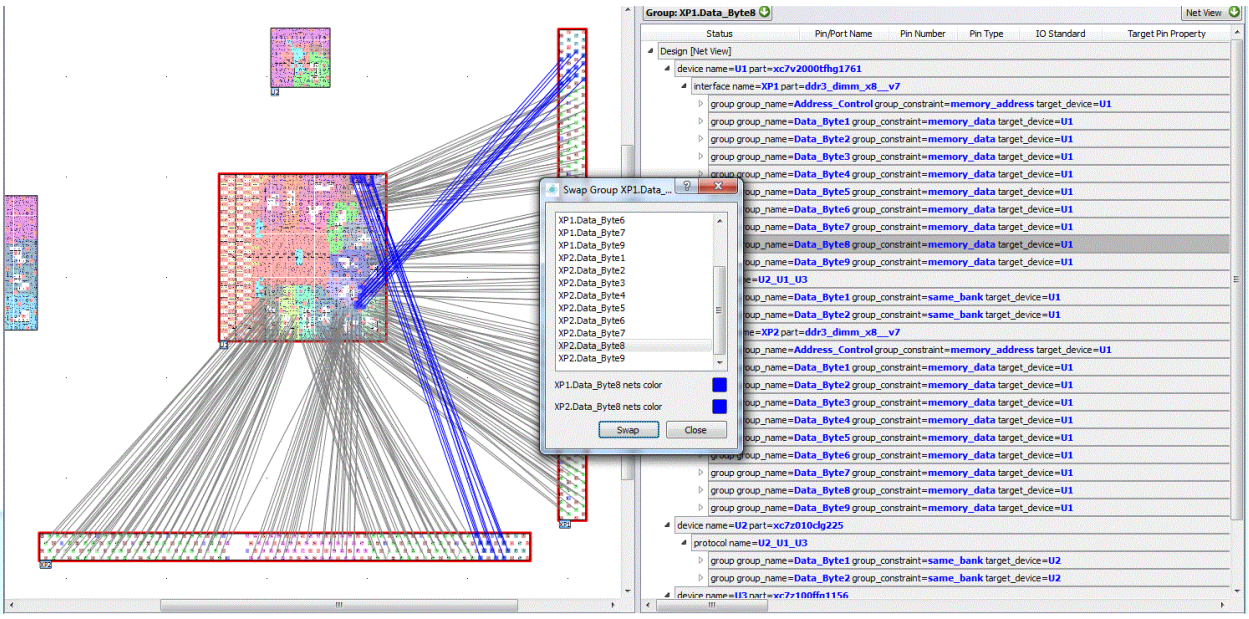


Note: Multi selection is not allowed in Swap Group pane.

4. Click Swap Group.

Note: After you click Swap, the Swap Group dialog box is continued to display. To close the dialog box click Close.

The two groups XP1.Data_Byte8 and XP2.Data_Byte8 are swapped.



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For support, see Cadence Online Support service.