Figure 2: Functional Timing for the wrreq Signal and the wrfull Signal

This figure shows the behavior for the `wrreq` and the `wrfull` signals.

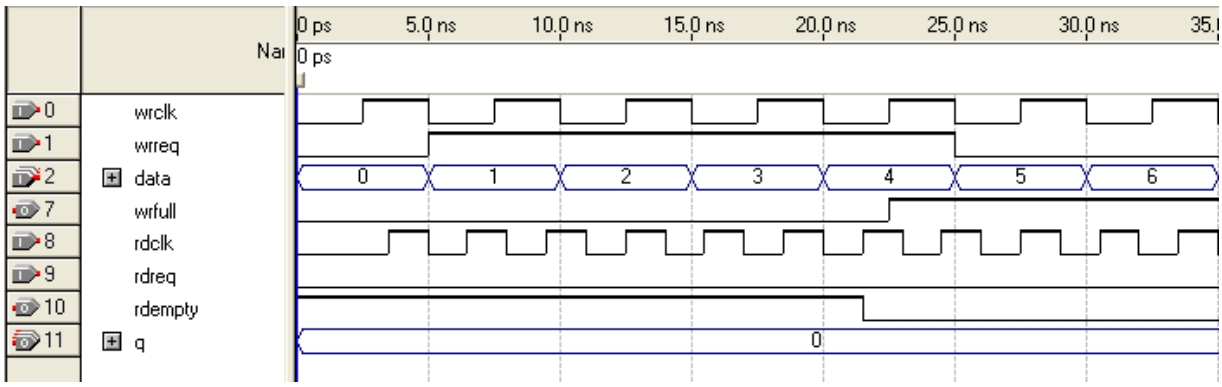
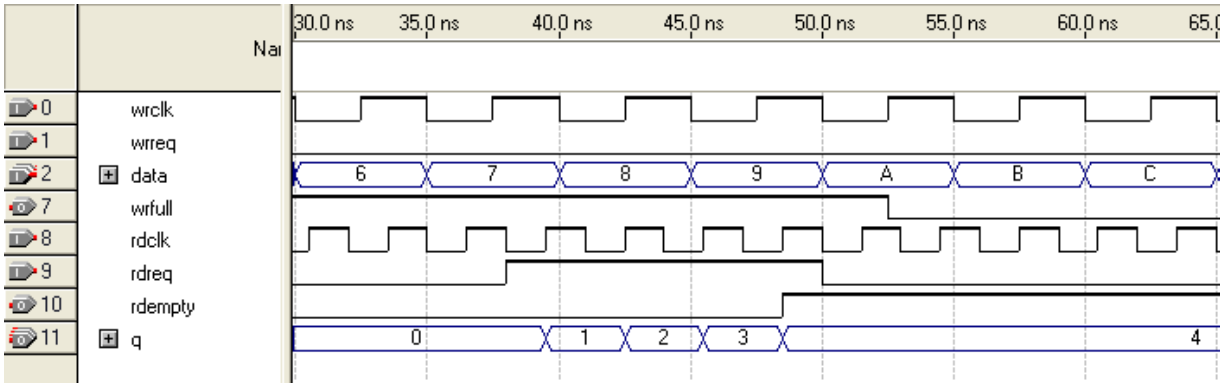


Figure 3: Functional Timing for the rdreq Signal and the rdempty Signal

This shows the behavior for the `rdreq` the `rdempty` signals.



The required functional timing for the DCFIFO as described previously is also applied to the SCFIFO. The difference between the two modes is that for the SCFIFO, the `wrreq` signal must meet the functional timing requirement based on the `full` signal and the `rdreq` signal must meet the functional timing requirement based on the `empty` signal.

SCFIFO ALMOST_EMPTY Functional Timing

In SCFIFO, the `almost_emtpy` is asserted only when the `usedw` is lesser than the `almost_empty_value` that you set. The `almost_empty` signal does not consider the data readiness at the output. When the `almost_empty_value` is set too low, it is possible to observe that SCFIFO asserts the `empty` signal without asserting the `almost_emtpy` signal.