RENESAS

R8C/Tiny Series

R8C/10, 11, 12, 13 Groups Serial Protocol Specification

1. Abstract

This specification defines the R8C/10, 11, 12, 13 groups serial protocol specification. The boot program stored in boot ROM area has the function to control Flash memory by communicating with a serial programmer when an MCU is shipped. A clock synchronous serial /UART mode can be selected for the communication.

2. Introduction

This specification defines the following items:

- Boot program
- Initial setting
- Control command
- Timing

Applicable products

- R8C/10, 11, 12, 13 Groups

3. Boot Program

When setting the MODE pin to “L” and driving the RESET pin “H”, a program in boot ROM area operates. This is called a boot program.

3.1 Operation Environment

The boot program operates with the high-speed on-chip oscillator included in the MCU in clock synchronous serial mode. **Execute sufficient evaluation in your system concerning the communication or reprogramming.**

3.2 Content in Boot Program

(1) Initial setting
(2) Initial communication with serial programmer
(3) Command control
Flash control command (programming, erasing and reading)
Various setting command (Read status, etc.)

3.3 Communication with Serial Programmer

Clock synchronous serial and UART modes can be selected for a communication with a serial programmer. Clock synchronous serial mode is a communication format with the RTS function. The transmit and receive is available by applying “L” to the MODE pin. The MODE pin is held “L” after executing all commands. UART mode is an asynchronous communication format. Figure 3.1 shows the Communication Format.
Also, the transfer data format is as follows:

Start bit	1 bit
Transfer data	8 bits
Parity bit	None
Stop bit	1 bit
Transfer format	LSB first

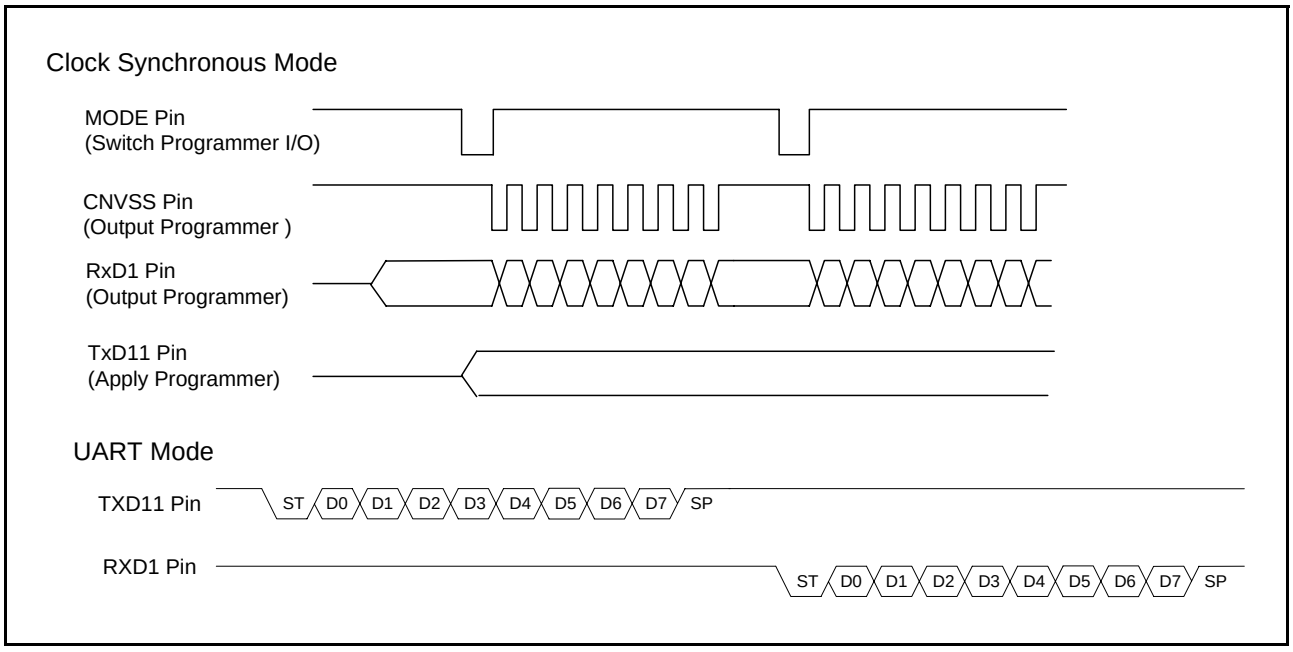

Figure 3.1 Communication Format

3.4 Used Pins

(1) MODE pin
This pin has a function as the RTS pin when selecting the clock synchronous serial.
(2) TxD11, RxD1 pins
These pins are the transmit and receive pins.
(3) CNVSS pin
This pin has a function as the CLK pin when selecting the clock synchronous serial.
(3) RESET pin
This pin controls RESET with a serial programmer
(4) Vcc, Vss pins
Output MCU Vcc and Vss levels for “H” or “L” output with the serial programmer.

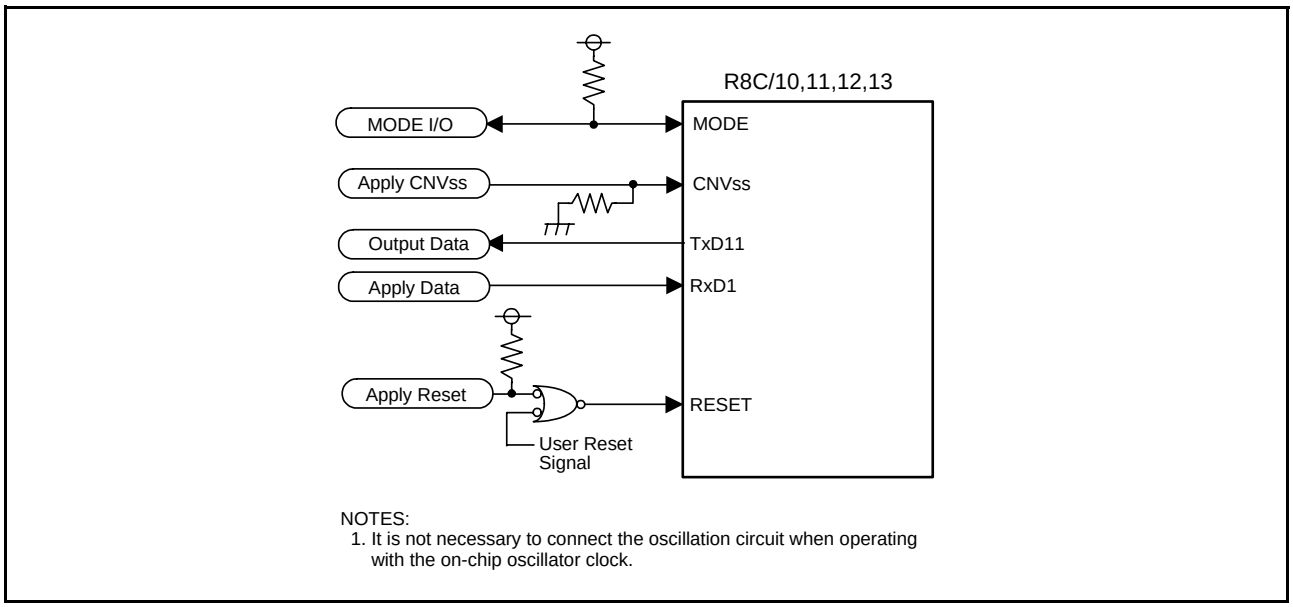

Figure 3.2 Connecting Example in Clock Synchronous Serial Mode

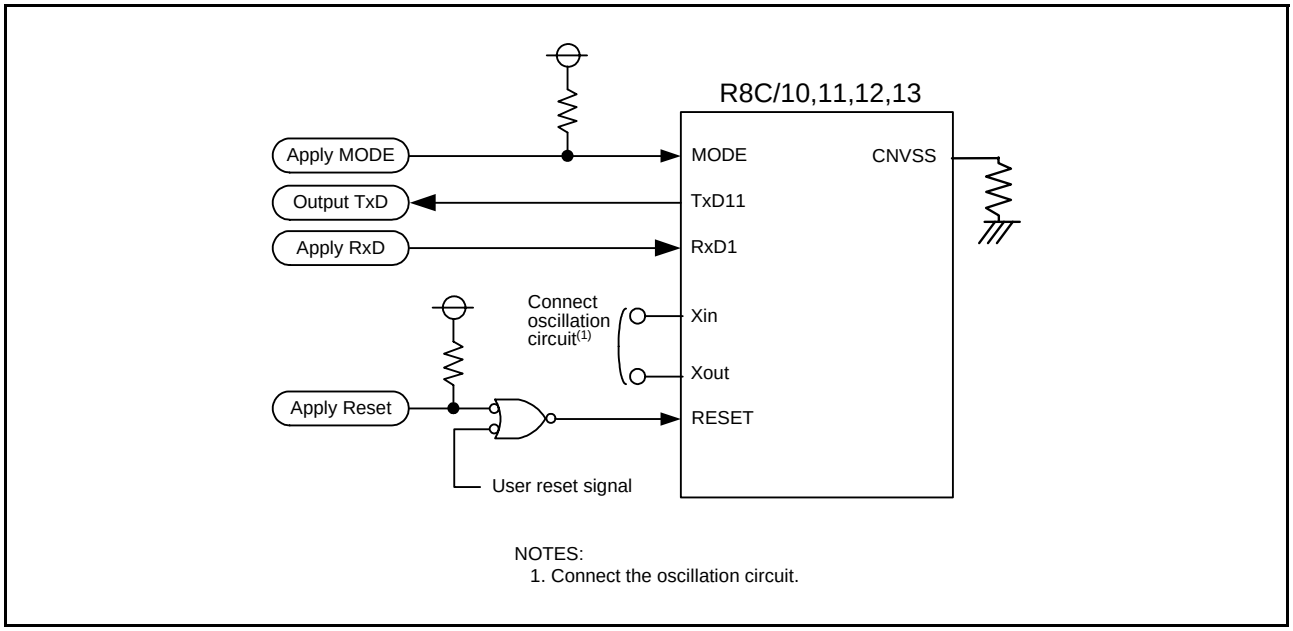

Figure 3.3 Connecting Example in UART Mode

4. Initial Setting

The following operations are performed in the initial setting of a boot program.
(1) Decide communication format
(2) Adjust bit rate (UART mode only)

4.1 Decide Communication Format

Decide clock synchronous serial mode or UART mode. Hold the pin levels on the Table 4.1 for Min. 15ms since the RESET pin is driven “H”. Figure 4.1 shows the Decided Timing of Communication Format for the timing diagram of clock synchronous serial mode.

Table 4.1 Pin Level in Mode Entry

MODE Pin	CNVSS Pin	RxD1 Pin	Mode
“L”	“L”	“L”	Clock synchronous
“L”	“L”	“H”	UART

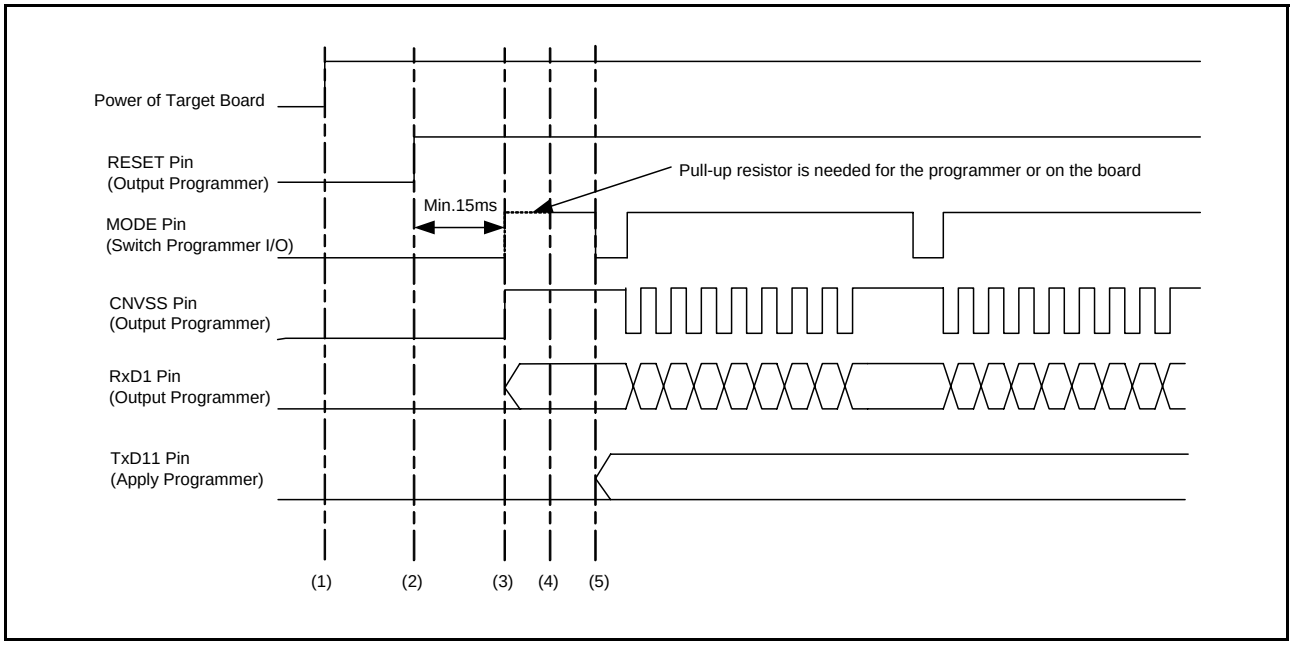

Figure 4.1 Decided Timing of Communication Format

(1) Set the power of the target board to ON.
(2) “L” is output to the MODE pin, “L” is output to the RxD1 pin, “L” is output to the CNVSS pin and “L” is output to the RESET pin. Then the RESET pin is driven “H”.
(3) After 15ms pass, “H” is output to the CNVSS pin and set the MODE pin to input.
(4) Change to serial mode.
(5) The serial transfer starts after checking that the MODE pin is held “L”.

4.2 Adjust Bit Rate (UART Mode Only)

The bit rate is adjusted to 9600bps by receiving the standard time command (00H) 16 times and the bit rate 9600 command (B0H) with 9600bps bit rate from the serial programmer. When receiving the bit rate 9600 command without any error, the bit rate 9600 command (B0H) is replied. Figure 4.2 shows the Bit Rate Adjustment Procedure.

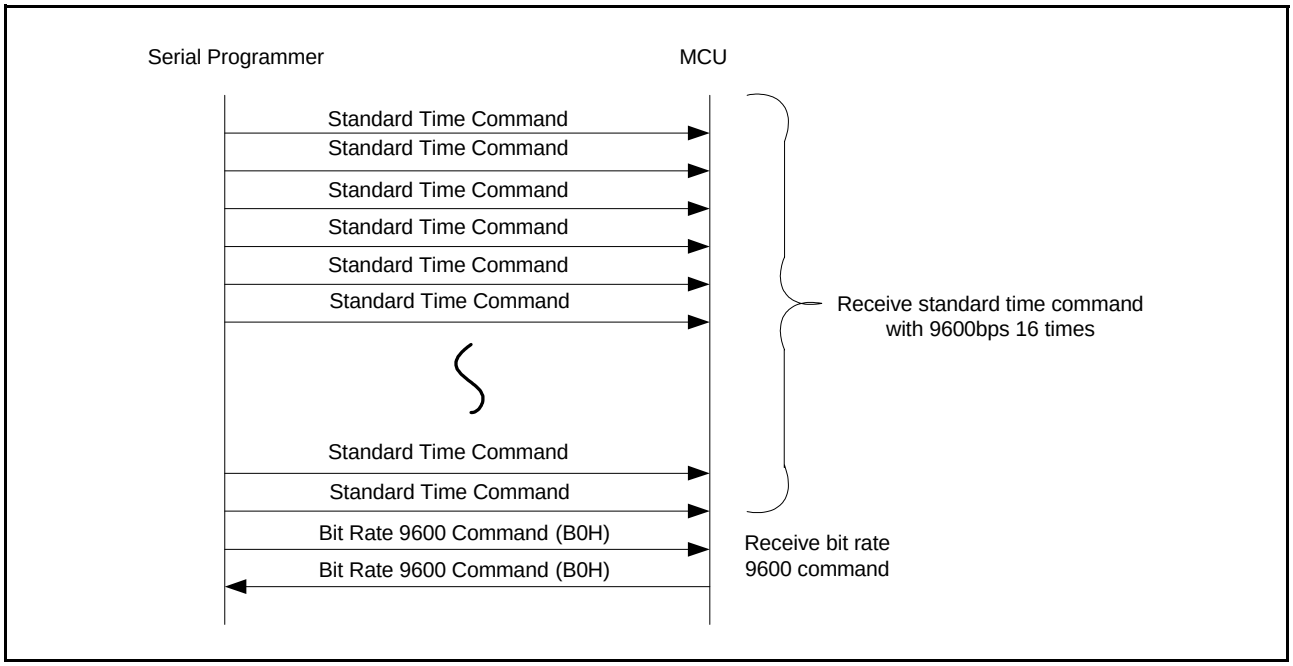

Figure 4.2 Bit Rate Adjustment Procedure

5. Command Specification

5.1 Control Commands

Table 5.1 lists the Control Commands.

Table 5.1 Control Commands

Control Command	1 byte	2 byte	3 byte	4 byte	5 byte	6 byte	7 byte or more	ID Unchecked
Page Read	FFH	Mid-order address	High-order address	**Data**	**Data**	**Data**	**Data**	Disable Acknowledgement
Page Program	41H	Mid-order address	High-order address	Data	Data	Data	Data	Disable Acknowledgement
Block Erase	20H	Mid-order address	High-order address	D0H				Disable Acknowledgement
Erase All Unlocked Block	A7H	D0H						Disable Acknowledgement
Read Status Register	70H	**SRD**	**SRD1**					Disable Acknowledgement
Clear Status Register	50H							Disable Acknowledgement
ID Checked Function	F5H	Low-order address	Mid-order address	High-order address	ID Size	ID1	Up to ID7	Enable Acknowledgement
Version Information Output Function	FBH	**Version**	**Version**	**Version**	**Version**	**Version**	**Version**	Enable Acknowledgement
Bit Rate 9600	B0H	**B0H**						Enable Acknowledgement
Bit Rate 19200	B1H	**B1H**						Enable Acknowledgement
Bit Rate 38400	B2H	**B2H**						Enable Acknowledgement
Bit Rate 57600	B3H	**B3H**						Enable Acknowledgement
Bit Rate 115200	B4H	**B4H**						Enable Acknowledgement
Standard Time Command	00H							Enable Acknowledgement

NOTES:
1. Shadings show the transmit from MCU to programmer, the rest shows the transmit from programmer to MCU.
2. SRD : Status register data, SRD1 : Status register data 1.
3. Blank products can acknowledge all commands.
4. The standard time data is transferred 16 times with an initial communication.
5. In the boot program, the numbers of the received data are not checked. Transmit neither too much nor too little data when transmitting commands.

6. Each Command

6.1 Page Read

6.1.1 Operation

The data in specified Flash memory area is read with 256-byte unit. Read area is specified by the high-order addresses (A16 to A23) and middle-order addresses (A8 to A15). 256 bytes of addresses xxxx00 to xxxxFFH are the target to read.

6.1.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 256th byte
	Command	Address		Data	Up to data
Programmer to MCU	FFH	Mid-order address	High-order address		
MCU to Programmer				Data0	Up to Data 255

NOTES:
1. Data 0 shows the data of the low-order address 00H and Data 255 shows the data of the low-order address FFH.

6.1.3 Procedure

(1) Transmit the page read command “FFH” at the 1st byte.
(2) Transmit the middle-order address at the 2nd-byte transfer and the high-order address at the 3rd-byte transfer.
(3) Receive the content in the low-order address 00H from the 4th byte by turns.

6.2 Page Program

6.2.1 Operation

The data is programmed into specified Flash memory area with 256-byte unit. Programmed area is specified by the high-order addresses (A16 to A23) and middle-order addresses (A8 to A15). 256 bytes of addresses xxxx00H to xxxxFFH are the target to read.

6.2.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 256th byte
	Command	Address		Data	Up to data
Programmer to MCU	41H	Mid-order address	High-order address	Data0	Up to Data 255
MCU to Programmer					

NOTES:
1. Data 0 shows the data of the low-order address 00H and Data 255 shows the data of the low-order address FFH.

6.2.3 Procedure

(1) Transmit the page program command “41H” at the 1st byte.
(2) Transmit the middle-order address at the 2nd-byte transfer and the high-order address at the 3rd-byte transfer.
(3) Transmit the programming data into the low-order address 00H from the 4th byte.

When the programming data is less than 256 bytes, transmit “FFH” for the shortage. Also, when the programming data is 257 bytes or more, the 257th byte is assumed as a command. When the programming error occurs during programming, the SR4 bit is set to “1” (program status ends with error).
Ensure the operating status of Flash memory by the read status register command after executing this command.

6.3 Block Erase

6.3.1 Operation

The specified Flash memory block is erased. Block area is specified by the high-order 8 bit (A16 to A23) and middle-order 8 bit (A8 to A15) in any address of the block to be erased.

6.3.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 256th byte
	Command	Block Address			
Programmer to MCU	20H	Mid-order address	High-order address	D0H	
MCU to Programmer					

6.3.3 Procedure

(1) Transmit the block erase command “20H” at the 1st byte.
(2) Transmit the middle-order address at the 2nd-byte transfer and the high-order address at the 3rd-byte transfer.
(3) Transmit the confirmation command “D0H” at the 4the byte.

Erasing to specified blocks starts after receiving the confirmation command “D0H”. Erasing sets the Flash content to “FFH”. When the programming error occurs during programming, the SR5 bit is set to “0” (erase status ends with error).
Ensure the operating status of Flash memory by the read status register command after executing this command.

6.4 Erase All Unlocked Blocks

6.4.1 Operation

The boot program erases all area (data area, program area) in the Flash memory.

6.4.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 256th byte
	Command				
Programmer to MCU	A7H	D0H			
MCU to Programmer					

6.4.3 Procedure

(1) Transmit the erase all unlocked block command “A7H” at the 1st byte.
(2) Transmit the confirmation command “D0H” at the 2nd-byte transfer.

Erasing to all blocks start after receiving the confirmation command “D0H”. Erasing sets the Flash content to “FFH”. When the programming error occurs during programming, the SR5 bit is set to “1” (erase status ends with error).
Ensure the operating status of Flash memory by the read status register command after executing this command.

6.5 Read Status Register

6.5.1 Operation

This register checks the operating status of Flash memory.

6.5.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 256th byte
	Command	SRD			
Programmer to MCU	70H				
MCU to Programmer		Output SRD	Output SRD1		

6.5.3 Procedure

(1) Transmit the read status register command “70H” at the 1st byte.
(2) Receive SRD at the 2nd-byte transfer.
(3) Receive SRD1 at the 3rd-byte transfer.

6.5.4 SRD Register

Each bit of SRD	Status Name	Definition	
		“1”	“0”
SR7 (bit7)	Sequencer status	Ready	Busy
SR6 (bit6)	Reserved		
SR5 (bit5)	Erase status	Error ends	Normal end
SR4 (bit4)	Program status	Error ends	Normal end
SR3 (bit3)	Reserved		
SR2 (bit2)	Reserved		
SR1 (bit1)	Reserved		
SR0 (bit0)	Reserved		

(1) Sequencer status
The sequencer status shows the operating status of Flash memory. This bit is set to “0” (busy) during auto-programming or auto-erasing. This bit is set to “1” (ready) when auto-programming or auto-erasing ends.
(2) Erase status
The erase status shows the erase operating status. When an error occurs, this bit is set to “1”. This bit is set to “0” when executing the clear status register command.
(3) Program status
The program status shows the programming status. When an error occurs, this bit is set to “1”. This bit is set to “0” when executing the clear status register command.

Both the SR5 and SR4 bits are set to “1” in the following cases:
- When the defined command is not applied accurately
- When the data other than D0H or FFH is applied in the cycle that the block erase confirmation command is applied. The command is canceled by applying FFH and the MCU enters read array mode.

(4) Reserved bit
When reading, its content is indeterminate.

6.5.5 SRD1 Register

Each Bit of SRD1	Status Name	Definition	
		"1"	"0"
SR15 (bit7)	Reserved		
SR14 (bit6)	Reserved		
SR13 (bit5)	Reserved		
SR12 (bit4)	Reserved		
SR11 (bit3)	ID checked bit	00 : Not checked 01 : Check not matched 10 : Reserved 11 : Checked	
SR10 (bit2)			
SR9 (bit1)	Reserved		
SR8 (bit0)	Reserved		

(1) ID checked bit
This bit shows the ID checked result.
(2) Reserved bit
When reading, its content is indeterminate.

6.6 Clear Status Register

6.6.1 Operation

This command initializes the status register. Initialize the status register with this command before erasing or page-programming to the Flash memory.

6.6.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 256th byte
	Command				
Programmer to MCU	50H				
MCU to Programmer					

6.6.3 Procedure

(1) Transmit the clear status command “50H” at the 1st byte.

6.7 ID Check Function

6.7.1 Operation

This command checks an ID stored in the Flash memory and an ID transmitted from a serial programmer. Some commands are not acknowledged if the ID stored in the Flash memory and the ID transmitted from the serial programmer do not match in the ID check function.

6.7.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	5th byte	6th byte	Up to 12th byte
	Command	Address			ID size	ID	ID
Programmer to MCU	F5H	DFH	FFH	00H	07H	ID1	Up to ID7
MCU to Programmer							

NOTES:
1. DFH, FFH and 00H are the addresses in which the ID1 is stored.

6.7.3 Procedure

(1) Transmit the ID check function command “F5H” at the 1st byte.
(2) Transmit the low-order address at the 2nd byte, middle-order address at the 3rd byte and the high-order address at the 4th byte in which the ID1 is stored.
(3) Transmit the ID number of pcs (07H) at the 5th byte.
(4) Transmit the ID at the 6th byte or above.

After transmit, the transmitted result is reflected to the SR10 and SR11. The ID stored in Flash memory and the ID transmitted with the serial programmer are recognized as mismatch when the transmit addresses do not match with ID addresses or the ID size is not 7.

6.8 Version Information Output Function

6.8.1 Operation

This command checks the boot program version.

6.8.2 Packet

	1st byte	2nd byte	3rd byte	4th byte	Up to 9th byte
	Command				
Programmer to MCU	FBH				
MCU to Programmer		‘V’	‘E’	‘R’	X

NOTES:
1. Transmit version information from ‘V’ as “VER.X.XX” (X; numbers) with 8 characters of ASCII code.

6.8.3 Procedure

(1) Transmit the command “FBH” of the version information output function at the 1st byte.
(2) Receive version information from the 2nd byte to 9th byte with ASCII characters.

6.9 Bit Rate 9600

6.9.1 Operation

Change the bit rate to 9600bps.

6.9.2 Packet

	1st byte	2nd byte
	Command	
Programmer to MCU	B0H	
MCU to Programmer		B0H

6.9.3 Procedure

(1) Transmit the command “B0H” of the bit rate 9600 at the 1st byte.
(2) Receive the confirmation command “B0H” at the 2nd byte.
(3) Set to 9600bps after receiving the confirmation command.

6.10 Bit Rate 19200

6.10.1 Operation

Change the bit rate to 19200bps.

6.10.2 Packet

	1st byte	2nd byte
	Command	
Programmer to MCU	B1H	
MCU to Programmer		B1H

6.10.3 Procedure

(1) Transmit the command “B1H” of the bit rate 19200 at the 1st byte.
(2) Receive the confirmation command “B1H” at the 2nd byte.
(3) Set to 19200bps after receiving the confirmation command.

6.11 Bit Rate 38400

6.11.1 Operation

Change the bit rate to 38400bps.

6.11.2 Packet

	1st byte	2nd byte
	Command	
Programmer to MCU	B2H	
MCU to Programmer		B2H

6.11.3 Procedure

(1) Transmit the command “B2H” of the bit rate 38400 at the 1st byte.
(2) Receive the confirmation command “B2H” at the 2nd byte.
(3) Set to 38400bps after receiving the confirmation command.

6.12 Bit Rate 57600

6.12.1 Operation

Change the bit rate to 57600bps.

6.12.2 Packet

	1st byte	2nd byte
	Command	
Programmer to MCU	B3H	
MCU to Programmer		B3H

6.12.3 Procedure

(1) Transmit the command “B3H” of the bit rate 57600 at the 1st byte.
(2) Receive the confirmation command “B3H” at the 2nd byte.
(3) Set to 57600bps after receiving the confirmation command.

6.13 Bit Rate 115200

6.13.1 Operation

Change the bit rate to 115200bps.

6.13.2 Packet

	1st byte	2nd byte
	Command	
Programmer to MCU	B4H	
MCU to Programmer		B4H

6.13.3 Procedure

(1) Transmit the command “B4H” of the bit rate 115200 at the 1st byte.
(2) Receive the confirmation command “B4H” at the 2nd byte.
(3) Set to 115200bps after receiving the confirmation command.

7. Timing

7.1 Byte Transfer Time (Clock Synchronous Mode Only)

End the data transmit within 300µs since the MODE pin is held “L”. When 300ms pass, the program judges the serial transmit and receive as an error and the command waiting state is held after “H” is applied to the MODE pin for 300µs.

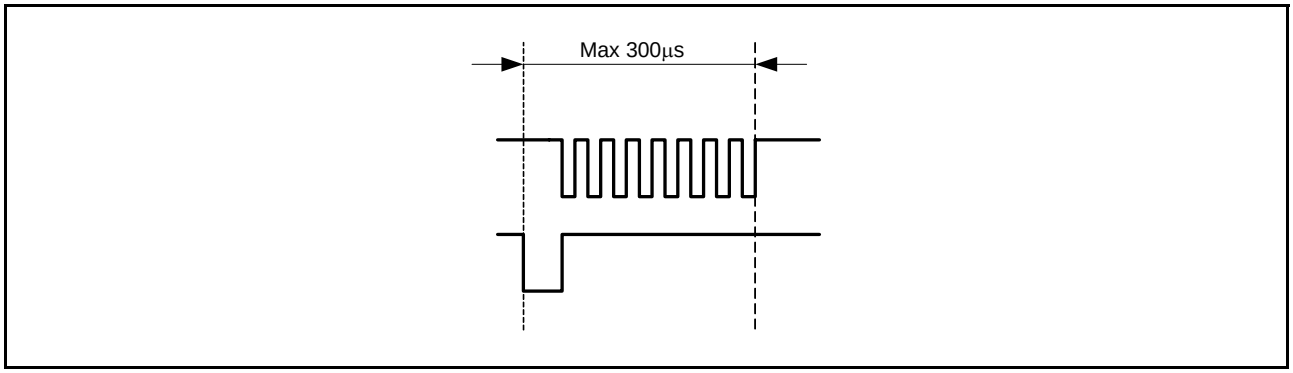

Figure 7.1 Byte Transfer Time

7.2 Data Transmit Interval (Between Byte and Byte)

7.2.1 Clock Synchronous Serial Mode

The MODE pin outputs “L” within 1.2ms to the following data receive prepared from the receive completion.

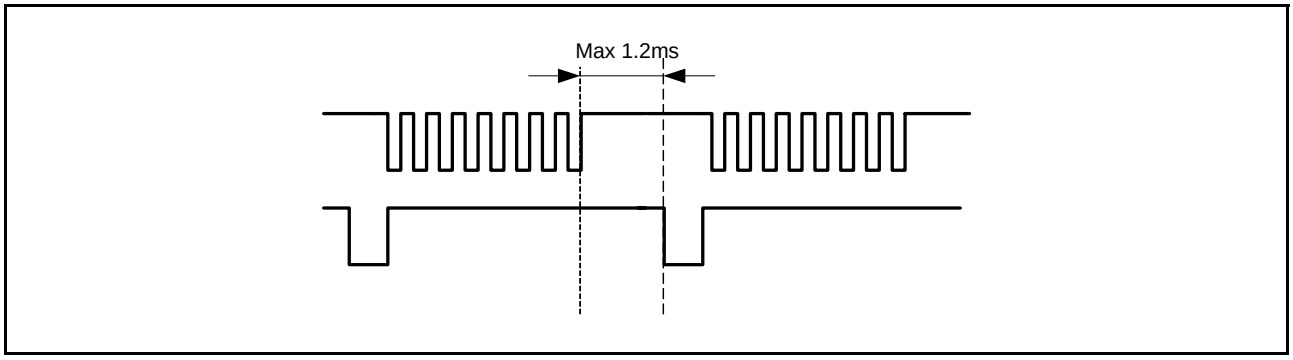

Figure 7.2 Data Transmit Interval of Clock Synchronous Serial Mode

7.2.2 UART Mode

Set Min.20ms at the standard time command transmit and Min. 50µs at the control command transmit, which are necessary for the receive process time in the boot program.

7.3 Command Receive Mode (Clock Synchronous Mode Only)

Judge the mode as the command receive mode if the MODE pin is not held “L” for 1.2ms.

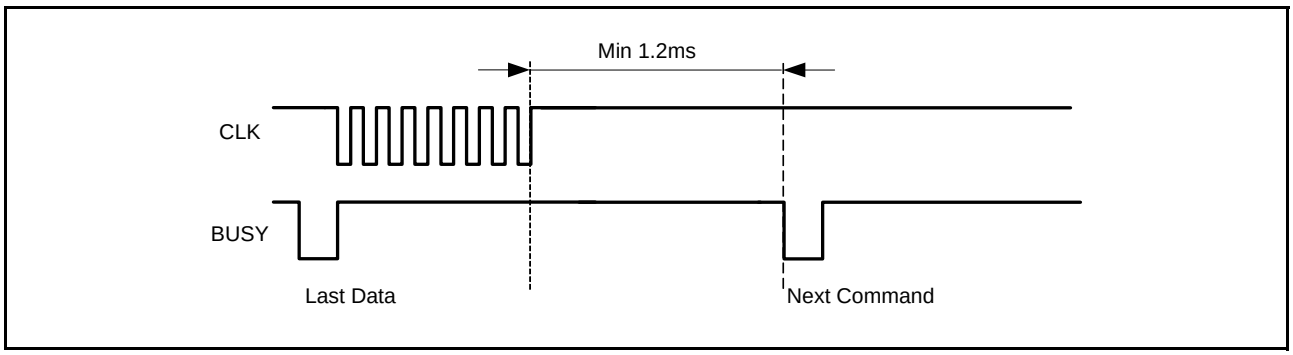

Figure 7.3 Command Receive Mode

7.4 Read Status Register Command

After transmitting the page program, block erase, erase all unlocked block commands, consider the programming time and erasing time and transmit the read status register command

REVISION HISTORY	R8C/Tiny Series R8C/10, 11, 12, 13 Groups Serial Protocol Specification

Rev.	Date	Description	
		Page	Summary
1.00	Jul 12, 2005	–	First Edition issued

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