Cadence Allegro and OrCAD: What's New in 17.2-2016 QIR 1 (HotFix 004)

This document describes the new features and enhancements in Cadence® Allegro® and OrCAD® products in 17.2-2016 Quarterly Incremental Release (QIR) 1. The products covered are:

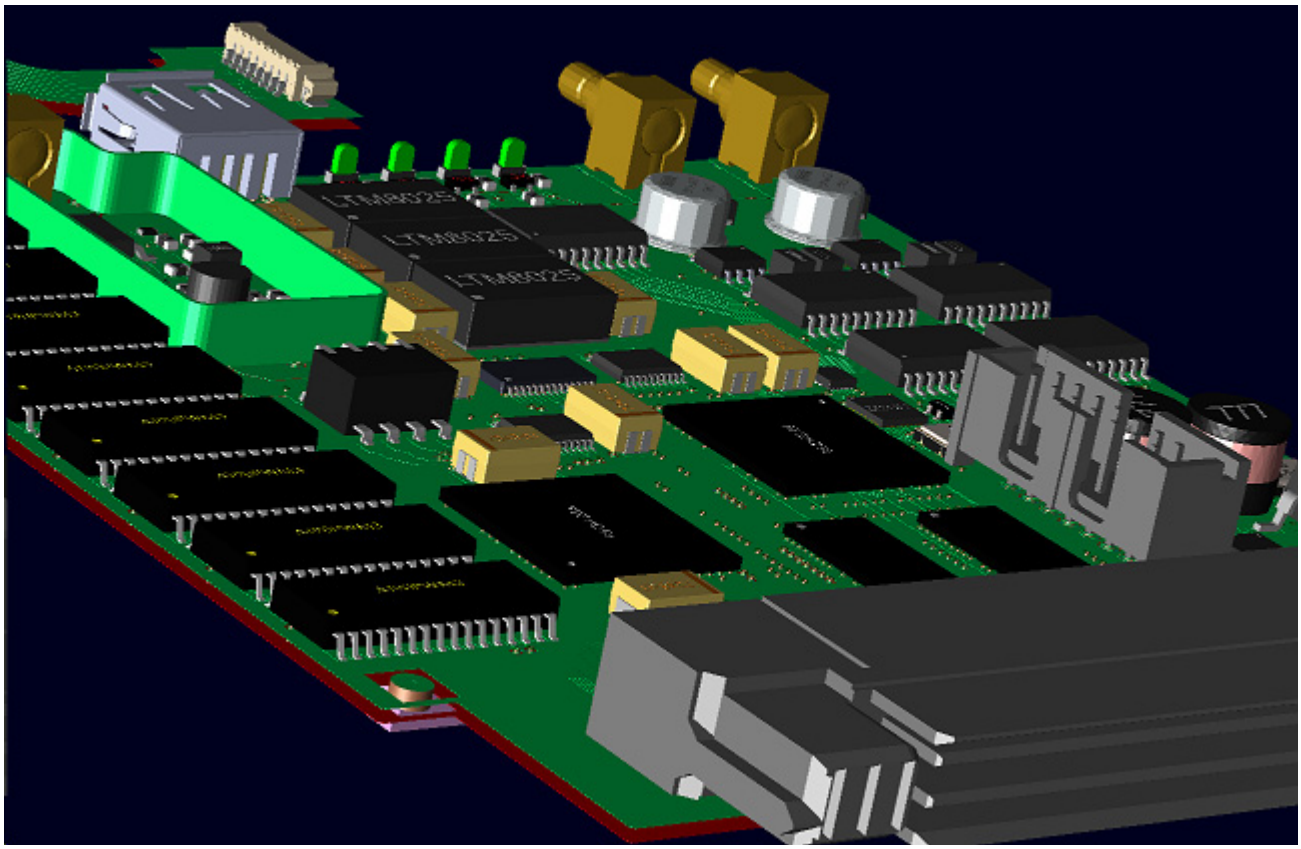
- Allegro PCB Editor
- Cadence SiP Layout and Allegro Package Designer (APD)
- OrCAD Capture
- OrCAD Capture CIS
- PSpice
- Allegro Sigrity PI

Allegro PCB Editor

This section describes the new features and enhancements in Allegro® PCB Editor 17.2-2016 QIR 1.

New 3D Canvas (Unsupported Prototype)

This is the first phase of major 3D improvements planned for PCB Editor. This release includes a graphics engine upgrade which brings higher quality visualization and speed when panning and zooming. Other features available in the 3D canvas include collision detection, etch layer visibility controls, and cross probing to the 2D canvas.



Getting Started

Out of the box, the original *3D Viewer* is still the default viewer. The new *3D Canvas* is available as an unsupported prototype feature that requires you to enable the environment variable `interactive_3d_canvas` found in *Setup – User Preferences – Unsupported*.

Once you set the variable, click the 3D toolbar icon or choose *View – 3D View*. Invoking 3D using either of these two methods results in the entire 2D PCB being transformed onto the 3D Canvas. Once invoked, a progress bar indicator appears, which might take time depending on the size of your design.

3D Canvas Navigation

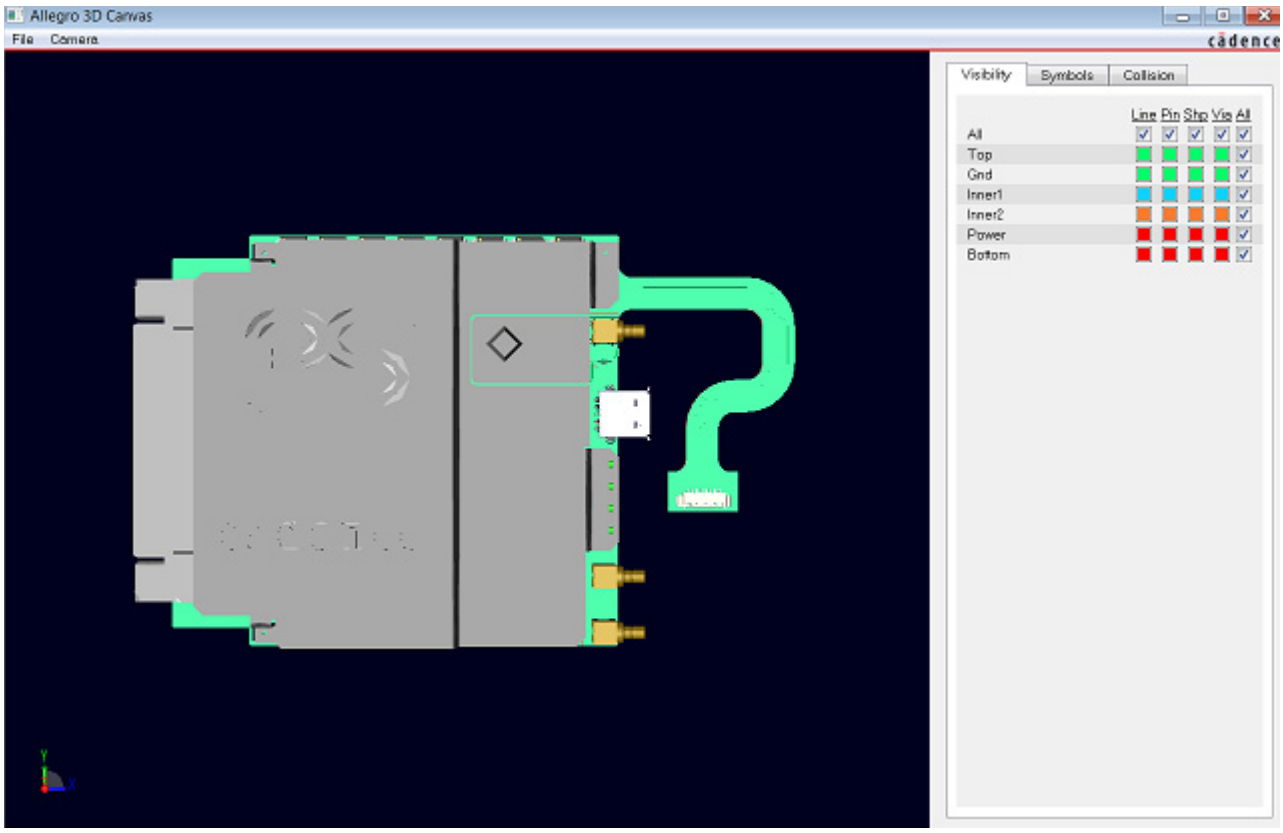
Movement around the canvas can be performed by using the following methods:

- Mouse wheel to zoom in and out
- Right-click and hold to grab canvas and pan in desired direction
- Right-click+SHIFT to rotate canvas in any direction

3D Canvas Controls

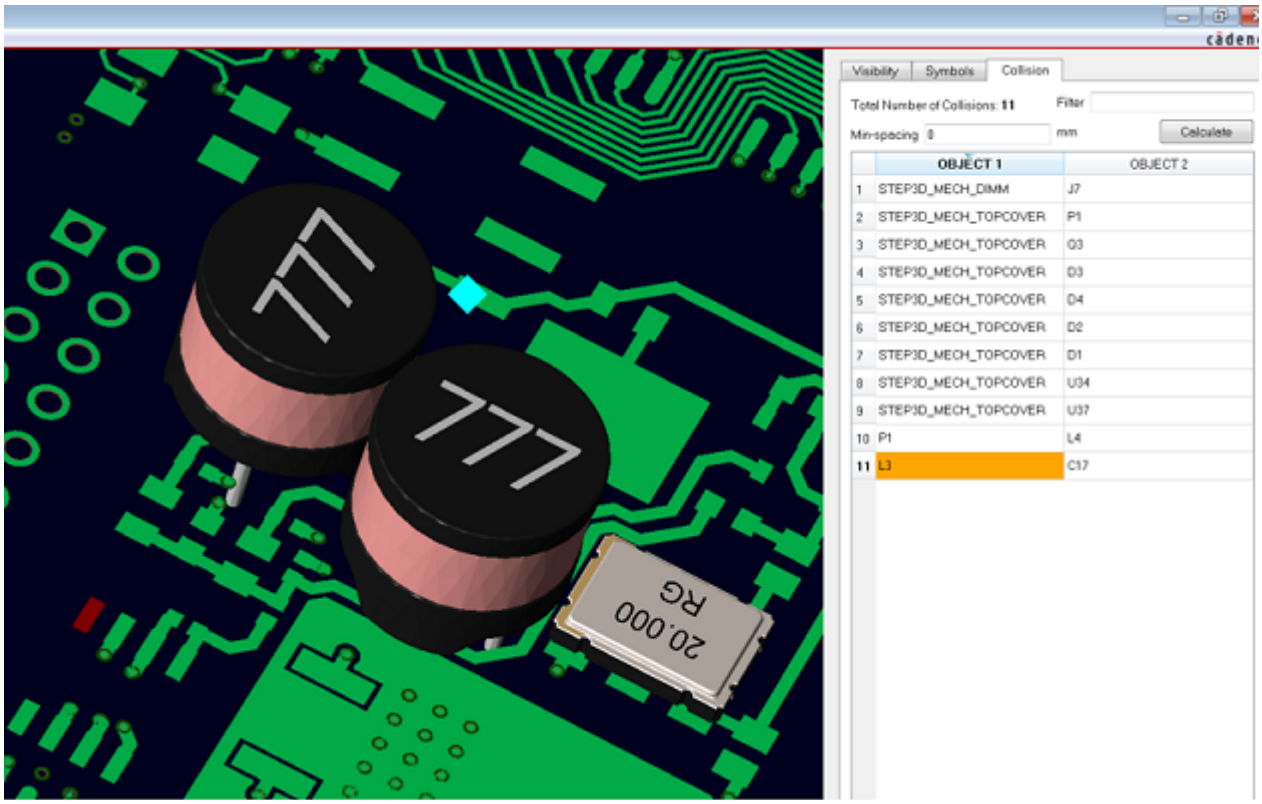
The new *3D Canvas* is supported by three option panes on the right side of the display.

- Visibility – controls the Line, Pin, Shape, and Via visibility of etch layers.
- Symbols – controls the Step Model or Placebound visibility for Top, Bottom, or Embedded Component layers.
- Collision – checks for overlap between symbols.



Basic Collision Detection

Overlapping symbols are reported in the *Collision* pane as shown in the following image. Select an object cell, right-click, and choose *Locate*. This results in the blue locator graphic near the symbol. The symbol also blinks a few times.



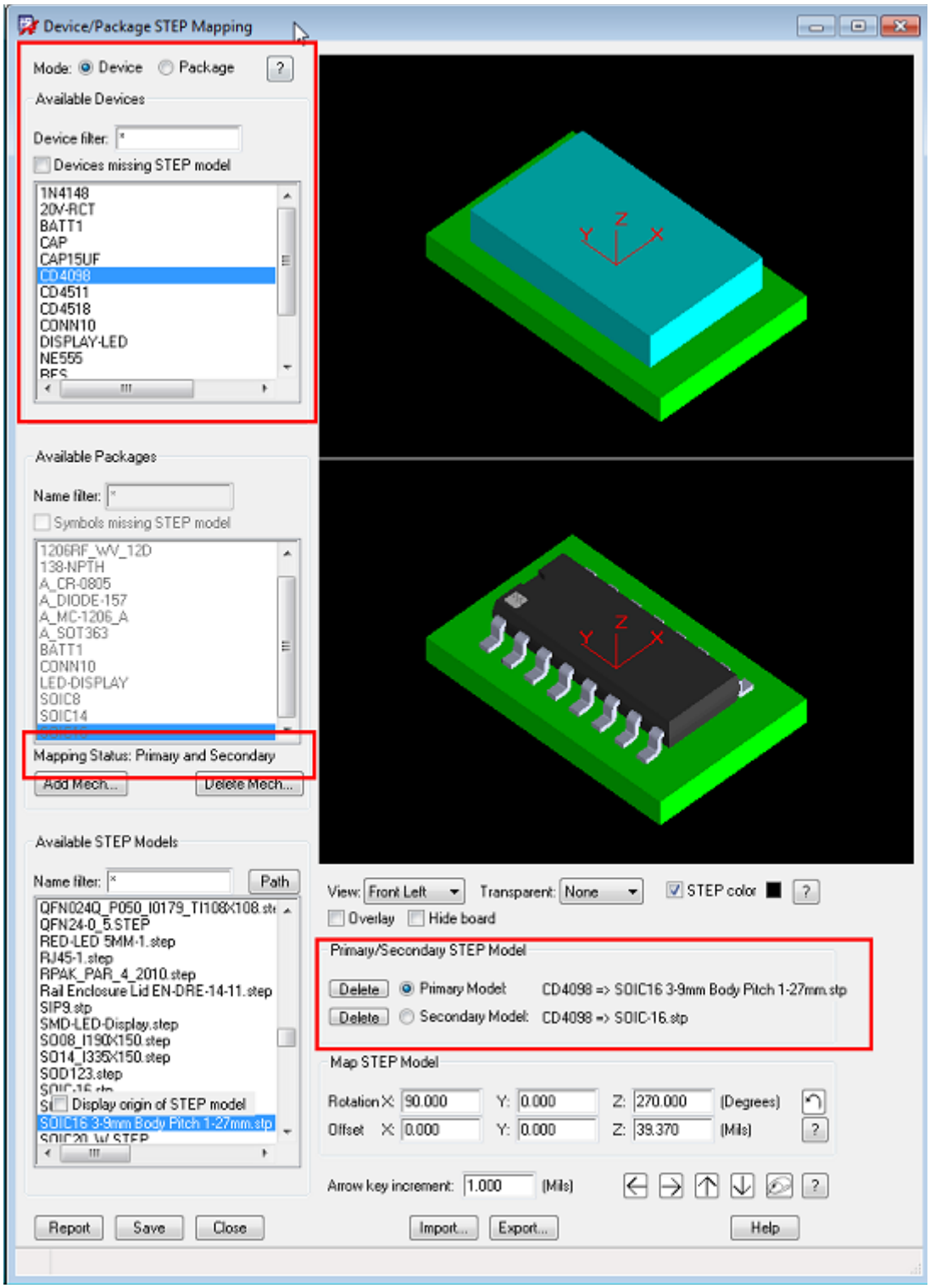
STEP Model Mapping to Devices

The STEP Mapper user interface is enhanced to support the mapping of a STEP model to a device as well as the package symbol.

Summary of STEP Mapping UI Changes:

- New Mapping Mode: Device or Package.
- New information button “?” for the mapping mode.
- New pane for current devices in design.

- New mapping status for package (Primary or Secondary)



New environment variables, `step_mapping_path`, and `step_facet_path` need to be set up using the menu *Setup – User Preferences – Path – Library* to support STEP mapping file import.

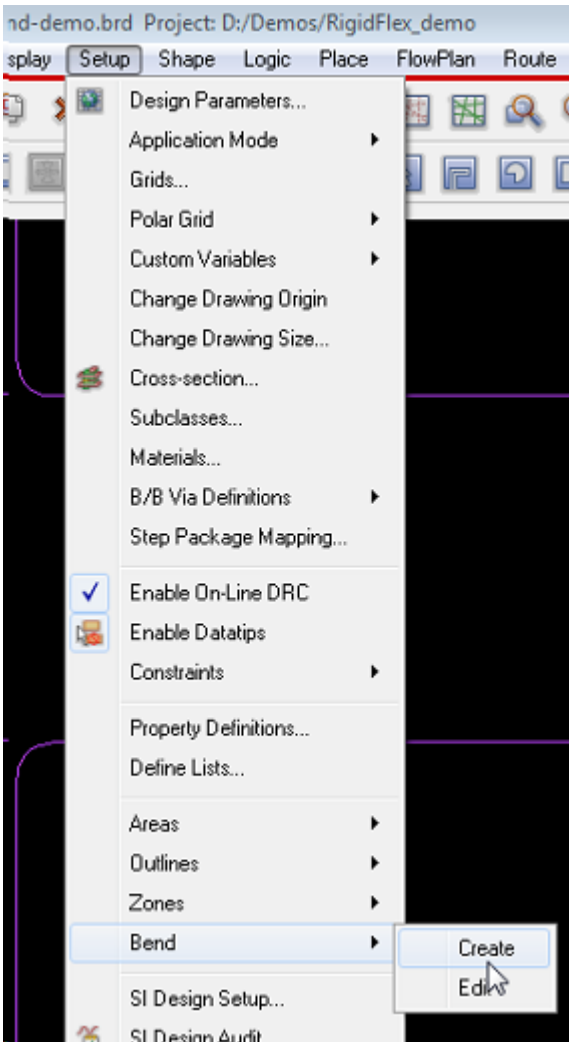
- `step_mapping_path` - Searches path for mapping files during logic import.
- `step_facet_path` - Searches path for STEP facet files during importing STEP mapping files.
- `steppath` (old) - Searches path for STEP files during STEP mapping process.

Bend Editor for Flex Design Applications

One of the general characteristics of a flex or a rigid/flex design, is to permit the design to bend. A bend is defined by the radius, angle, and direction of the bend. This release introduces a *Bend Editor* where you can define a bend line that represents the center of a bend zone arc. The bend line parameters assign attributes that are attached as a property to the bend line. Once the line is defined, a bend area is created that visually displays the extents of the bend based on the bend values. There is also an option to add via keepout and package keepout geometries relative to the bend area's outline geometry.

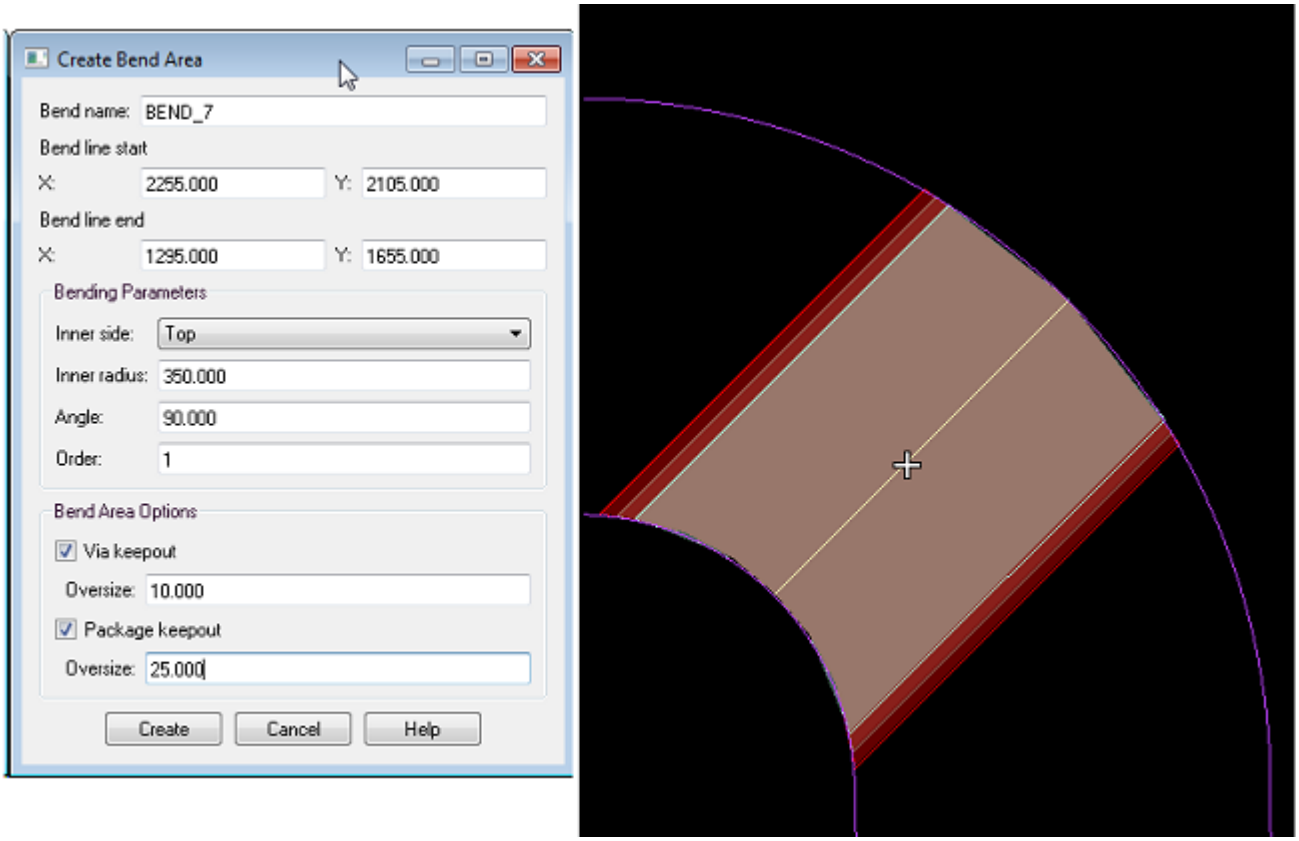
Creating a Bend Definition

From the PCB Editor menu, select *Setup – Bend – Create*.



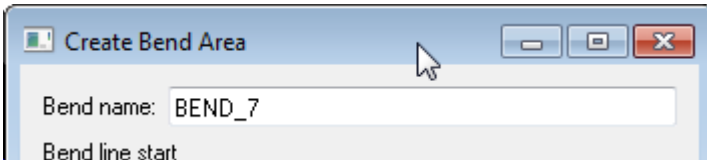
The *Create Bend Area* dialog box appears. The first step is to enter a unique name for the bend area. Use the dialog box to manually enter the start and end points of the bend line, if known, or add them through manual picks in the PCB Editor. The bend line is added to the RIGID FLEX/BEND_LINE subclass. You can specify the bend parameter information that includes bend direction, radius, angle, and bend order. Options for via and package keepouts are selected by default. When you click *Create*, the bend area (added to the RIGID FLEX/BEND_AREA subclass), optional keepouts, and bend line properties are created.

The bend line, bend area shape, via, and package keepout (if selected) geometries are combined into a single group. The group name is defined by the bend area name set in the *Create Bend Area* dialog box.



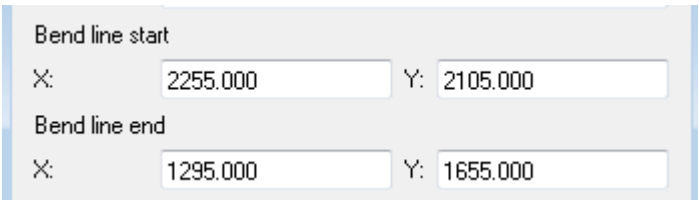
The *Create Bend Area* dialog box fields values are:

- Bend name: The bend area requires an ID or name. Each name must be unique, duplicate bend area names are not allowed. This name is referenced when exporting and importing IDX files for ECAD/MCAD collaboration.

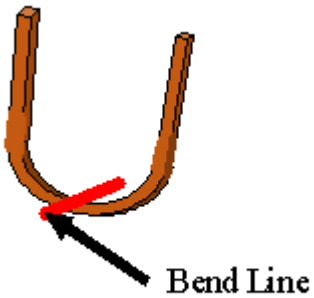


- Bend line start: The X:Y location of the start point of the bend line may be entered in these fields if the value is known. A mouse pick may be used to define the bend line start point. The X:Y values are populated based on the first pick that defines the bend line start point.

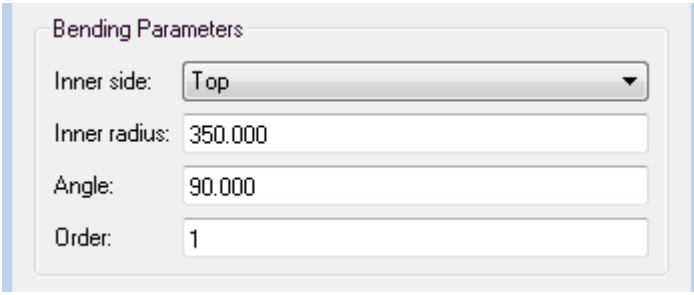
- Bend line end: The X:Y location of the end point of the bend line may be entered in these fields if the value is known. A mouse pick may be used to define the bend line end point. The X:Y values are populated based on the second pick that defines the bend line end point.



Note: The bend line defines the center of the bend along the bend radius as shown in the following image.

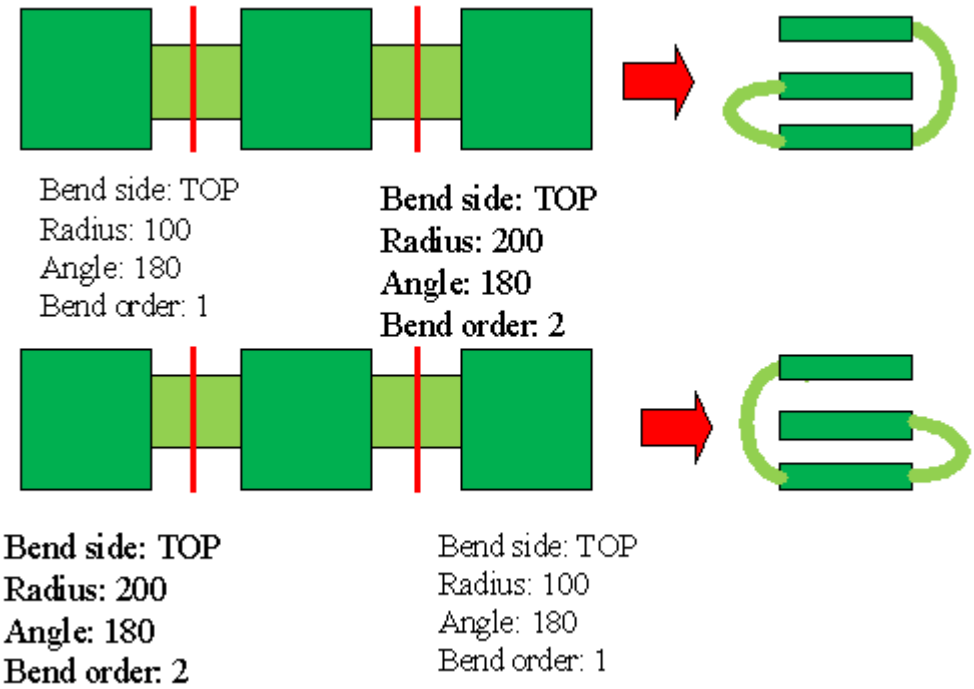


Bending Parameters

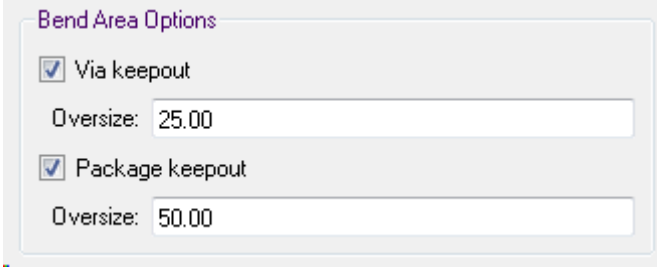


- *Inner side*: This field defines the inside surface of the bending area. The options are TOP or BOTTOM. Selecting TOP, indicates the bend is in the upwards direction, whereas selecting BOTTOM indicates a downward direction.
- *Inner radius*: This field defines the bend radius on the inside surface of the bend area.
- *Angle*: This field defines the final angle of the bend.

- *Order*: This optional field defines the order sequence number of a bend. When multiple bends exist in a design, the sequence of bends may impact the final result of a flex or rigid/flex bend process.



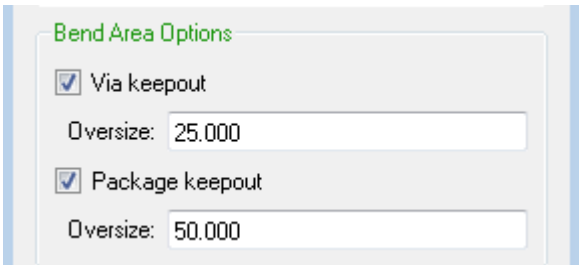
Bend Area Options



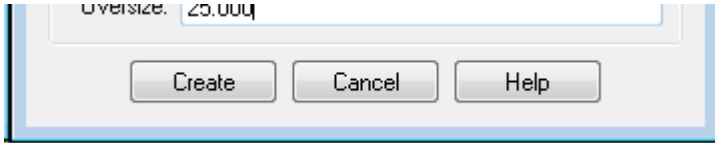
- *Via keepout*: Selecting this checkbox indicates that a via keepout is generated for the bend area. The via keepout uses the same outline as the bend area outline. Once the bend area is generated, the via keepout becomes a member of the bend area group.
  - *Oversize*: This field expands the via keepout size from the bend area size. The via keepout does not expand beyond the DESIGN_OUTLINE boundary.
- *Package keepout*: Selecting this checkbox indicates that a package keepout is generated for the bend area. The package keepout uses the same outline as the bend

area outline. Once the bend area is generated, the package keepout becomes a member of the bend area group.

- *Oversize*: This field expands the package keepout size from the bend area size. The package keepout does not expand beyond the DESIGN_OUTLINE boundary.



- *Create*: Applies the values defined in the dialog box and creates the *Bend Area Group* with the *Bend Name* as the group name.



- *Cancel*: Closes the *Create Bend Area* dialog box.

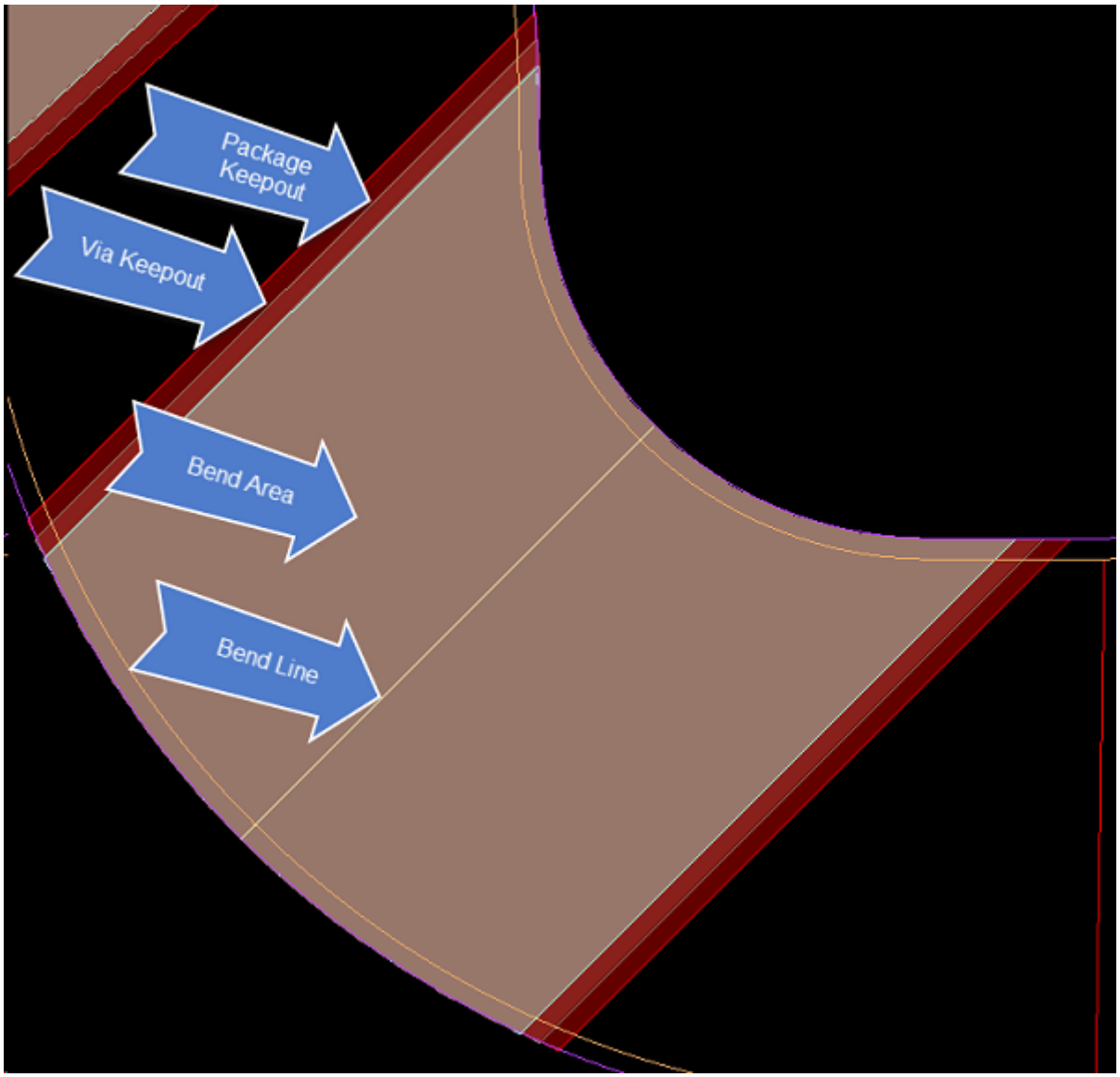


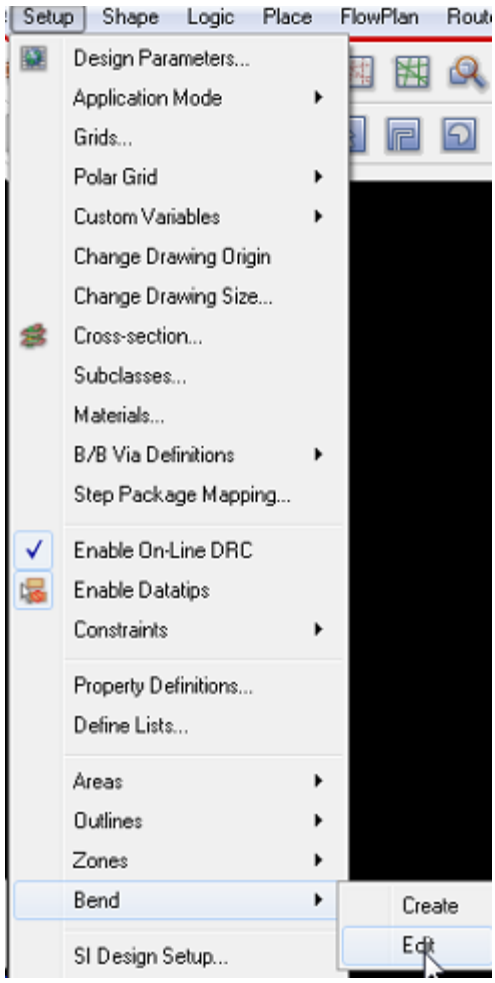
Figure 1-1 Bend Area Objects

Note: Bend areas are not allowed to overlap. If the bend area parameters cause a bend area to overlap another bend area, new bend area creation fails.

```
Use Create to generate a bend area or re-add bend line.
Bend area extents overlapping with existing bend.  Not created.
Command >
```

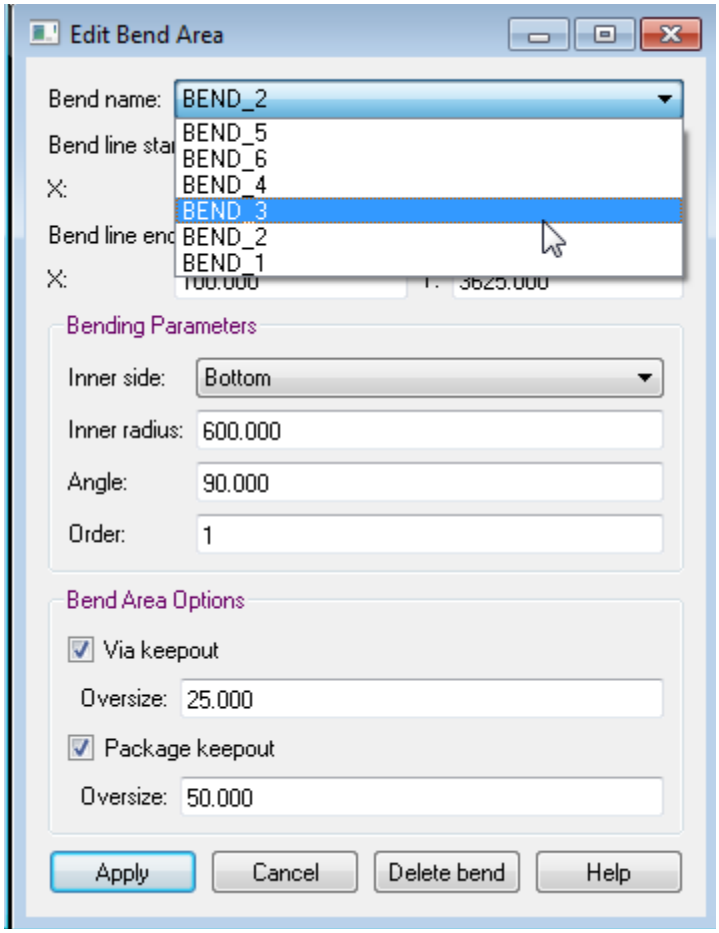
Editing a Bend Definition

From the PCB Editor menu, select *Setup – Bend – Edit*.



The *Edit Bend Area* dialog box appears. The first step is to select a bend area for editing. The bend area selection is made by using the pull-down menu from the *Bend name* field and

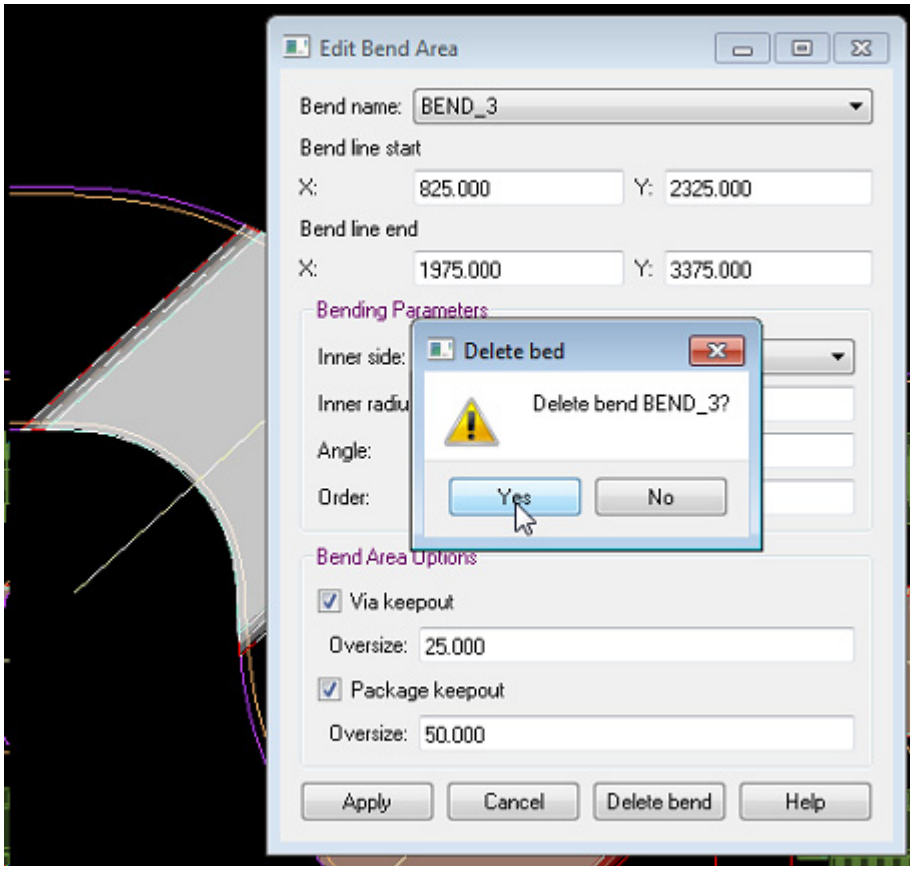
selecting one of the available bend areas that exist in the design. Once the bend area is selected, the PCB Editor window zooms into the selected bend area.



Bend line start and end points may be manually entered in the *Edit Bend Area* dialog box, or by mouse picks in the design canvas. Bend data and bend area options are adjusted in appropriate fields of the dialog box. Select the *Apply* button to update the bend area in the design to the new modifications.

Deletion of a bend area is performed by using the *Edit Bend Area* dialog box. Select the bend area to delete and then click the *Delete* Bend button. You are prompted to verify the

delete process. Selecting the *Yes* button continues the delete process. Selecting the *No* button aborts the delete process for that bend area.



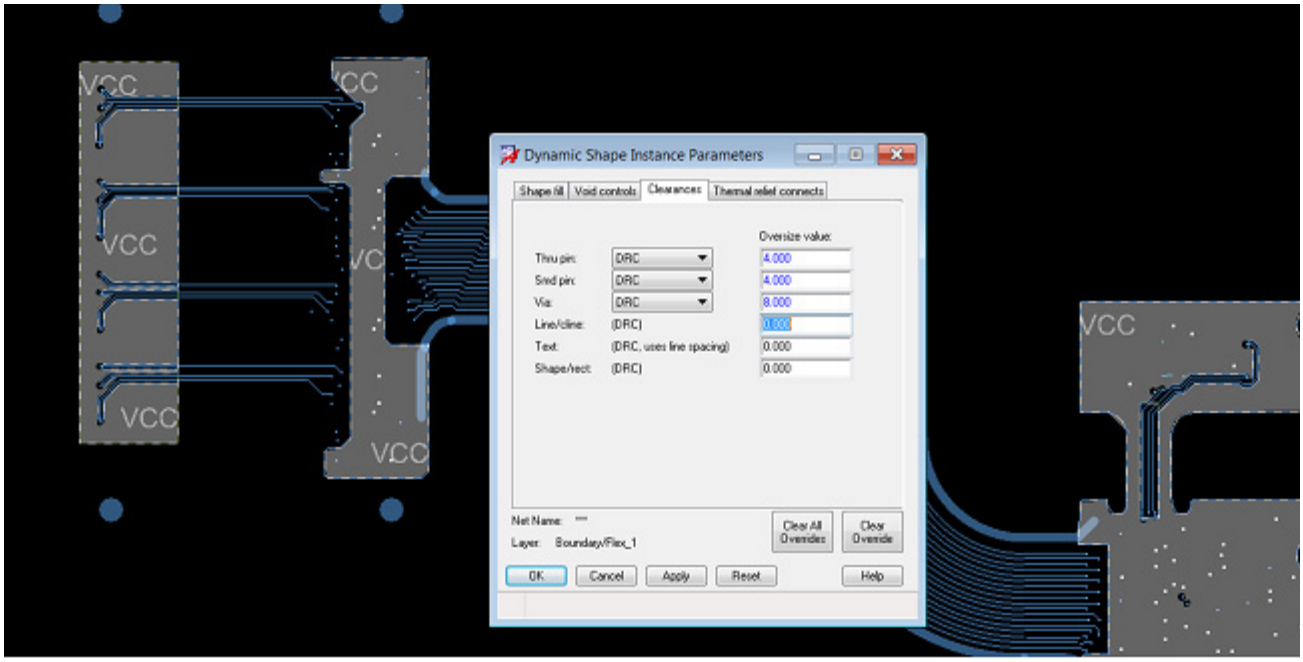
Note: Bend areas are not allowed to overlap. If the modified bend area parameters cause a bend area to overlap another bend area, then new bend area fails to be updated and may be deleted.

```
Use Create to generate a bend area or re-add bend line.
Bend area extents overlapping with existing bend.  Not created.
Command >
```

Shape Application Mode Updates

Assigning parameters to multiple dynamic shapes is now possible by applying override parameters to a multiple selection set of dynamic shapes. While in *Shape edit* application mode, select the shapes to be updated, right-click and choose *Shape – Parameters*. Using

the new *Find by Query* application to narrow down your shape selection set. For more information, see section on Find by Query.



Add Notch Update

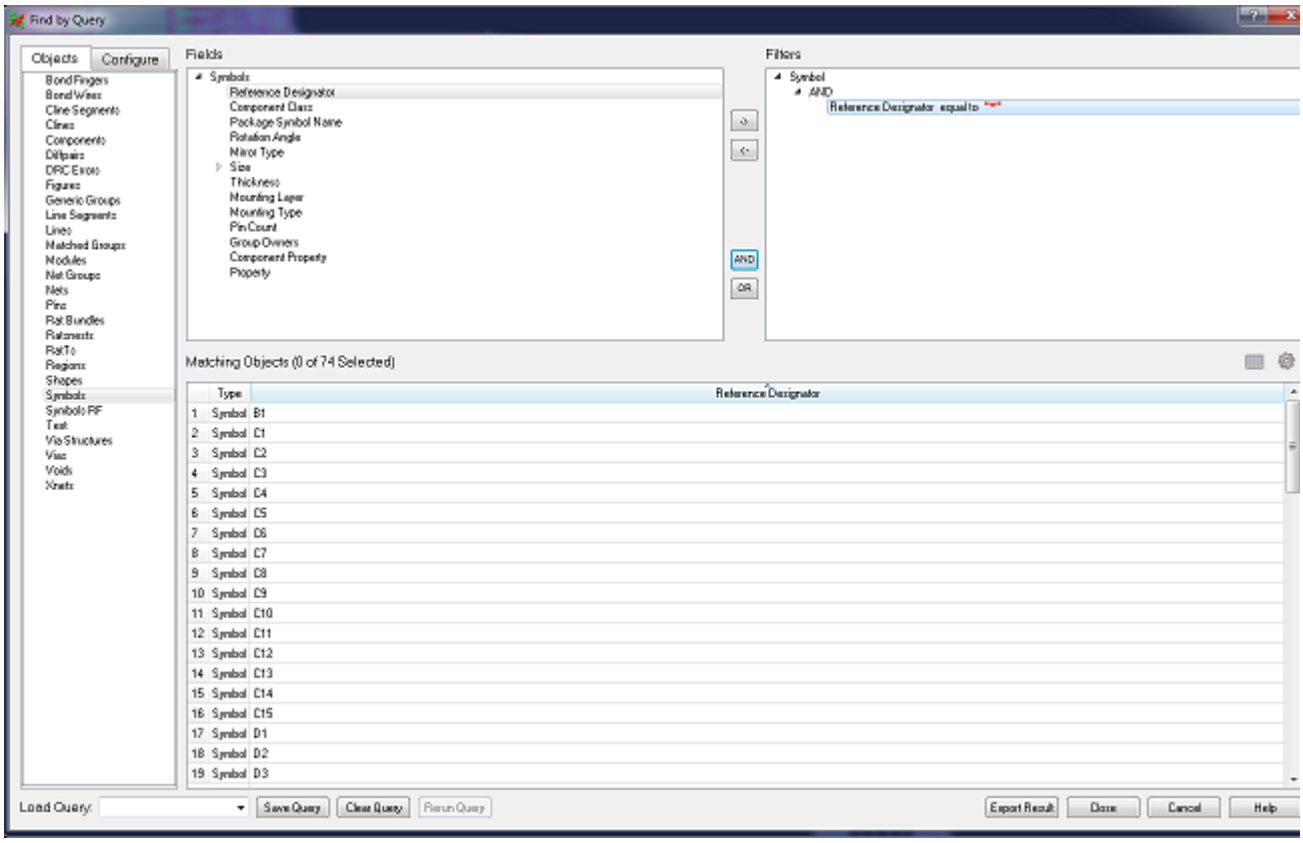
The *Add notch* command now supports any angle options with default pull-down choices of 90 (default) as well as 45 and135 degrees. Alternatively, you can directly enter angle values from 1 – 179 in the new *Add notch Angle* field located in the *Options* pane.

Slide IX/IY support

The *Shape – Slide* command now supports the IX and IY commands during the active movement of an edge. For example, an entry of IX 100 during the slide command positions the selected vertical edge 100 units in the positive X direction.

Find by Query

The *Find by Query* function, located in the *Find* pane, has been modernized to easily locate the complete set of design elements in the canvas. Now, with a few clicks, you can create, save, and recall time saving queries. The saved queries can also be re-used in new designs and can be used with all *Edit* commands.

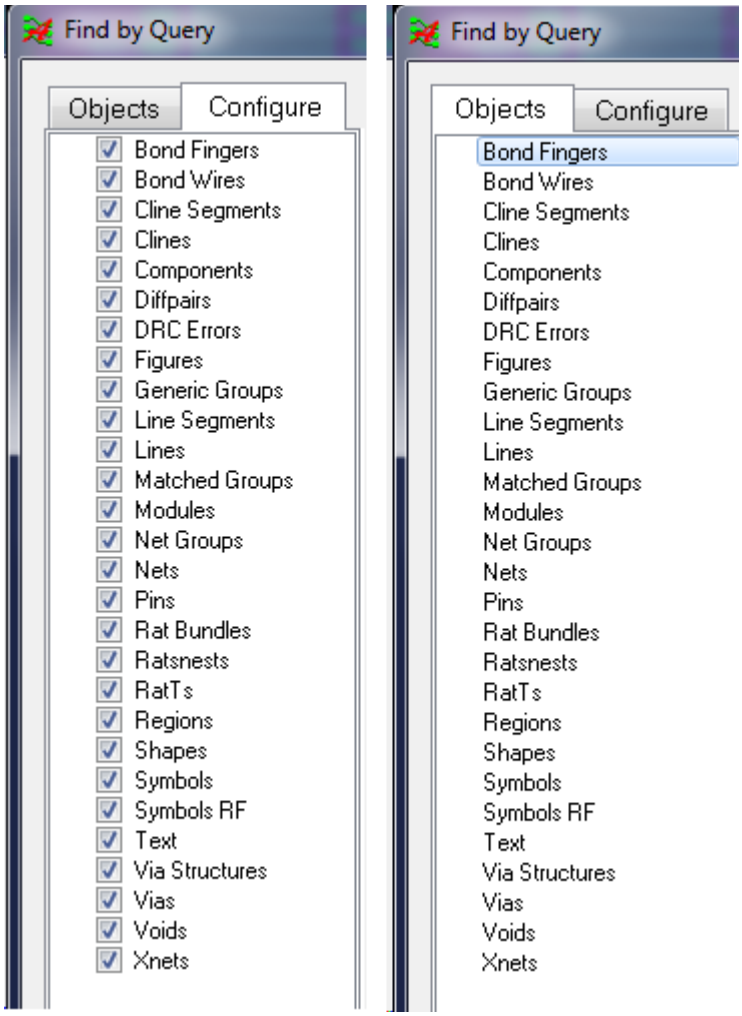


Find by Query Options

The Configure tab of the Find by Query form lets you set the visibility and selectibility of the different objects.

Configure Tab

Configure which design elements/objects are available when creating a query. In the following images, all objects are checked in the *Configure* tab which means they are all visible and selectable in the *Objects* tab.

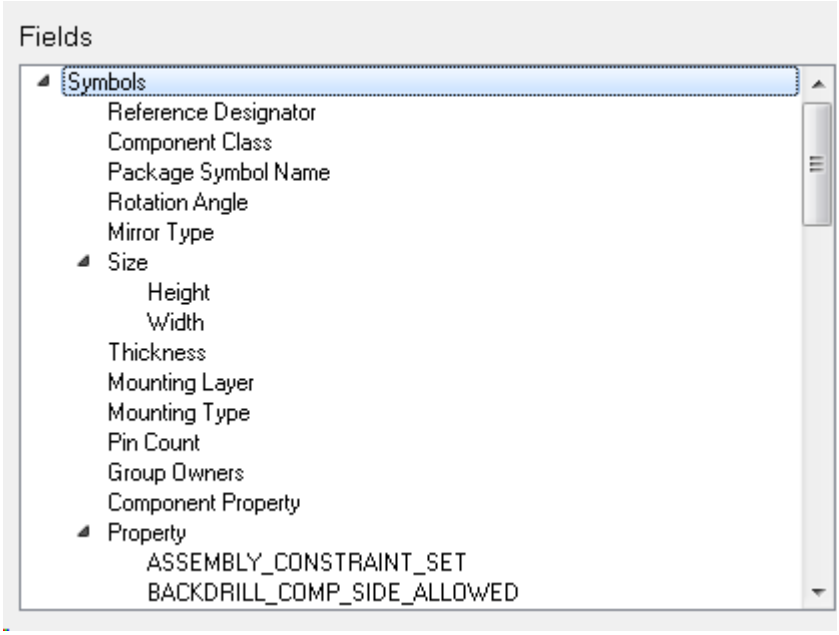


Find by Query Basics

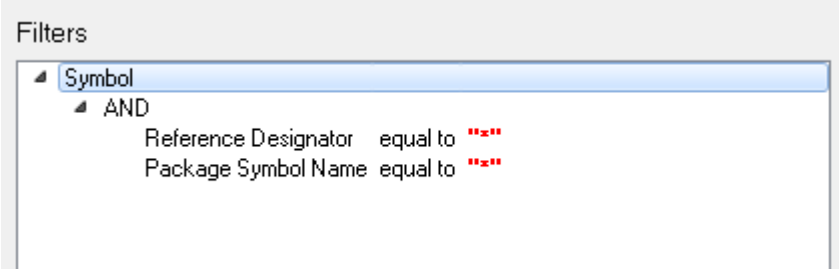
- Queries are created by moving elements from the *Objects* tab to the *Fields* pane. As objects are added to the *Fields* pane, they expand to reveal the attributes unique to them. Queries are then created and refined by moving attributes from the *Fields* pane to the *Filters* pane. As items are added to the *Filters* pane, items in the design that match the query are displayed in the *Matching Objects* pane.
- Elements can be moved from one pane to another in three possible ways:

- Double clicking on an element
- Drag and drop from one pane to another
- Using the left/right arrow buttons

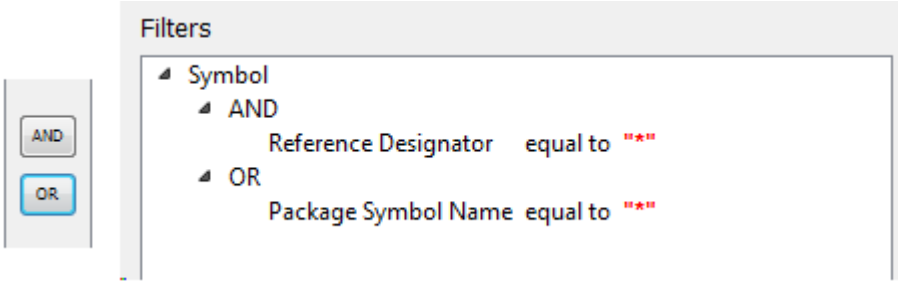
- The *Objects* tab determines which elements can be part of your query. Items unchecked in the *Configure* tab will not appear in this pane.
- Objects added to the *Fields* section may have multiple elements – all of which can be chosen to be part of the query. Available elements can be viewed or hidden simply by clicking on the small triangle to the left of the object name.



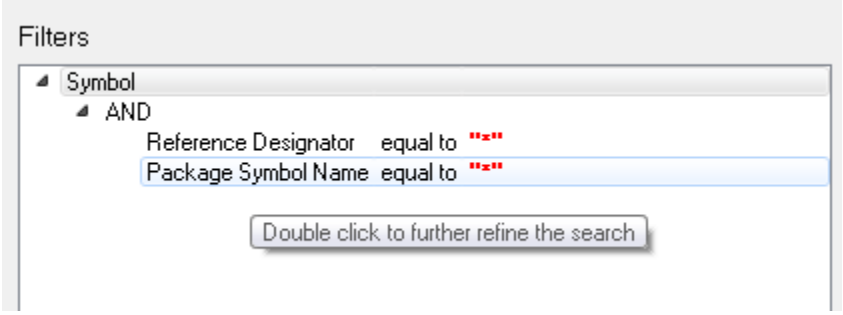
- Queries are created once elements are added to the *Filters* pane. The following example equates to Symbols that have a Ref Des equal to “*” and a Package Symbol Name equal to “*”



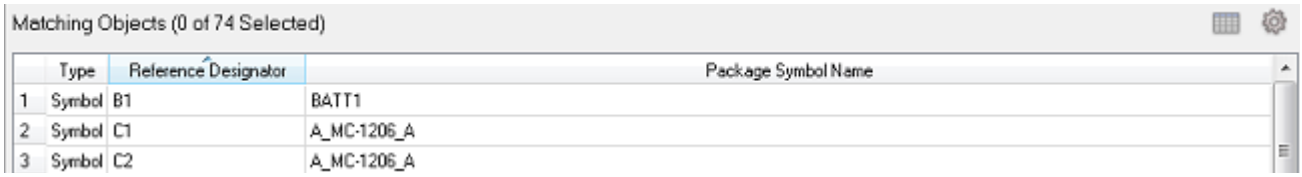
- Selecting the OR button creates a different expression as shown in the following image:



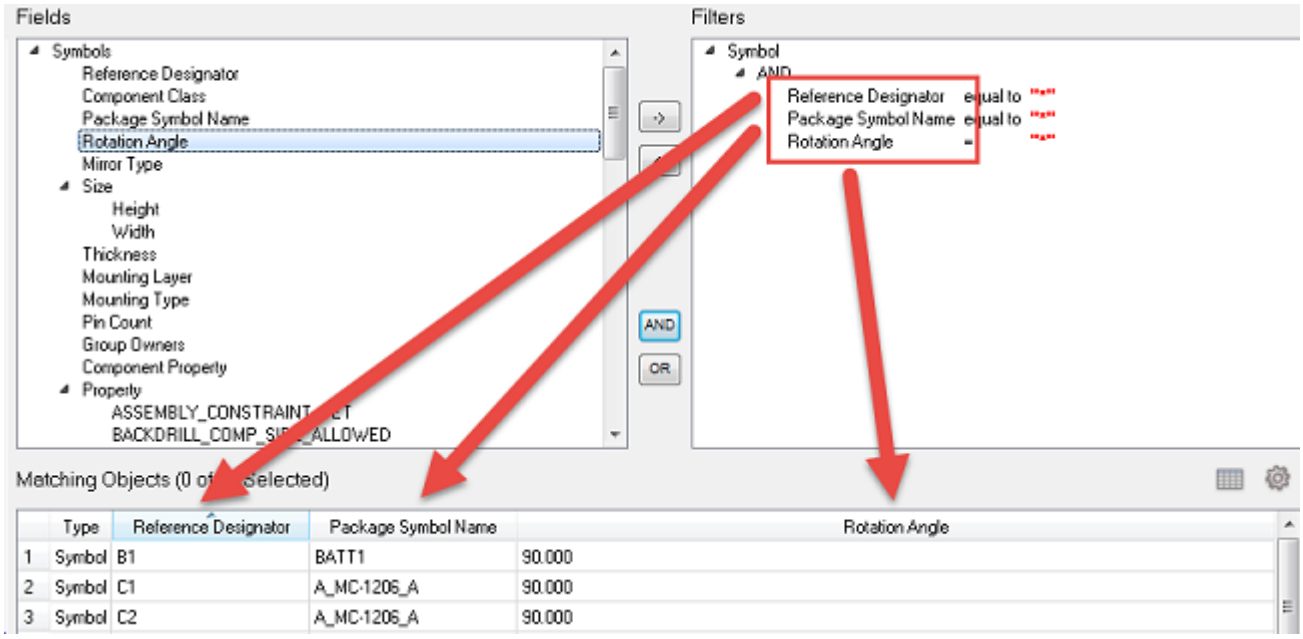
- The *Filters* default of “*”equates to all possibilities. The bold “*” and red text is a visual indicator that additional refinements can be made. A hover over pop-up has also been added as a reminder.



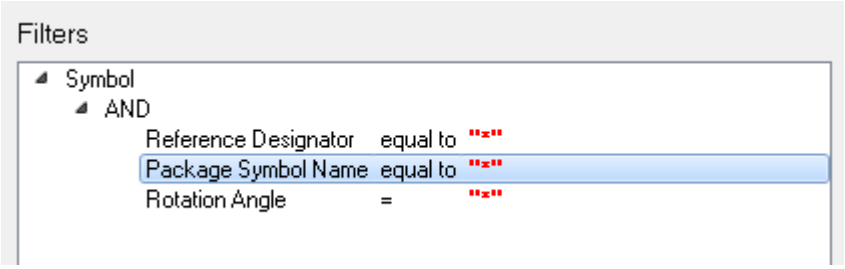
- Current results that match the query are available in the *Matching Objects* pane at the bottom of the dialog box.

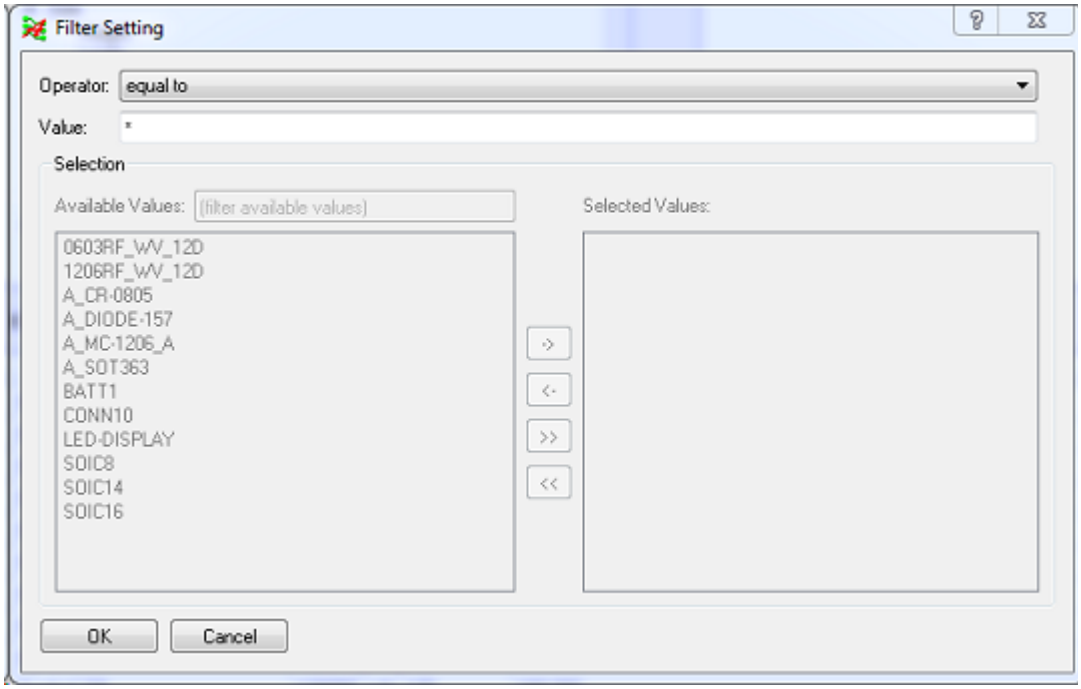


- As *Filters* are added, columns of the same type are added to the *Matching Objects* pane.

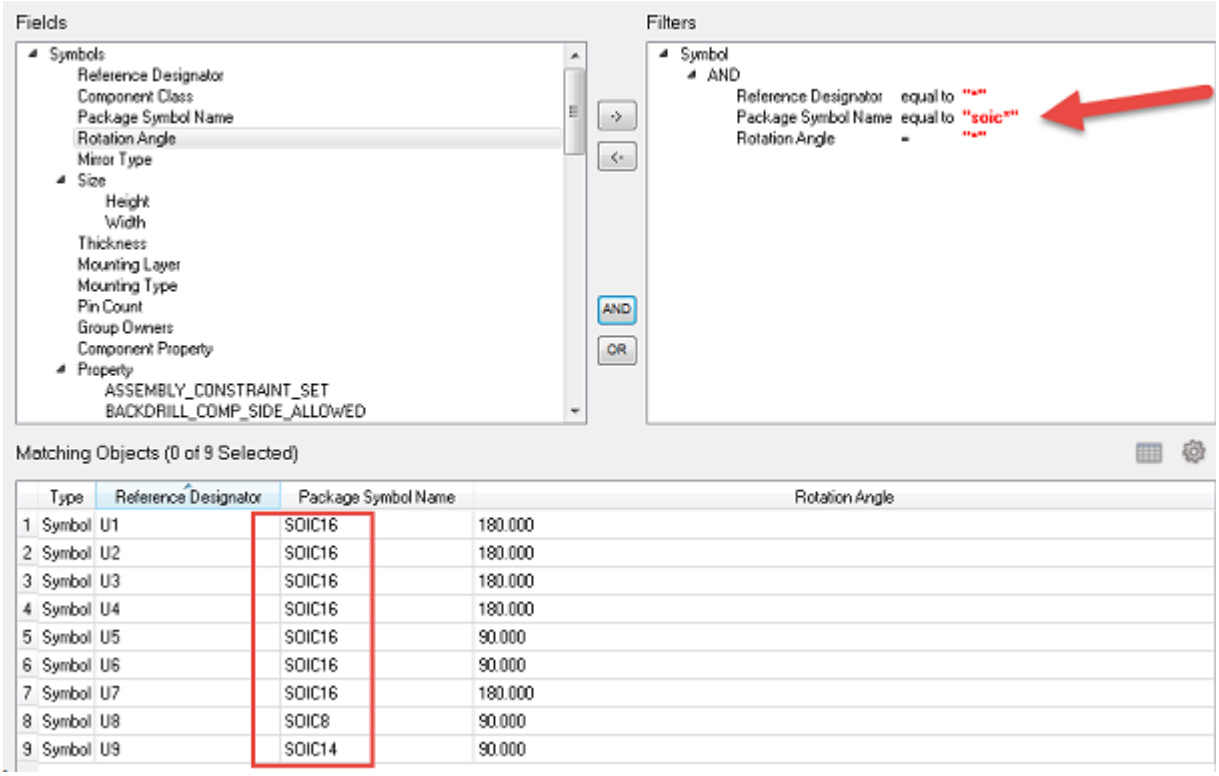


- You can refine the query by double-clicking the red text.

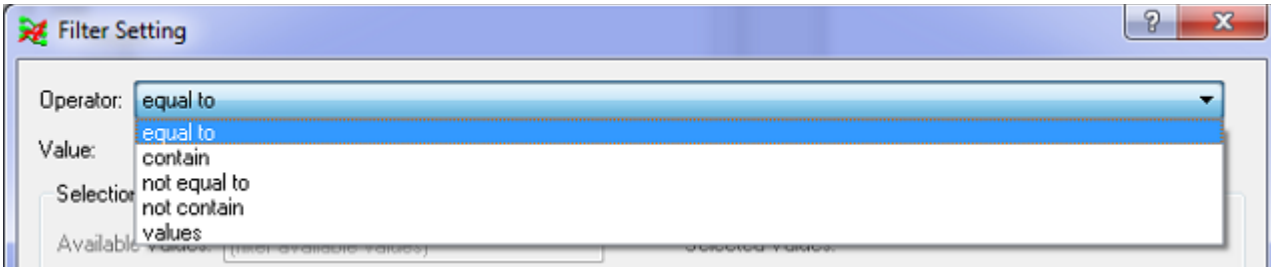




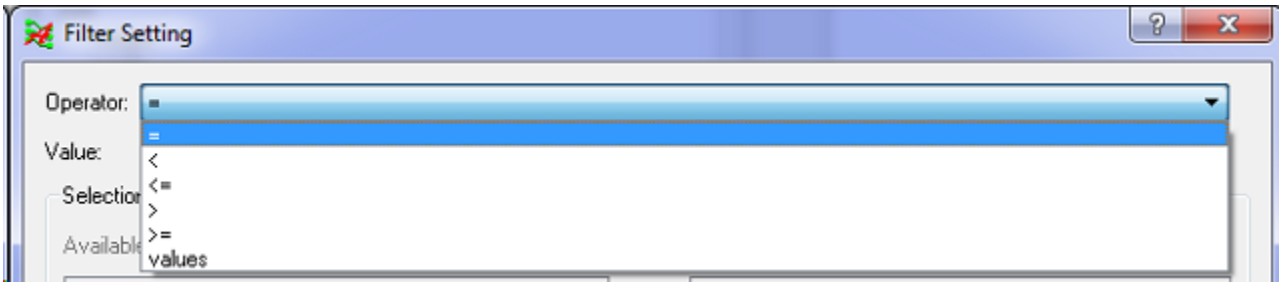
- The *Filters* support wildcard (as shown in the next image with “soic*”).



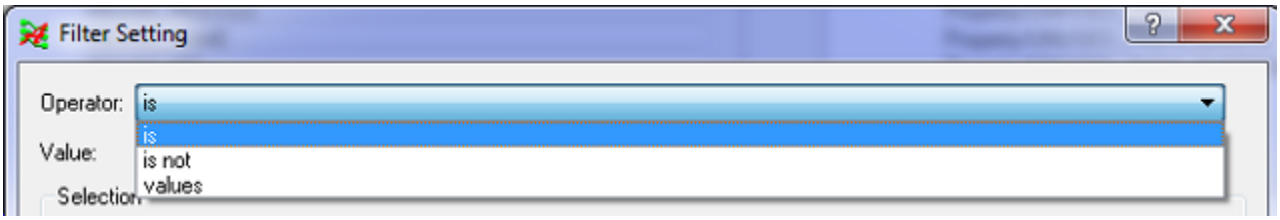
- You can refine the *Filters* with a broad set of valid operators. Some of the examples are shown in the following images.



String Operators



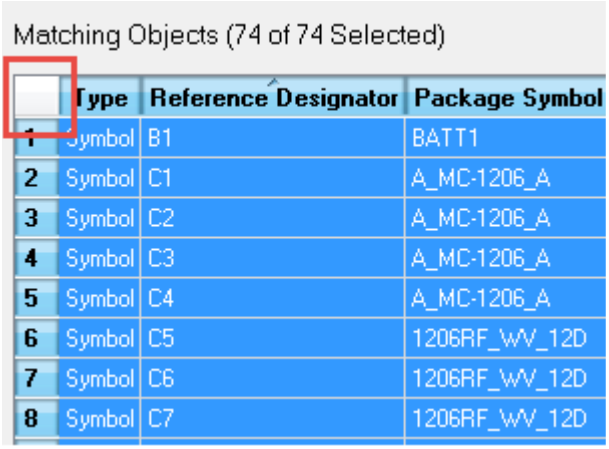
Numerical Operators

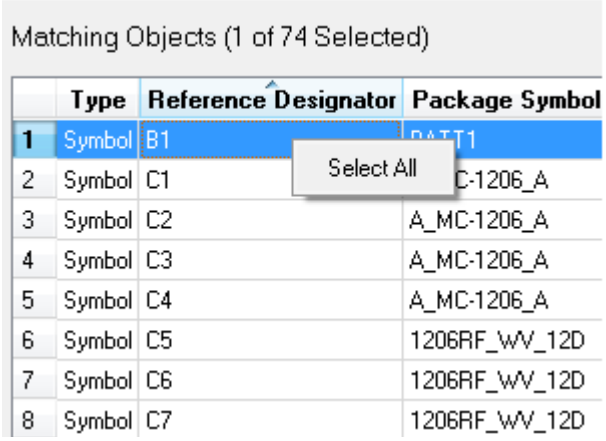


Enum Operators

- *Matching Objects* can be selected by row or as a group. Objects selected in the *Matching Objects* pane are also selected/zoomed in the canvas. All objects can be selected in one of two ways:
  - Click on the upper left square in the *Matching Objects* spreadsheet.

- Right-click on any matching object and choose on *Select All*.

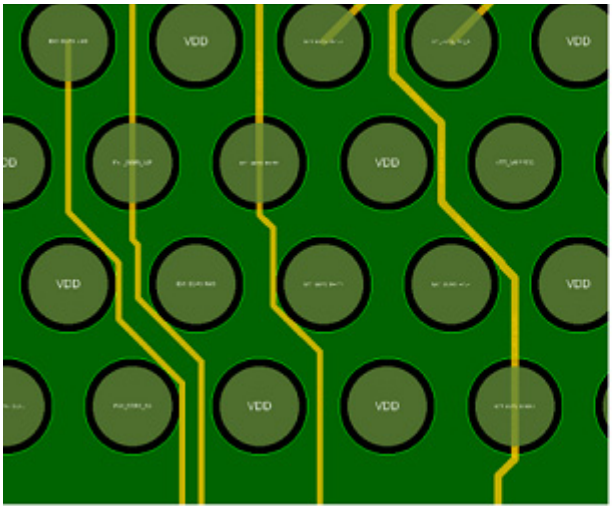




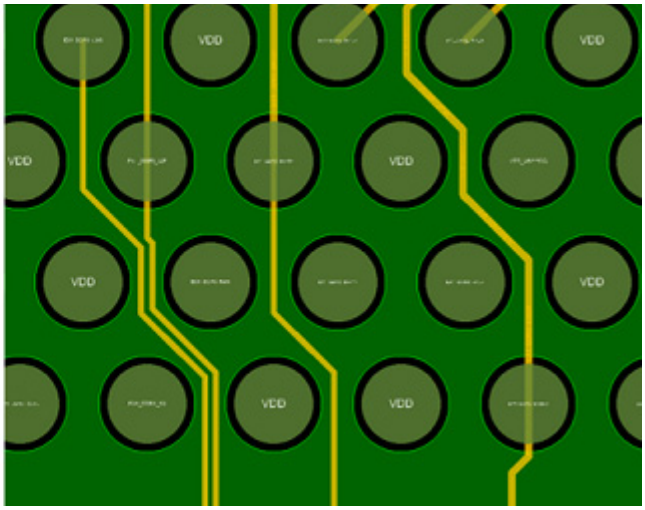
Route Optimization (Unsupported Prototype)

The new `add connect` routing behavior is designed to center the routes in a channel. To enable, set the environment preference variable *`optimize_in_channel`* in the *Unsupported* folder of the *User Preferences Editor*. The value of this variable defines the maximum channel size from pad edge to pad edge for routing optimization to take place. The

following examples show the tendency of legacy routing to hug obstacles, possibly crossing void opening while optimize attempts to center between pads with minimal jogs.



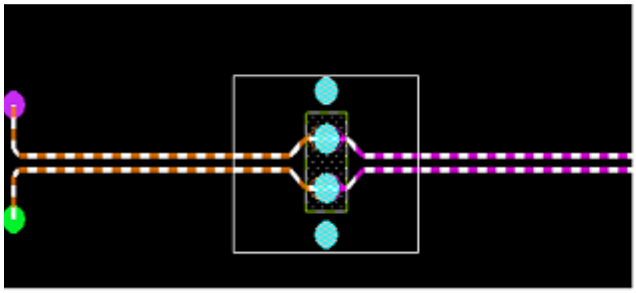
Routes are not optimized



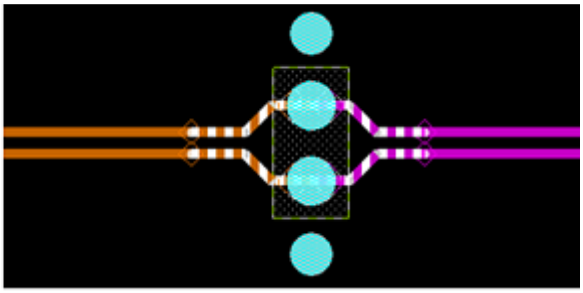
Routes are optimized

Via Structure Update

The *Route – Via Structure – Create* menu supports a new option to cut clines and only include cline/segments inside the drawn rectangle. With the new cline cutter, you no longer need to disconnect/manipulate clines so that it only includes desired portion of cline for easy re-use in design.



Draw rectangle



Clines are cut

Group Routing

The new spacing option called *Control Trace* shifts routes from that respective anchor trace. The default mode continues to shift routes from the center line outwards

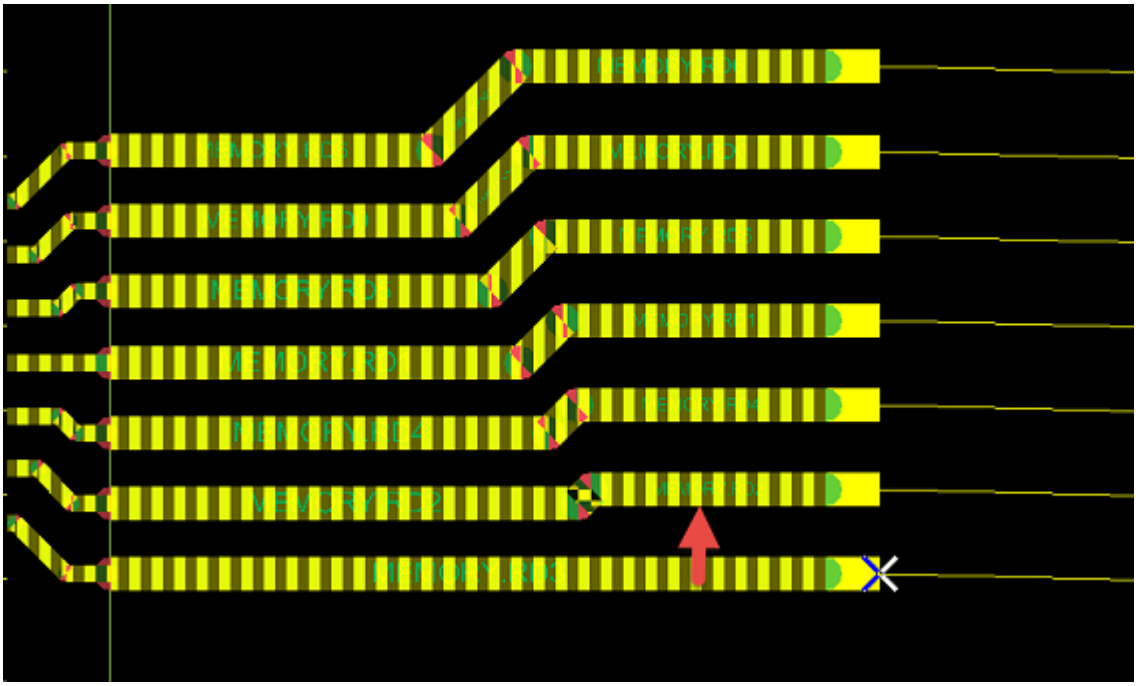


Figure 1-2 Control Trace Spacing Mode

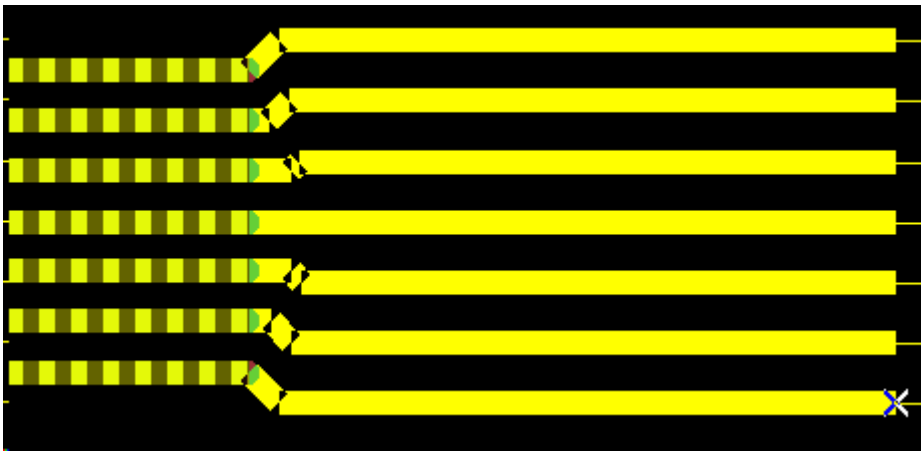


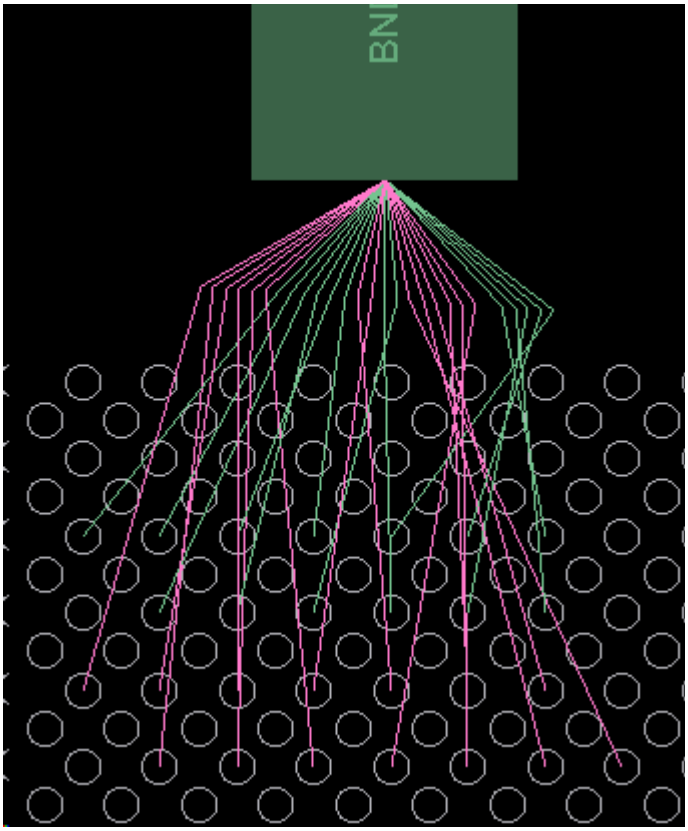
Figure 1-3 Default Spacing Mode

Create Flow Update (Unsupported Prototype)

The Create Flow command now supports a native snap to 45 degree option. This new behavior is enabled by default, but can be unset in the *User Preferences Editor*. The name of the variable is *Create Flow on 45*.

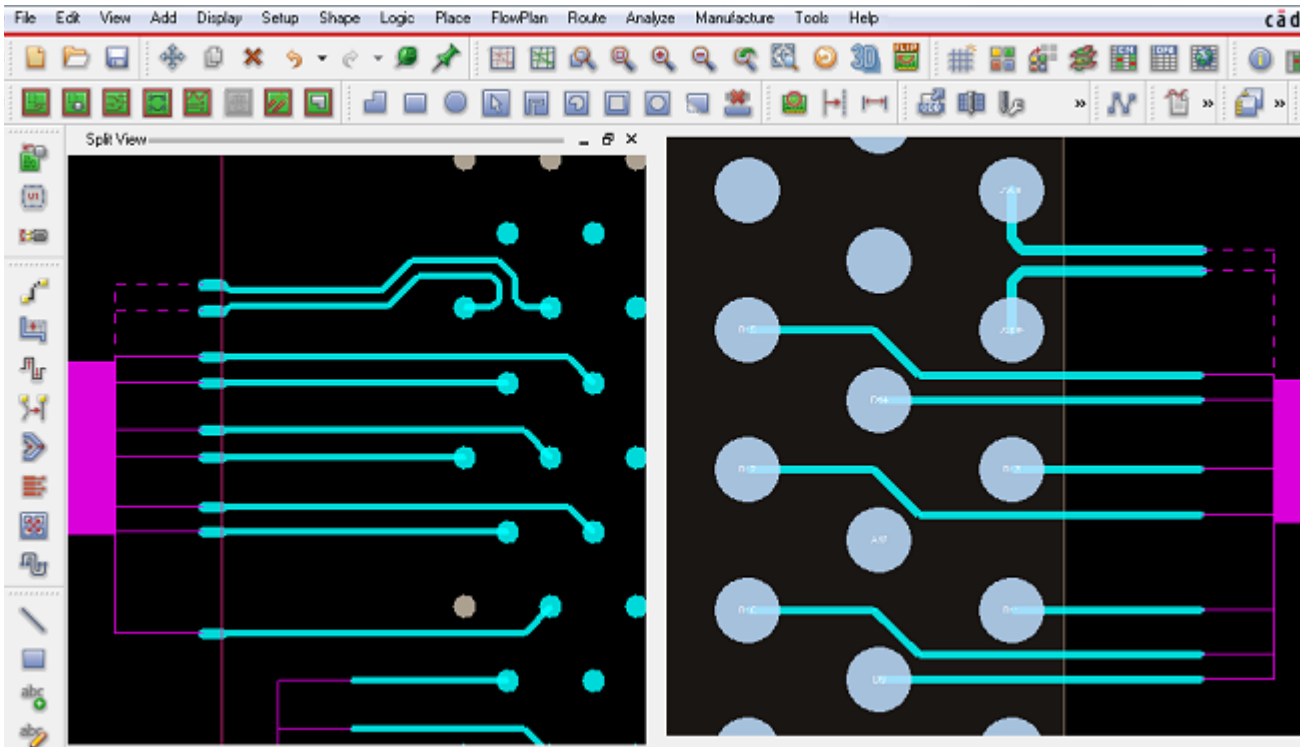
Bundle Layer Control

You can now assign desired routing layers to individual rats on bundles without the need to split the bundle. The Rat Layer Control is a new mechanism for assigning routing layers in `AiBT` and Auto Connect. Hover over the bundle, right-click, and choose *Flow Edit – Ratlayer Control* and select the desired rats.



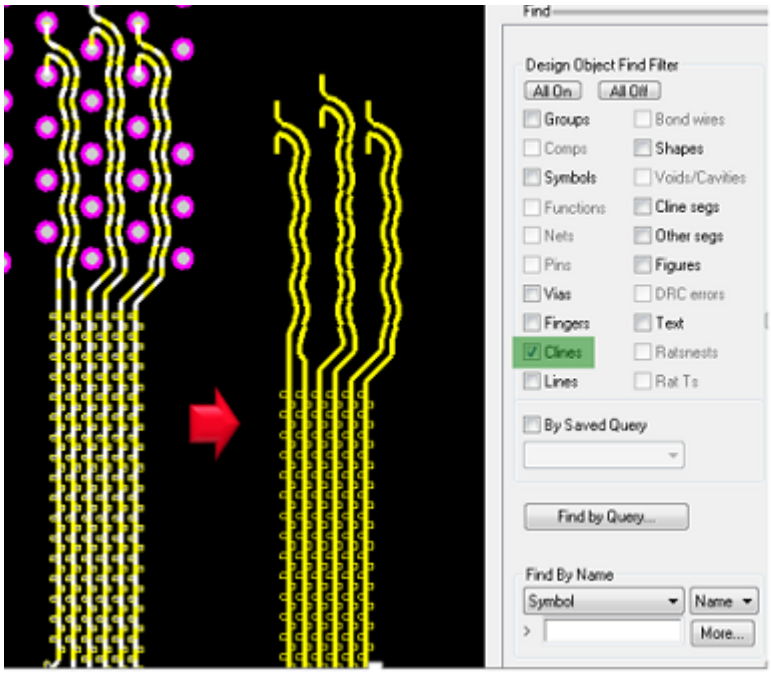
Enhanced Bundle Viewing

It may be advantageous to view in a split screen both ends of a bundle especially during the package breakout stage of the design process. On selecting a bundle in a pre-select mode a new option called *Split Bundle View* is available in the context-sensitive menu.

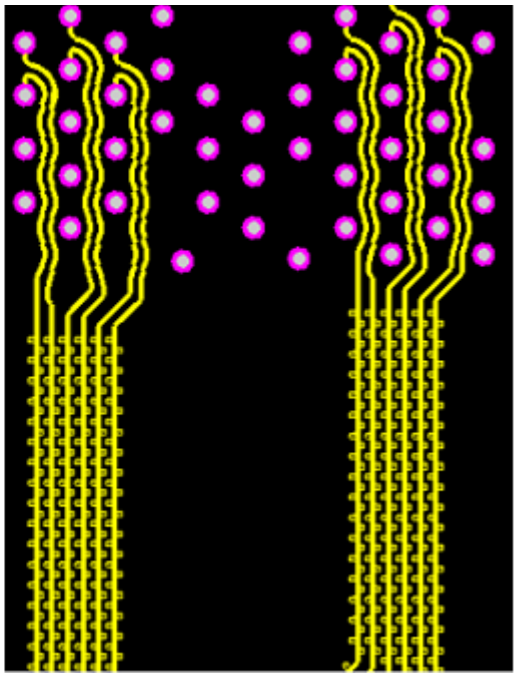


Tab Routing Update

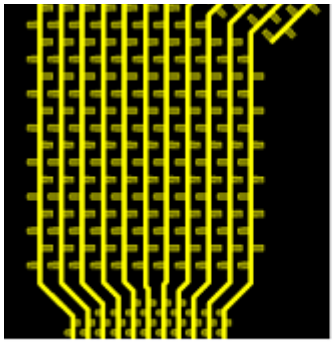
The etch editing commands have been enhanced to intelligently keep or remove existing tabs on clines or segments. The suite of *Tabbed Routing* commands are part of the *High Speed* product option and are located in the *Route – Unsupported Prototypes* menu.

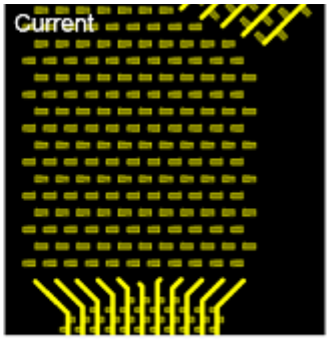


Tabs are copied with cline/segments



Easily copy multiple cline/segments with tabs and snap to pads or cline segments





Currently, when clines/segments are deleted, tabs are left behind

In 17.2 QIR1, tabs are deleted with clines/segmen

Add RF Trace

A new routing option is designed for RF/Analog circuits requiring shape-based routes. The *Add RF Trace* command can be found in the *Route – Unsupported Prototypes* menu.

- Bend Type – one of the following three bend types is used during trace routing:
  - Square – trace routed using unmitered bends.
  - Mitered – trace routed using mitered bends.
  - Curve – trace routed using curve bends with free radius values.
- Width Transition Mode – one of the following width transition modes is used to achieve transition effects at width change points during trace routing:
  - None – direct transition without any transition effect at width change point.
  - Round – round transition effect at width change point.
  - Taper – taper transition effect with specified length at width transition point.
- Transition Taper Length – the normal length of the taper to achieve transition effect. The length of the actual taper may be shorter than this value because there is no enough space on the segment where the taper effect is applied.
- Conductor Line Width – the width of the conductor segments of the trace.
- Centerline Curve Radius – the centerline curved radius for trace with curve bend effects.
- Miter Fraction – miter fraction value for trace with mitered bend effects.

- Snap to connect point – when checked, the command tries to snap to an object during routing.
  - Inherit Width – when *Snap to connect point* is checked, this field is enabled. If checked, trace width is inherited from the snapped object, if possible. The field is mutually exclusive to *Taper Connect to Pin*.
  - Taper Connect to Pin – when *Snap to connect point* is checked, this field is enabled. If checked, trace segment connecting to the snapping pin is tapered.
- Create generic shape – This enables generic shape editing commands to operate on the added shape.

Convert RF Trace

Use to convert RF traces to generic shapes. This should be used if shape boundary edits are necessary. The *Convert RF Trace* command can be found in *Route – Unsupported Prototypes*.

Chip on Board (COB)

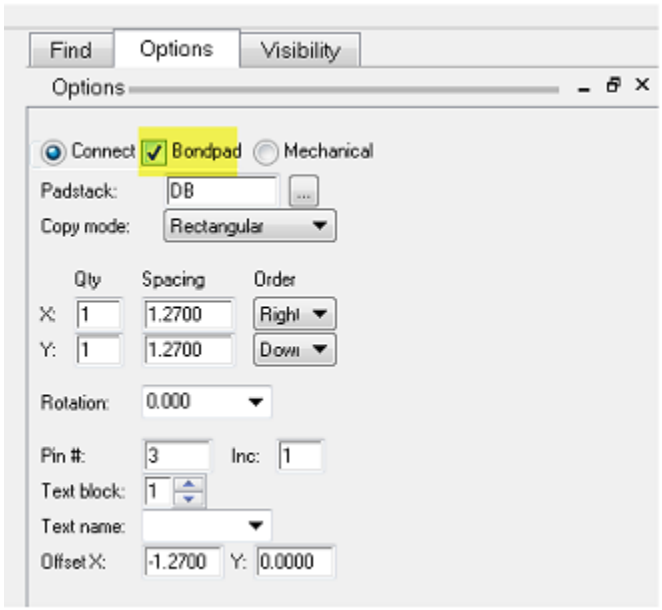
Chip on Board, also known as Direct Chip Attachment, refers to the assembly process where a bare die is mounted, electrically connected with wires and typically encapsulated with a silicone or epoxy based material on the Printed Circuit Board. The implementation of such technologies is seen across the Consumer, Telecom, Computer, Mil-Aero, Avionics, and Medical Equipment market sectors.

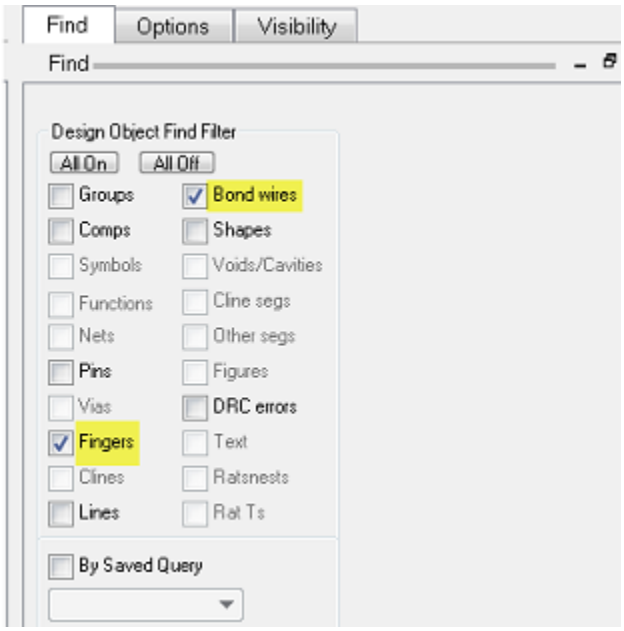
In this release, Allegro PCB Editor supports basic wire bond applications. Advanced automated functions originating in the APD/SIP tools have not been tiered down to PCB Editor.

Getting Started

Package Symbols targeted for wire bond application must be created using the *Bondpad* option while in the Symbol Editor. Existing library symbols cannot be directly leveraged by the PCB Editor wire bond applications. Pins on existing symbols will have to be deleted then re-

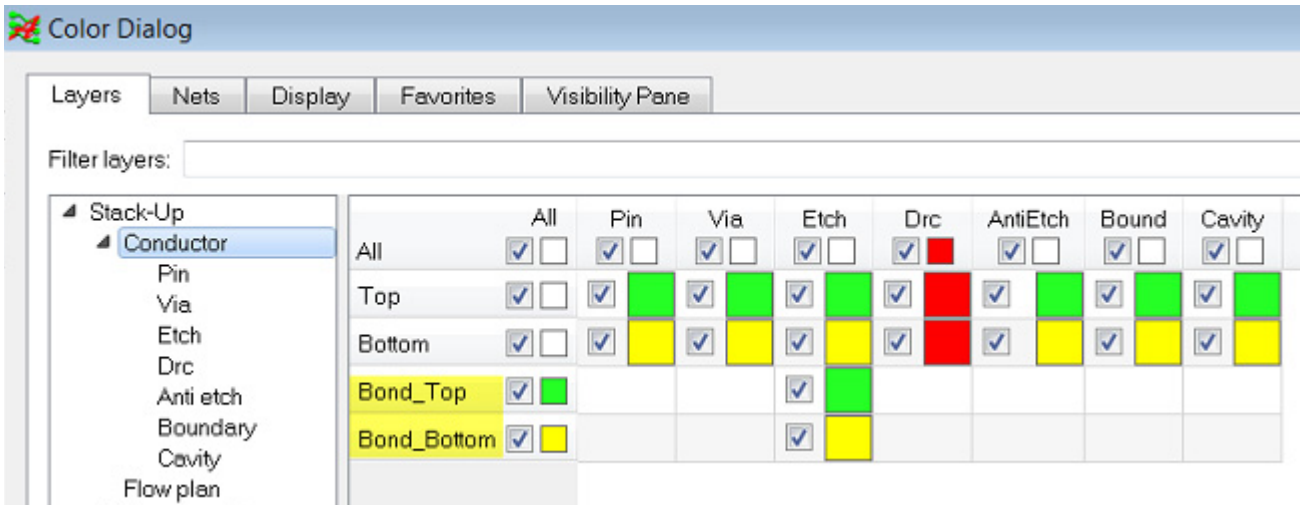
added with the *Bondpad* option shown in the left figure. In addition, the *Find* filter has been updated with 2 new entries; *Fingers* and *Bond wires*.





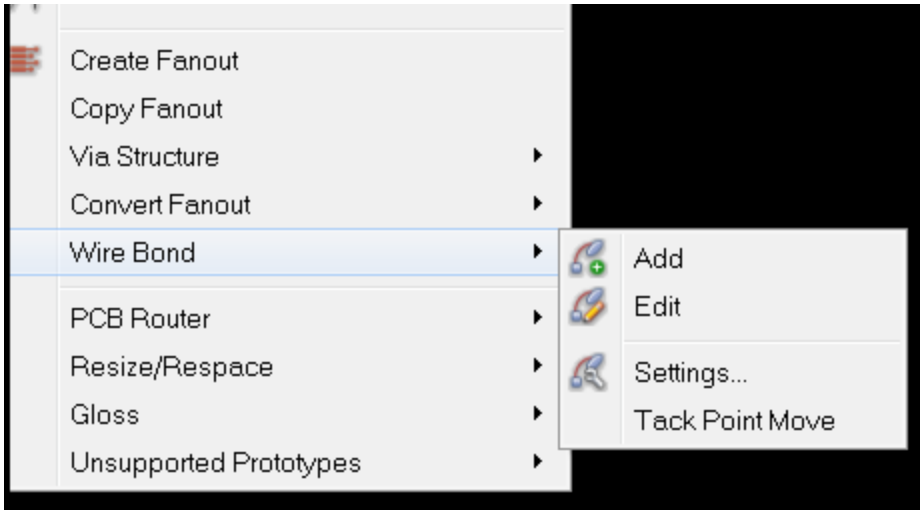
New Subclasses

Two new subclasses (*Bond_Top* and *Bond_Bottom*) are available to support the package symbol that includes die pins. These layers should be considered as virtual layers as they are not typically included in fab packages.



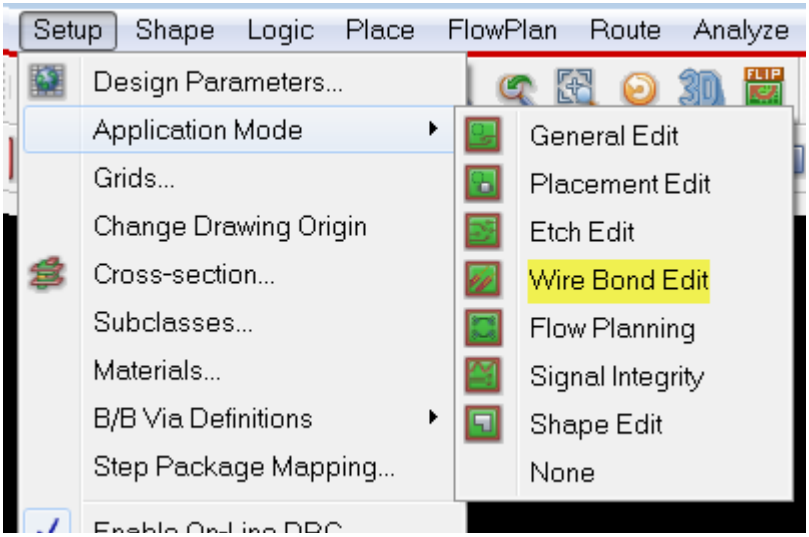
Menu Path

The wire bond commands inside the Allegro PCB Editor are located in the *Route* menu. They include *Add*, *Edit*, *Settings*, and *Tack Point Move*.



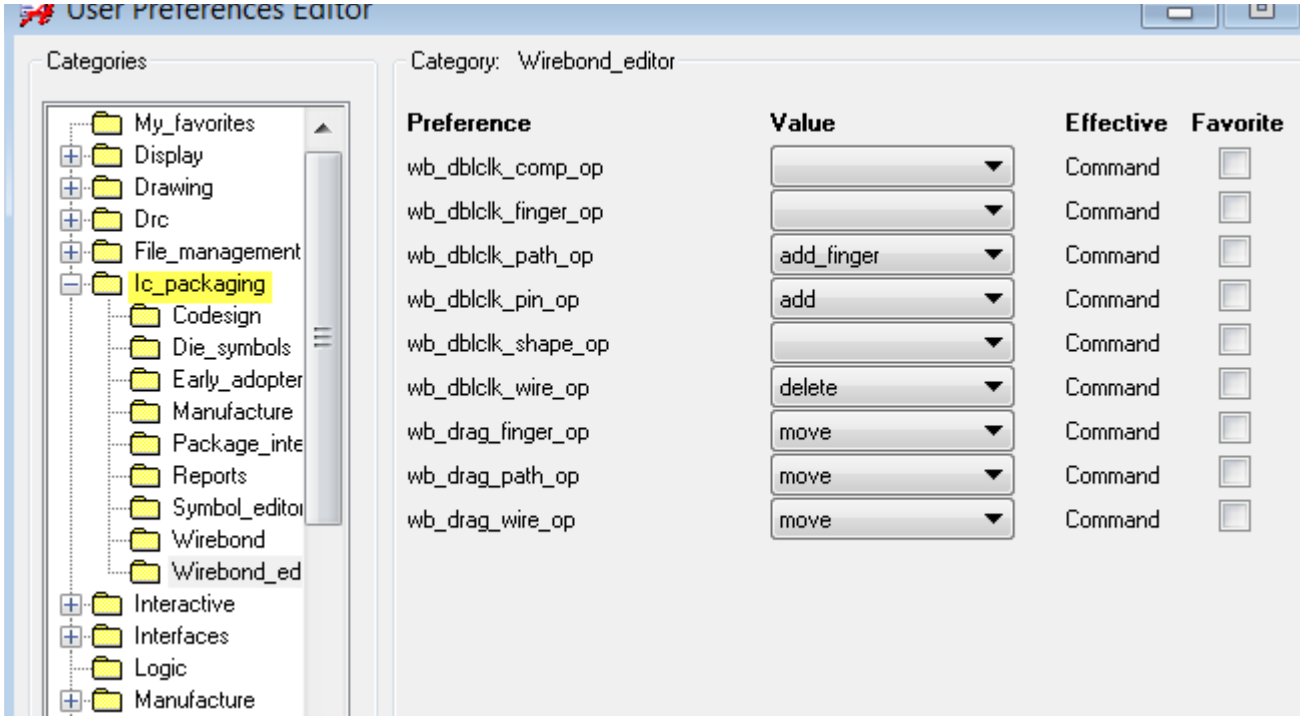
Application Mode

A new *Wire Bond Edit a*pplication mode is available for working in a noun-verb editing environment.



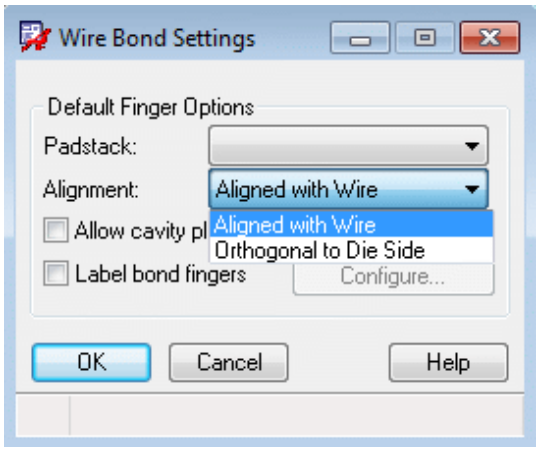
User Preference Variables

A suite of variables is available to customize the command behavior. Based on the following examples, a double-click on a die pad invokes the `wirebond_add` command.



Defining the Bond Finger Pad

The padstack and alignment options used for *Bond Fingers* can be set in the *Route – Wirebond – Settings* file.



Adding a Wirebond

Wirebonds can be added by selecting single or multiple pins. Feedback is provided as to the length and angle of the wire.

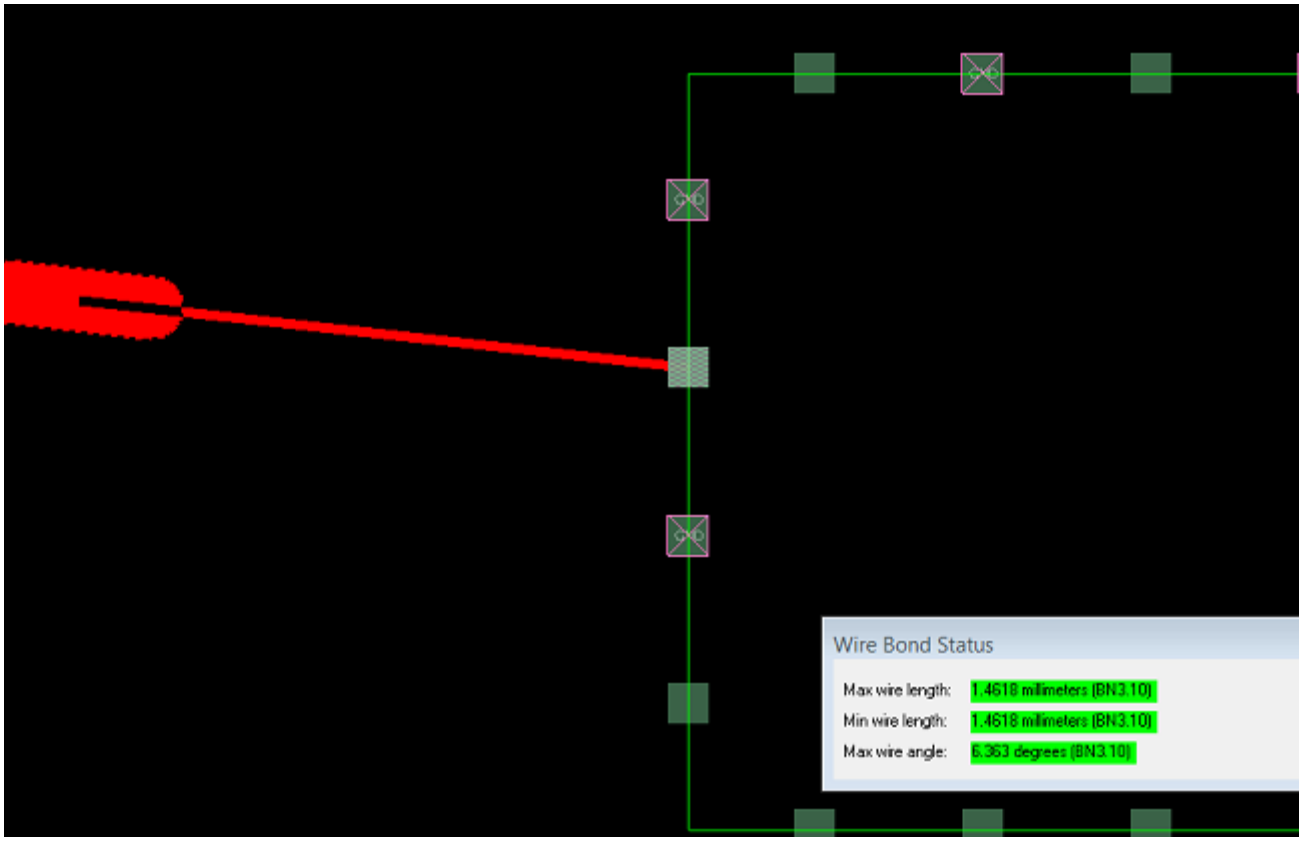


Figure 1-4 Adding a Single Wirebond

Moving Track Point

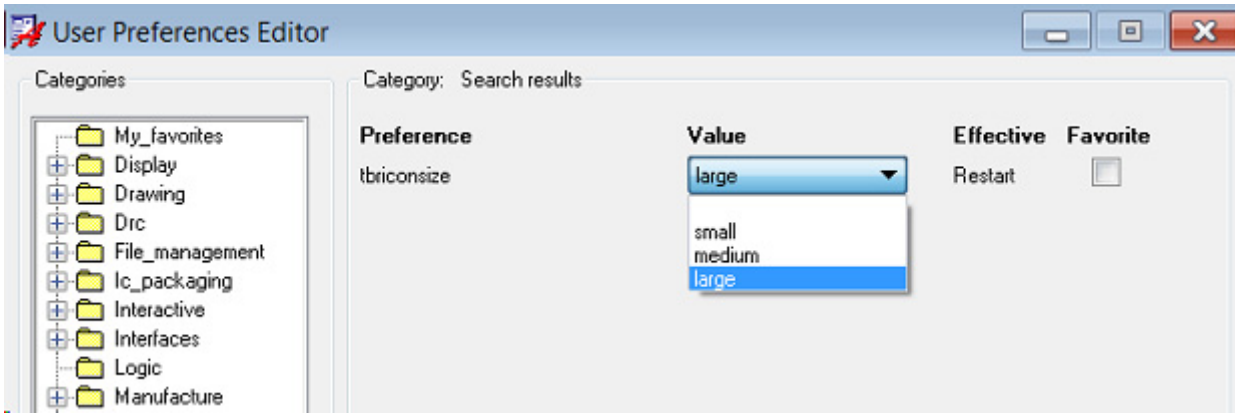
Wires can be repositioned within the bond finger using the *Tack Point Move* command. This may become necessary to support multiple wires within the bounds of the finger.

Figure 1-5 Trackpoint Move

Display Canvas

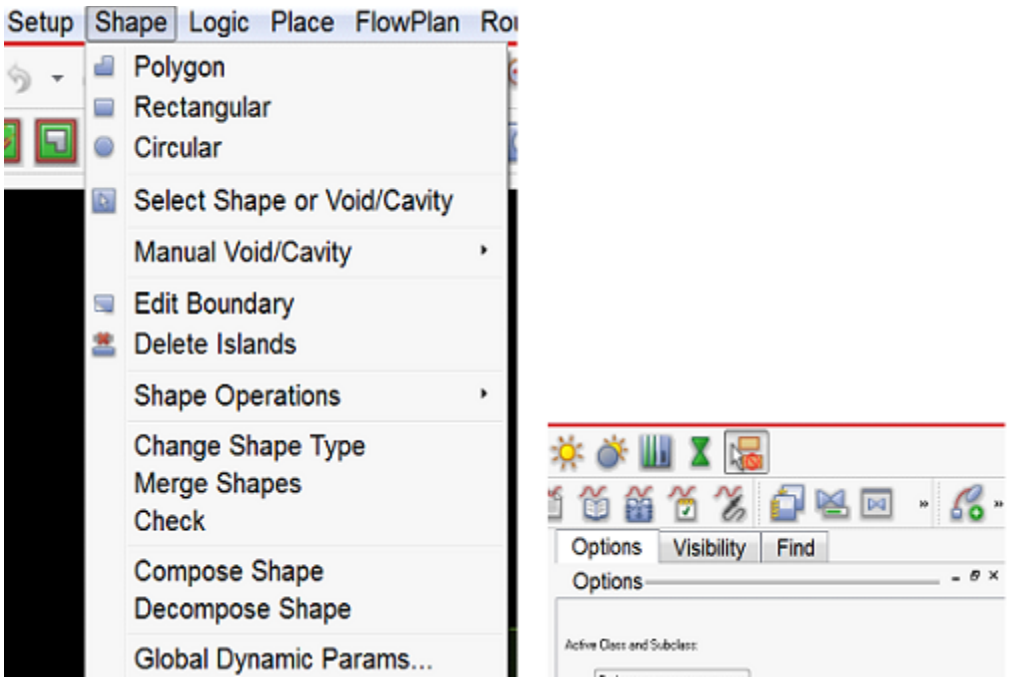
Toolbar Icons

Icon size can be controlled by the User Preference variable `tbiconsize` with values of small, medium and large.



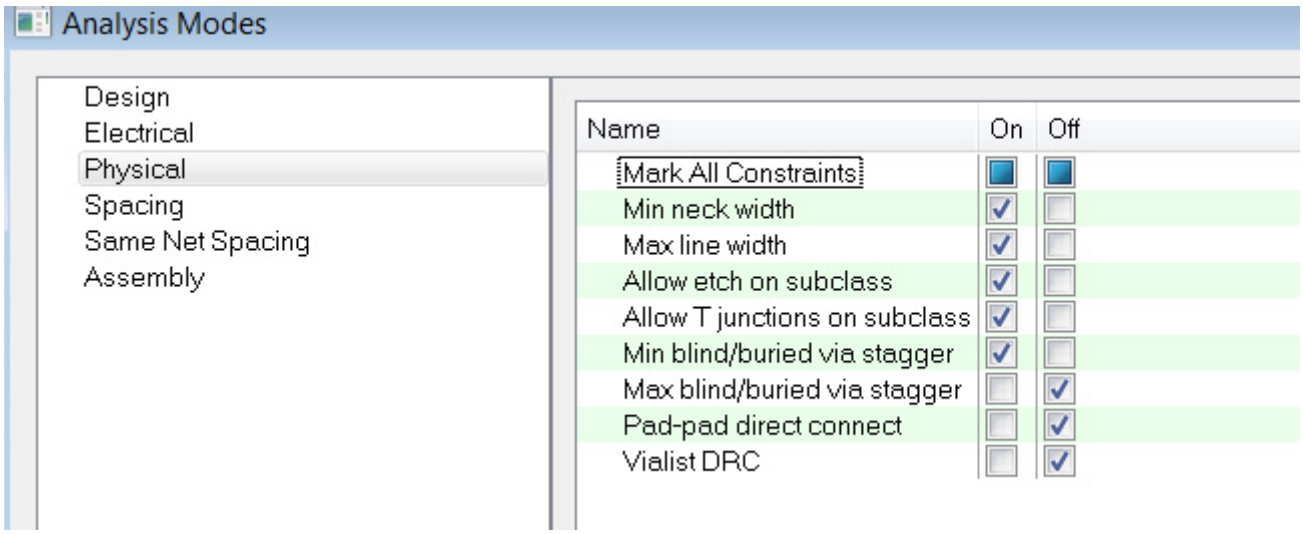
Fontsize

The legacy *fontsize* user preference variable can be used to control the size of menu text and form headers. The system default value is set to 9, following examples use a value of 12.



Analysis Mode Form Update

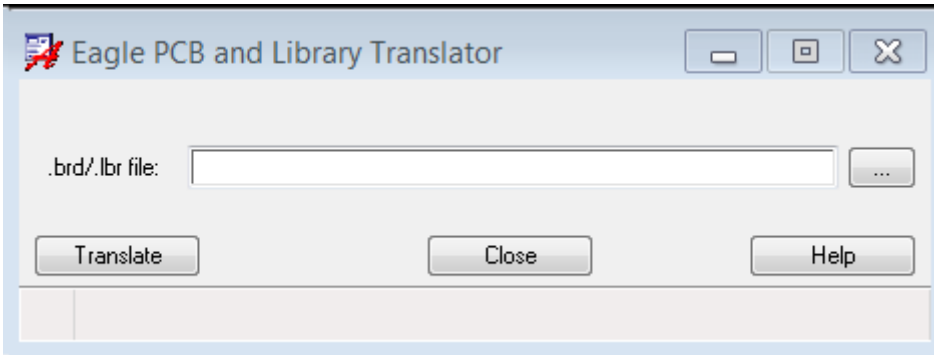
As part of a User Interface modernization initiative, the DRC *Analysis Modes* UI has been enhanced. Mode categories have been consolidated to Design, Electrical, Physical, Spacing, Same Net Spacing and Assembly for wire bond checks.



Eagle PCB and Library Translator

PCB files sourced from Eagle CAD can now be translated into Allegro and OrCAD PCB Editors. Click the *Help* button located in the translator user interface for more information.

Translator is located at *File - Import – CAD Translators.*



Productivity ToolBox Updates

The following new features have been added to the Allegro Productivity Toolbox:

- PCB Design Compare
- Custom Variables

PCB Design Compare

New toolbox application which compares two databases and identifies the differences between them. This is useful when tracking changes in the product life-cycle. The application provides two different modes:

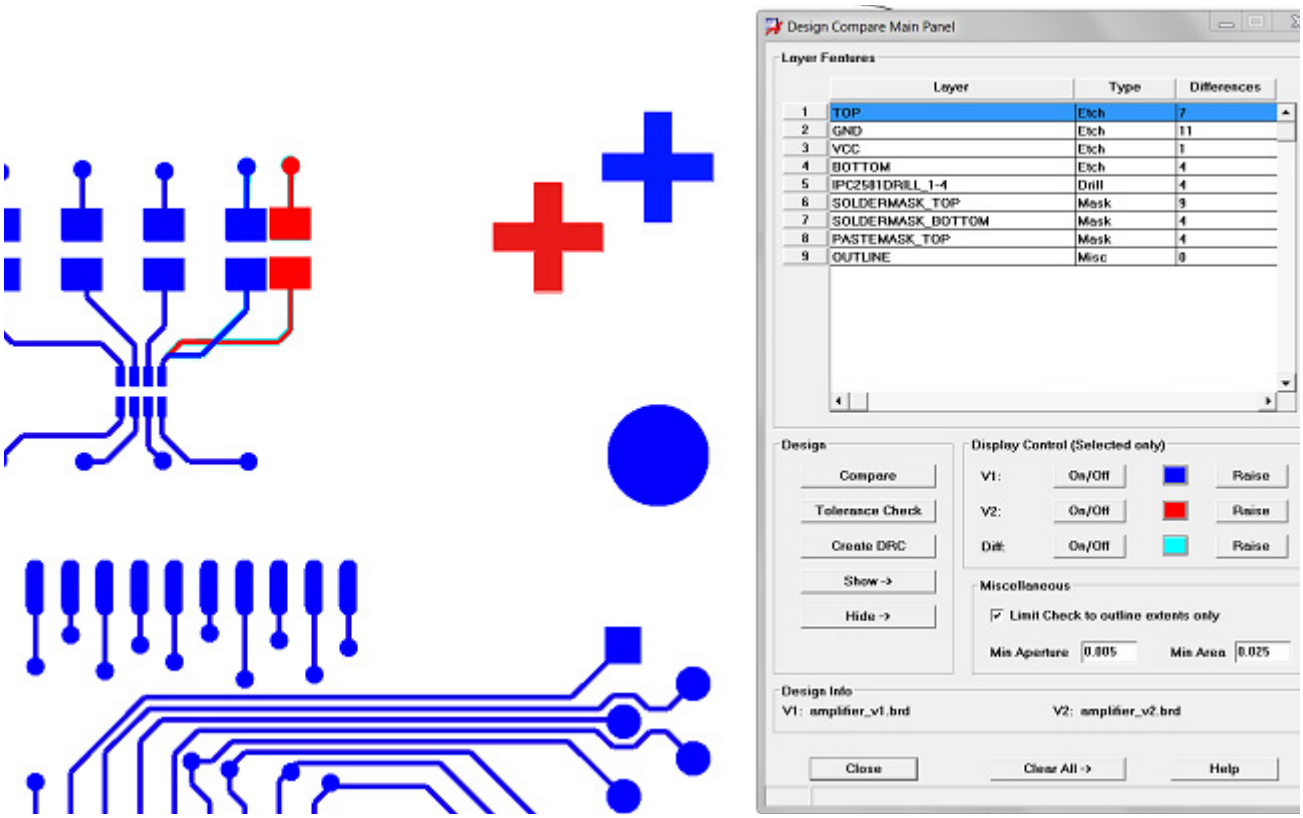
Standard Compare

Default mode which extracts and writes differences to an HTML report with information that applies to:

- Modification of stackup (cross section)
- Netlist and connectivity
- Pin connectivity modifications
- Property changes
- Testpoint modifications (testpoint moved, renamed, and so on.)
- Device type modification (ECO part)
- Placement modifications
- Renamed components

Graphical Compare

Alternatively the application lets you also compare two databases on a graphical basis. Based on IPC2581 all or individual layers can be compared. Differences are highlighted. If necessary DRC markers can be generated.

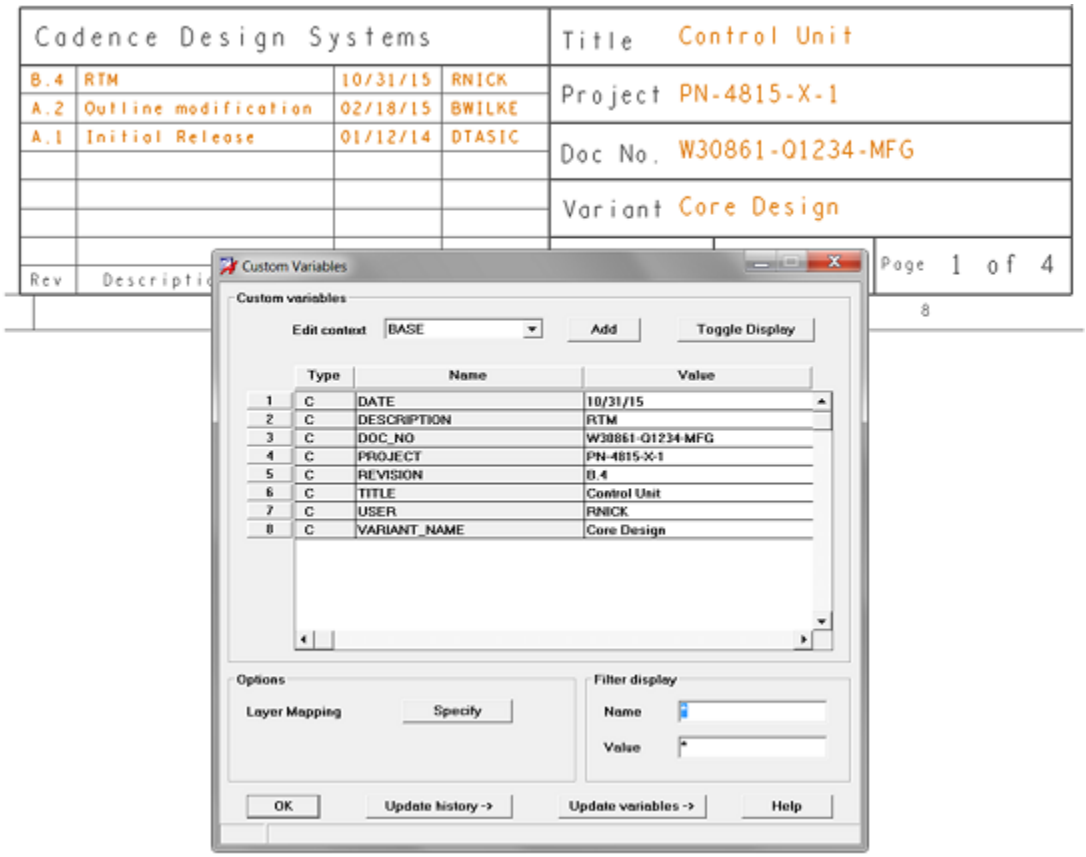


Custom Variables

Once a design is completed in PCB Editor, manufacturing data need to be created. Beyond Gerber and drill data, drawings for assembly, drill holes, and layer stackup have to be created. These drawings contain title blocks with meta data information such as Date, Part Number, Revision and so on.

Custom Variables is an application which allows you to define meta data (variables) and update them on the PCB drawing. Using system-defined variables you can control data fields, such as revision levels, ECO numbers, engineers, and PCB numbers. The application is also variant aware in that it allows to define variant specific overlays to title blocks.

Custom Variables has a history feature, which enables you to push current variables values to the corresponding history placeholder before updating the main variables.

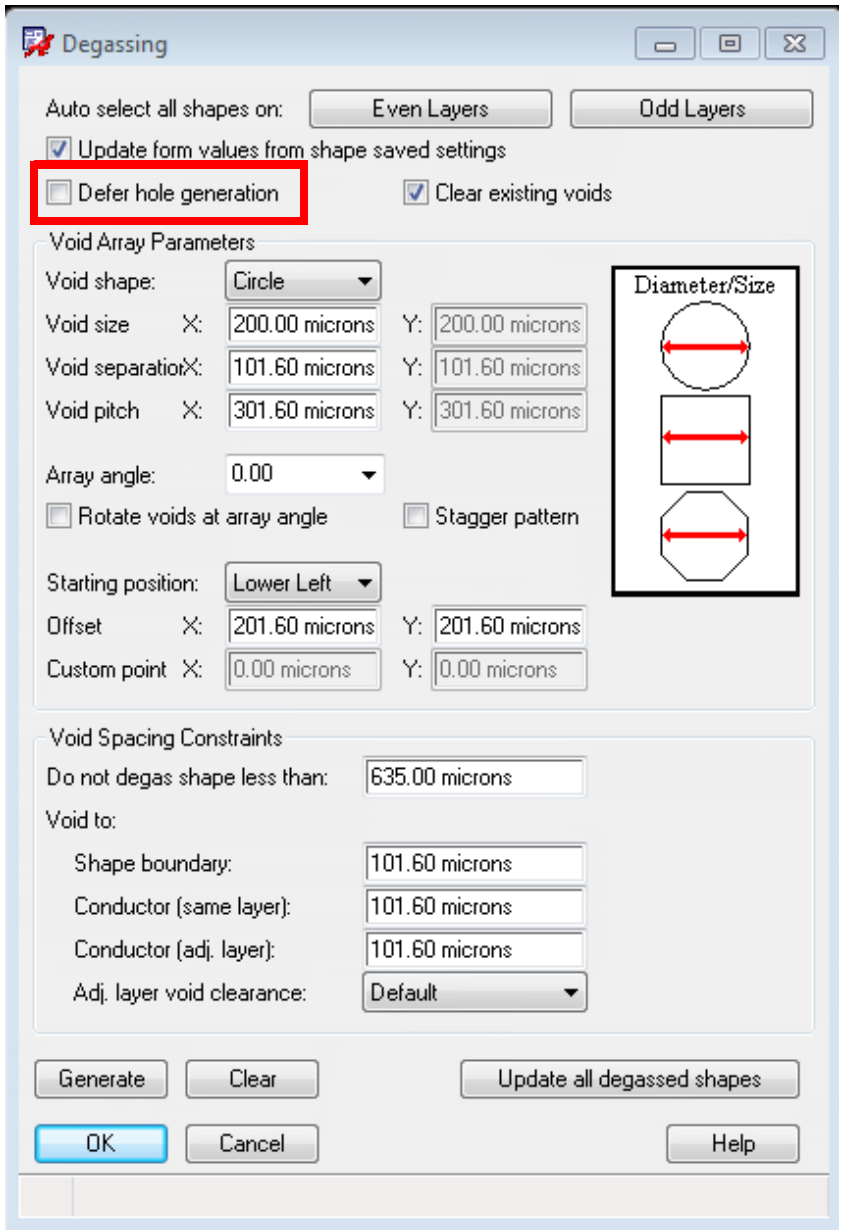


Cadence SiP Layout and Allegro Package Designer (APD)

This section describes the enhancements and new features in Cadence® SiP Layout and Allegro® Package Designer (APD) 17.2-2016 QIR 1.

Deferred Parametric Degassing

In continuation of the wafer-level packaging support and to improve productivity, the parametric degassing can now be deferred in the `degas` command (*Manufacture – Shape Degassing*) by selecting the *Defer hole generation option* in the Degassing dialog box.

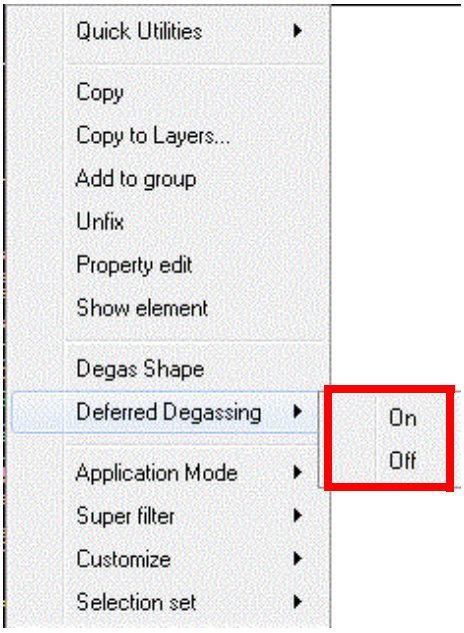


With emerging WLP and other very thin substrate formats, where manufacturing requirements are much more stringent, the degassing pattern is a very fine mesh with many

thousands to millions of holes. This causes database size and performance to degrade significantly.

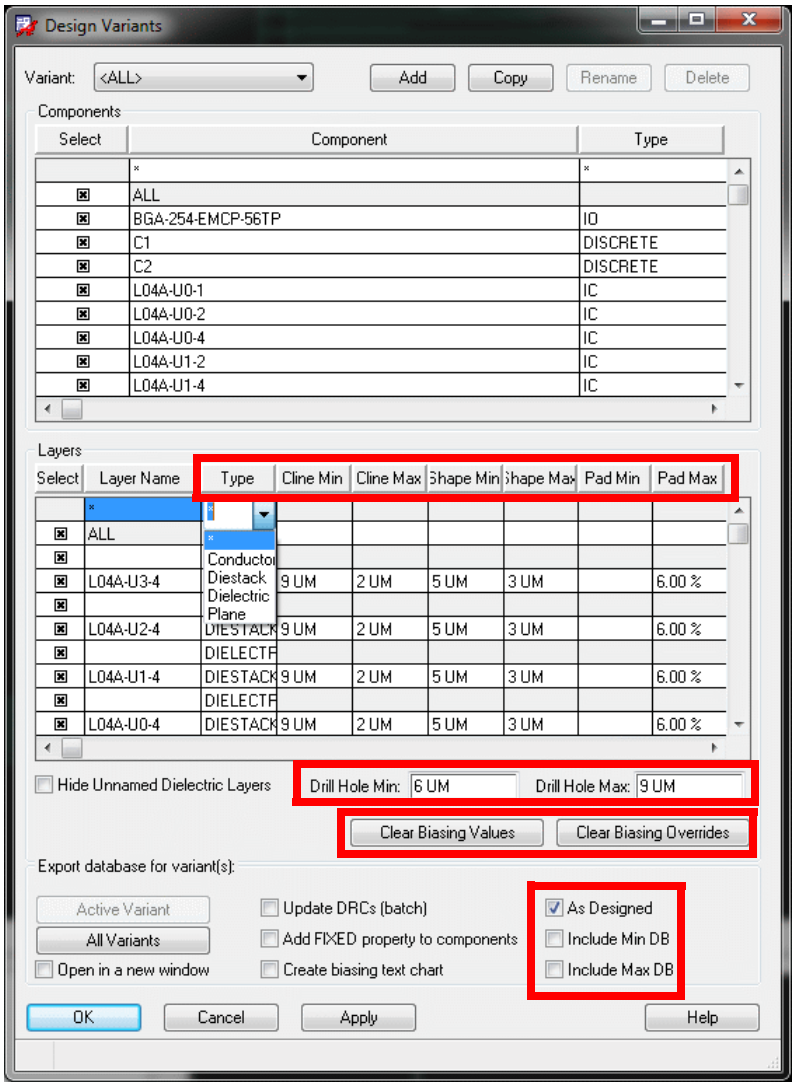
When you set *Defer hole generation*, degassing settings are recorded on the shape immediately, but the actual holes are cut only when they are needed for specific rule checks and for manufacturing output generation.

You can set deferred degassing *On* or *Off* from the pop-up menu of a shape in the Shape Edit application mode.



Biasing in Variant Design

You can now define biasing values based on manufacturing tolerances for the dimensions of different elements in the variant designs. The biasing values specified in the master design are inherited by all variants, but can be customized.



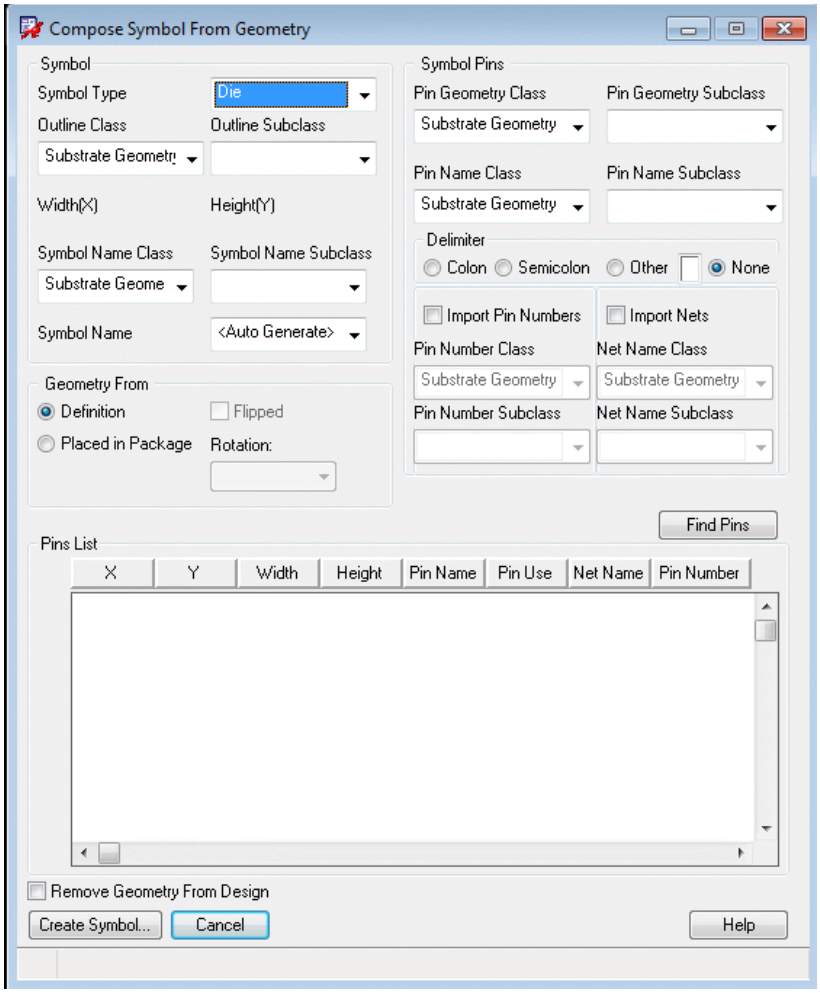
For each layer or group of layers, you can specify *Type*, *Cline Min*, *Cline Max*, *Shape Min*, *Shape Max*, *Pad Min*, and *Pad Max*. The values can be specified as percentage by adding the percentage symbol (`%`) to the value; for example, `6.00%`. Add a value to the All row to set all layers to that value. You can filter specific types of layers and apply the same value for all the selected layers, or enter values for each specific layer. You can also specify *Drill Hole*

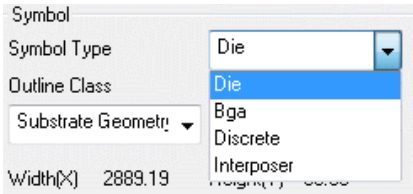
Min and *Drill Hole Max* values. You can clear all specified biasing values by clicking *Clear Biasing Values*, or clear overrides by clicking *Clear Biasing Overrides*.

While exporting the variants, you can choose *Include Min DB*, *Include Max DB*, or *As Designed*.

Compose Symbol from Geometry

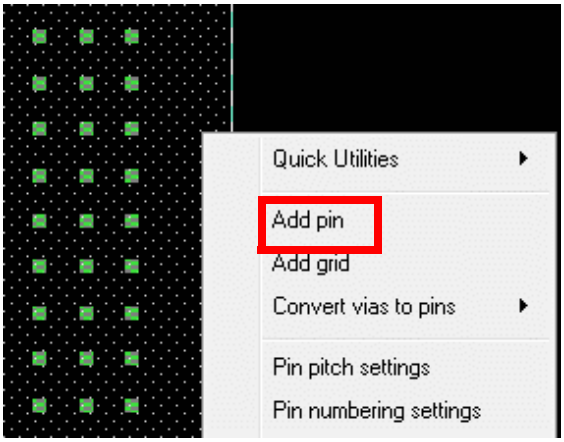
Compose from geometry extracts the necessary information from geometry data and creates a representative symbol of the type of component which includes all necessary information. You can use the enhanced and extended Compose Symbol From Geometry (*Add – Compose Symbol From Geometry*) feature to add die, BGA, discrete, and interposer (Only SiP Layout). This feature replaces and enhances the Compose Die from Geometry feature, which created only dies.



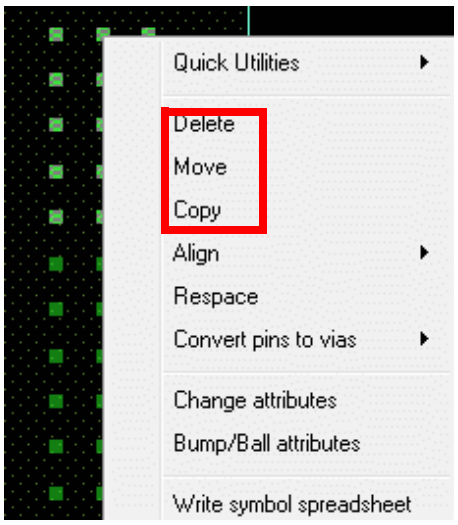


Co-Design Die Pin Operations

In addition to aligning and moving pins, you can now add, delete, and copy co-design die pins in the Symbol Edit application mode.



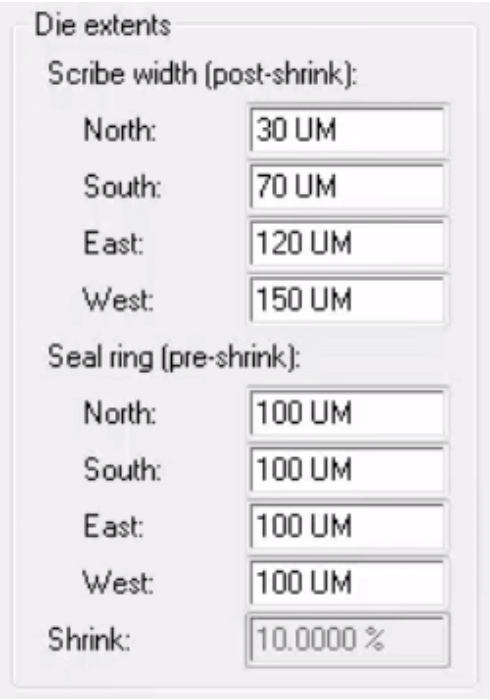
Symbols or Comps



Pins

Support for Seal-Ring, Scribe, and Die Shrink

The seal-ring, die shrink, and scribe values specified in the die abstract (`.xda`) file set the default values in SiP Layout when adding a co-design die. In the Symbol Edit application mode, choose *Die Properties* from the context menu of a die component to display and edit the seal-ring and die shrink values in the *Die extents* group.



Support for Probe Pin in Co-Design Dies

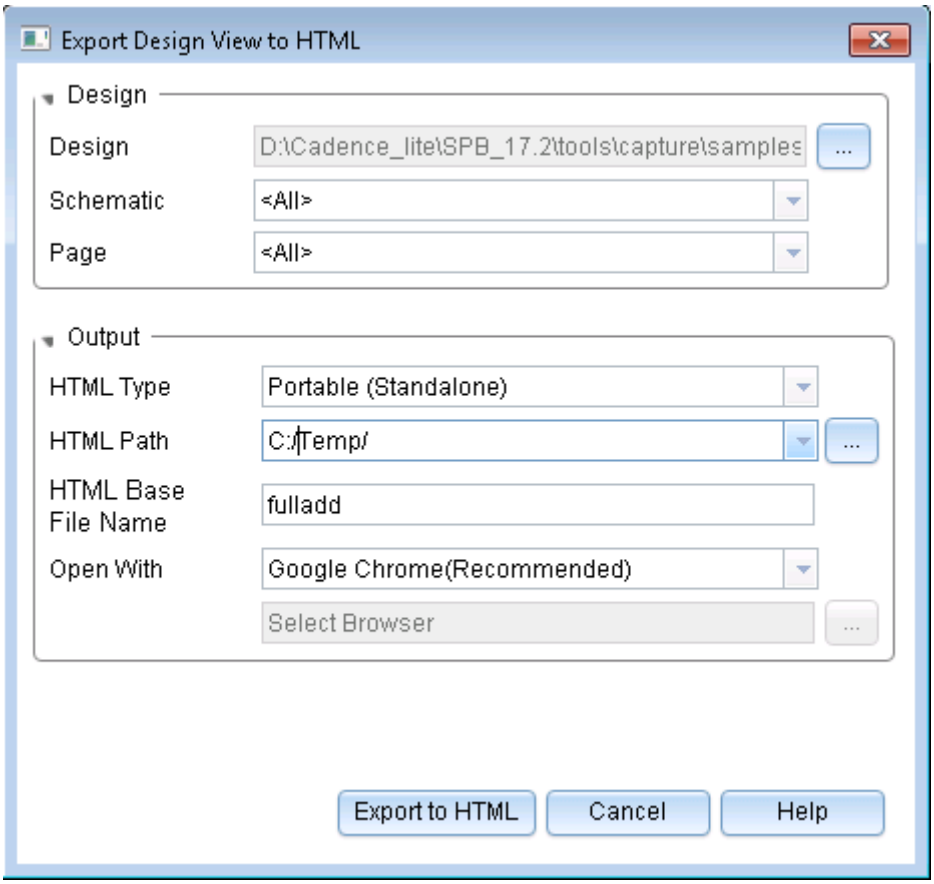
Probe pins, regions where probes can be used to test the finished product, are now supported for co-design dies. Probe pins are treated by the tools as any other pins and will support all properties that can be assigned to other pins. The probe pins will be part of reports and interfaces, such as component compare, as other pins.

OrCAD Capture

This section describes the enhancements and new features in OrCAD® Capture 17.2-2016 QIR 1.

Viewing Designs as HTML

You can now export your design to an HTML file and view it in any HTML browser. To export your design to HTML, choose *File – Export – Design HTML.*



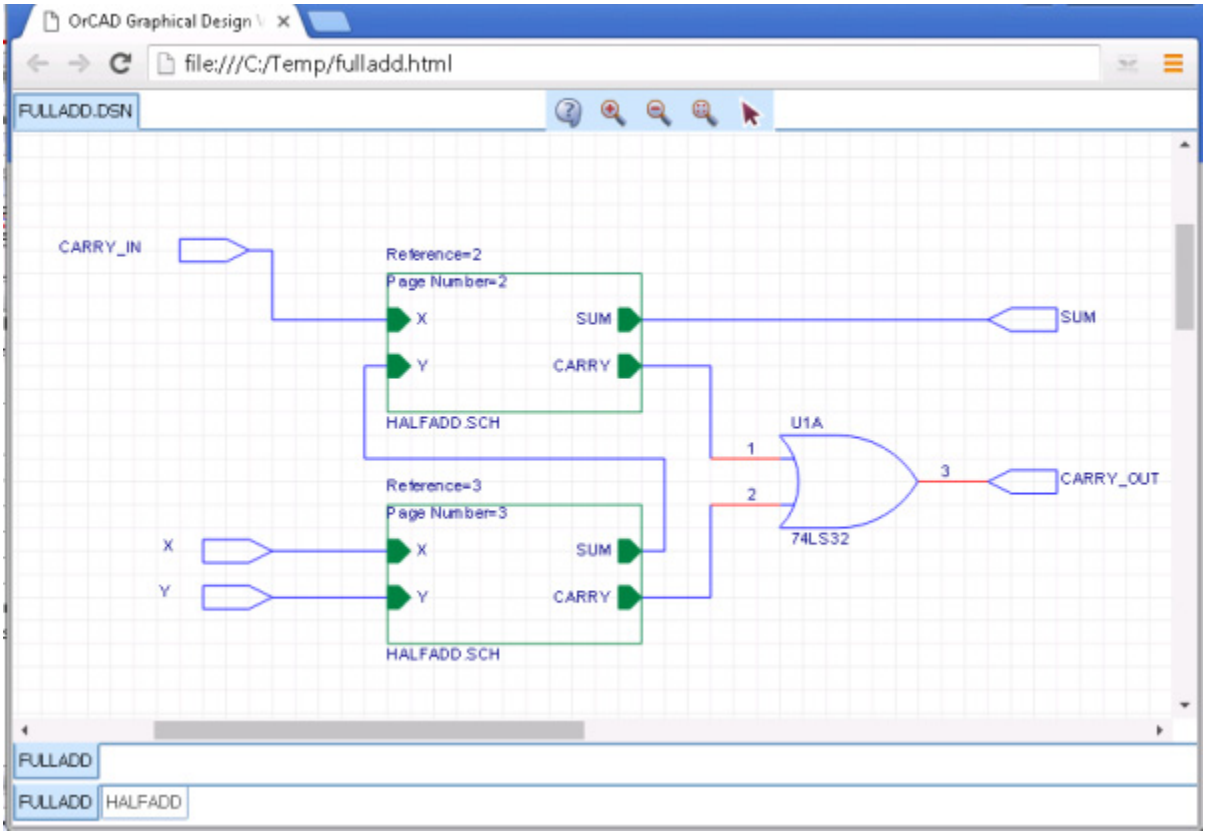
Click *Export to HTML* in the Export Design View to HTML window to open the design in the specified Internet browser.

Note: Google Chrome is the recommended browser.

You can export the complete design, or select a particular schematic or schematic page to be exported to HTML. The HTML file name follows the following syntax:
`<DesignName>[<-SchematicName>-<SchematicPageName>].html.`

You can generate either a lightweight HTML or a portable HTML. The lightweight HTML requires a Cadence hierarchy on the machine. The portable HTML, which requires more disk space than the lightweight HTML, does not require a Cadence hierarchy and can be launched from any machine.

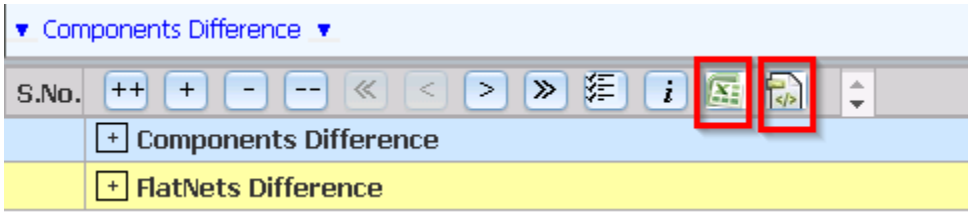
The following figure shows a design HTML file:



Saving Design Differences as HTML or Excel File

Now, you can save design differences as an HTML file (`.html`) or a Microsoft Excel file (`.xls`) by clicking the HTML or Excel icon as shown in the following figure. The files are saved in your default downloads folder.

The HTML and Excel icons are displayed in the Component Differences section of the Design Differences html file.



The following figure illustrates an example of design differences saved as an HTML file.

S.No.		FULLADD.DSN	BCD.DSN	Information
	Components Difference			Number of differences: 29
1	2	Present	Not Present	
2	3	Present	Not Present	
3	U1A[Occ:U1A]	Present	Not Present	
4	U3A[Occ:U3A,U3C]	Present	Not Present	
5	U2A[Occ:U2A,U2D]	Present	Not Present	
6	U3B[Occ:U3B,U3D]	Present	Not Present	
7	U2B[Occ:U2B,U4A]	Present	Not Present	
8	U2C[Occ:U2C,U4B]	Present	Not Present	
9	U1B[Occ:U1B,U1C]	Present	Not Present	
10	U30	Not Present	Present	
11	U31	Not Present	Present	
12	U32	Not Present	Present	
13	U33	Not Present	Present	

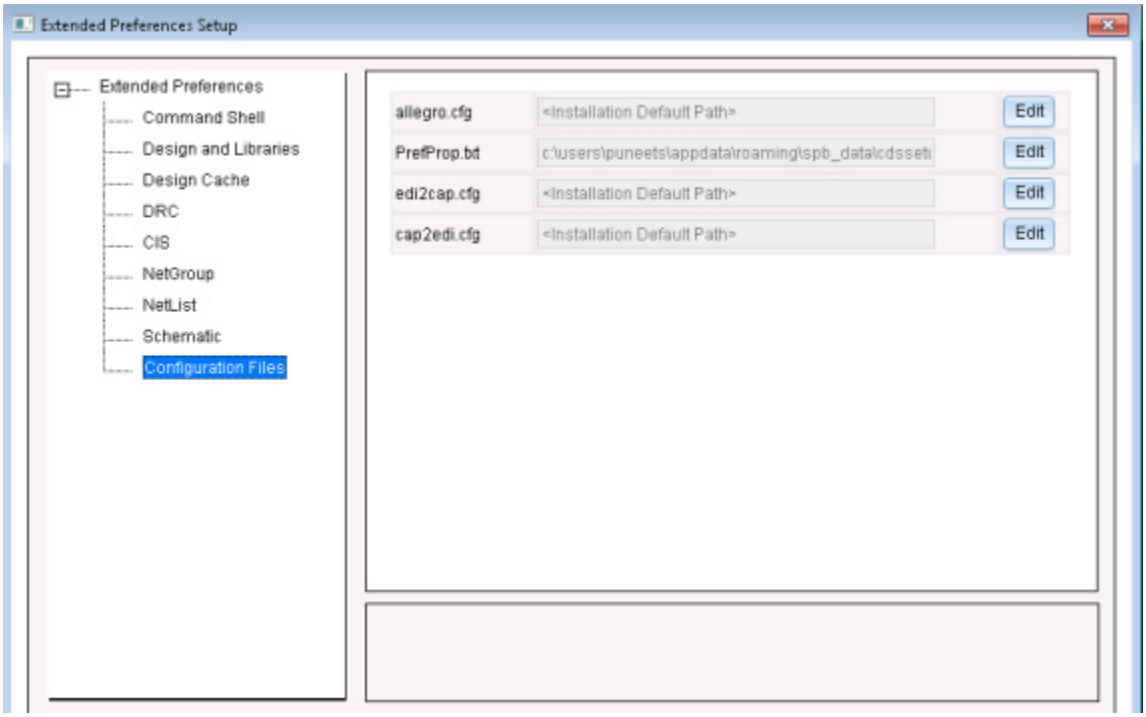
The following figure illustrates an example of design differences saved as an Excel file(.xls).

2					
3		Components Difference			Number of differences: 29
4	1	2	✓	✗	
5	2	3	✓	✗	
6	3	U1A[Occ:U1A]	✓	✗	
7	4	U3A[Occ:U3A,U3C]	✓	✗	
8	5	U2A[Occ:U2A,U2D]	✓	✗	
9	6	U3B[Occ:U3B,U3D]	✓	✗	
10	7	U2B[Occ:U2B,U4A]	✓	✗	
11	8	U2C[Occ:U2C,U4B]	✓	✗	
12	9	U1B[Occ:U1B,U1C]	✓	✗	
13	10	U30	✗	✓	
14	11	U31	✗	✓	
15	12	U32	✗	✓	

Customization Support for Design Configuration Files

You can modify the following configuration files from *Options – Preferences – More Preferences – Extended Preferences – Configured Files*:

- `Allegro.cfg`
- `PrefProp.txt`
- `edi2cap.cfg`
- `cap2edi.cfg`



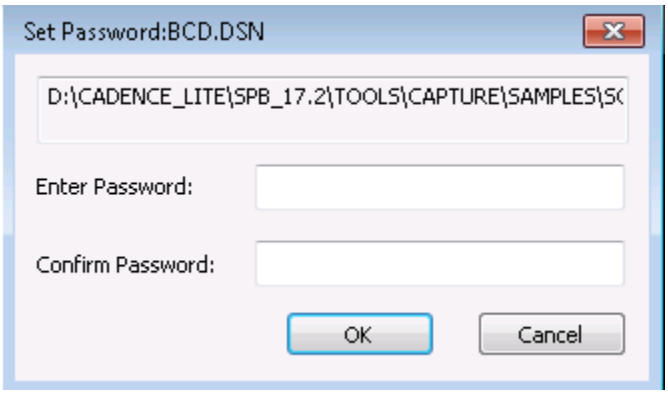
Any file selected for edit is saved to your home directory (`%HOME%`) and is read from the same path.

Protecting Capture Designs with Password

You can protect your designs by adding a case-sensitive password. You can then remove or modify the password.

Setting Password

Choose *Design – Set Password* to open the Set Password dialog box where you can specify a password. You can also select the design in the Project Manager window, right-click, and choose *Set Password* from the pop-up menu to open the Set Password dialog box.



You cannot open password protected designs in any earlier releases.

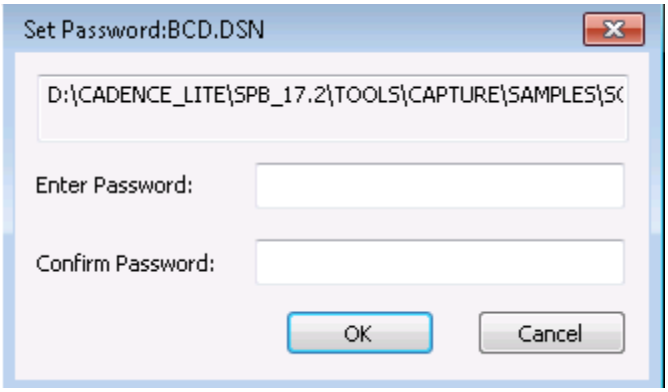
Note: There is no way to recover a design if you forget the password. Cadence cannot recover the design, or remove the password added to the design.

Removing Password

To remove password from a design, either choose *Design – Remove Password* or select the design in project Manager and choose *Remove Password* from the pop-up menu.

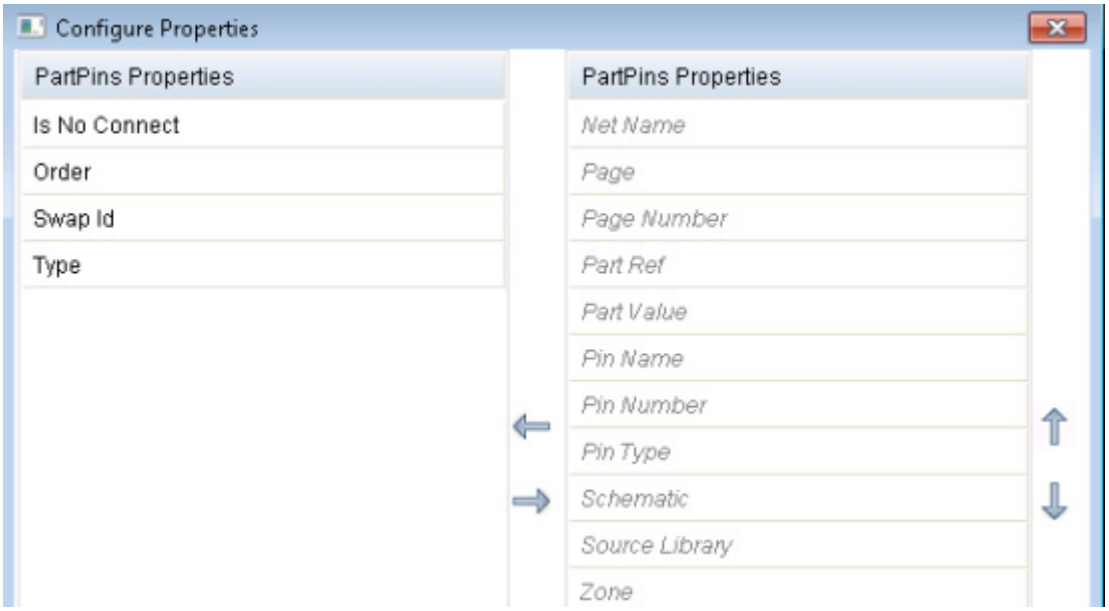
Changing Password

To change the password of a design, choose *Design – Change Password* to open the Set Password dialog box, where you can set the new password.



Configuring the Find Window Properties

You can configure the Find window using the *Configure Properties* window. Right-click in the Find window and choose Configure Properties to open this window.



As shown in the figure, the right side of the window displays those properties that are displayed in the Find Window. You can remove properties from this list by clicking the arrow pointing left. However, the default properties that are greyed out cannot be removed. You can select available properties in the left and click the right pointing arrow to add them to the list of properties to be displayed. You can also change the order in which properties are displayed by selecting the properties and clicking the up or down arrow.

Configuring the Browse Parts Window

Configure the Browse Parts window using the *Configure Properties* window. Right-click in the Browse Parts window and choose Configure Properties to open this window.

The right side of the window lists the properties that are displayed in the Browse Parts window. Select properties and click the left pointing arrow to remove them from the list. However, you cannot remove the default properties, which are greyed out.

You can select available properties from the left side and click the right pointing arrow to add them to the list of displayed properties.

You can define the order the non-default properties using the up and down arrows.

New Utilities Added in Capture

Following new utilities have been added in Capture:

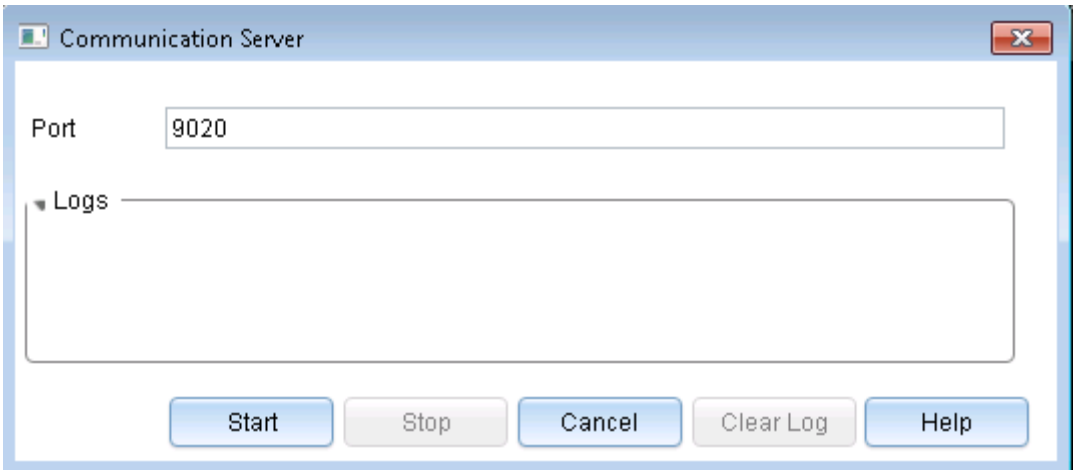
- Communication Server
- Replace Path in Design Cache
- Show All Open Libraries and Designs
- Customize Page (On Creation)
- Check/Correct Corrupt Library
- Find and Replace Text

Communication Server

This utility provides you an option to enable Capture as a communication server. You need to mention the port at which Capture will listen for server-client interactions.

You can enter a port number and start the server using the *Start* button. You can stop the server using the *Stop* button.

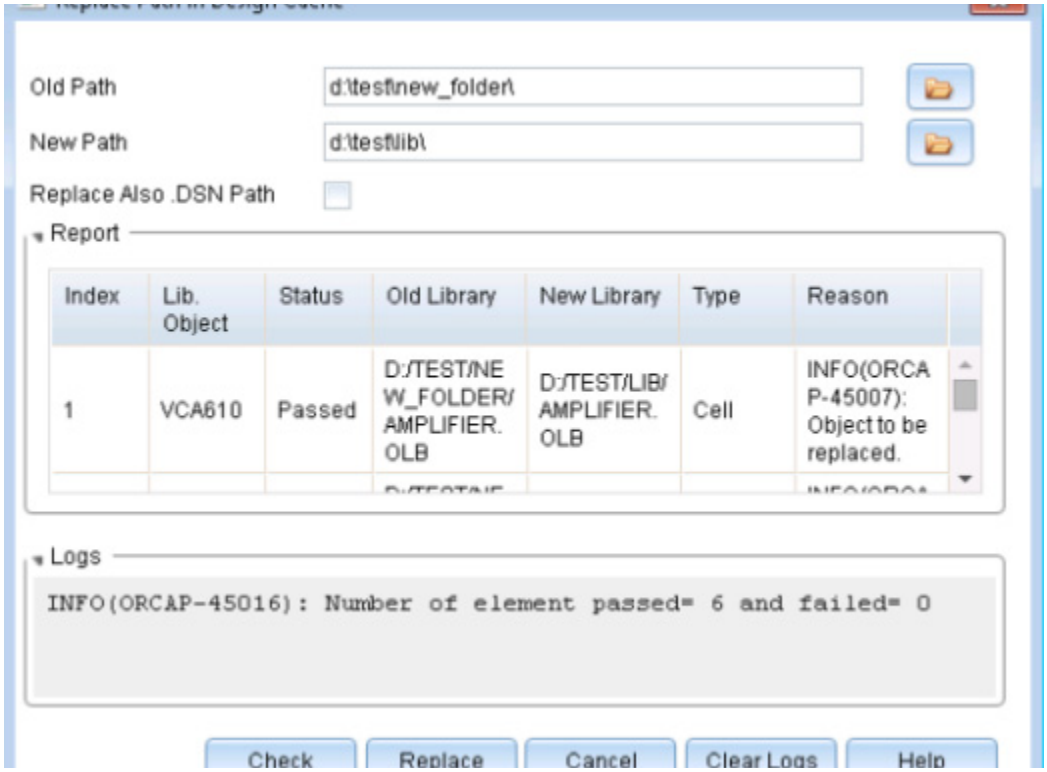
You can write your own server and client-side TCL methods and use this framework to establish a communication channel between Capture (server) and other applications (client).



For more details, see the *Utilities command* section in *Capture Reference Guide*.

Replace Path in Design Cache

This utility allows you to replace the path of all the old libraries used in a design with updated and new libraries. Using the *Check* button, you can verify if the same library parts are found in the new library and replace those library parts with the new parts available in the new library.



The Report section lists the parts that are replaced or are to be replaced with the new parts in the new library.

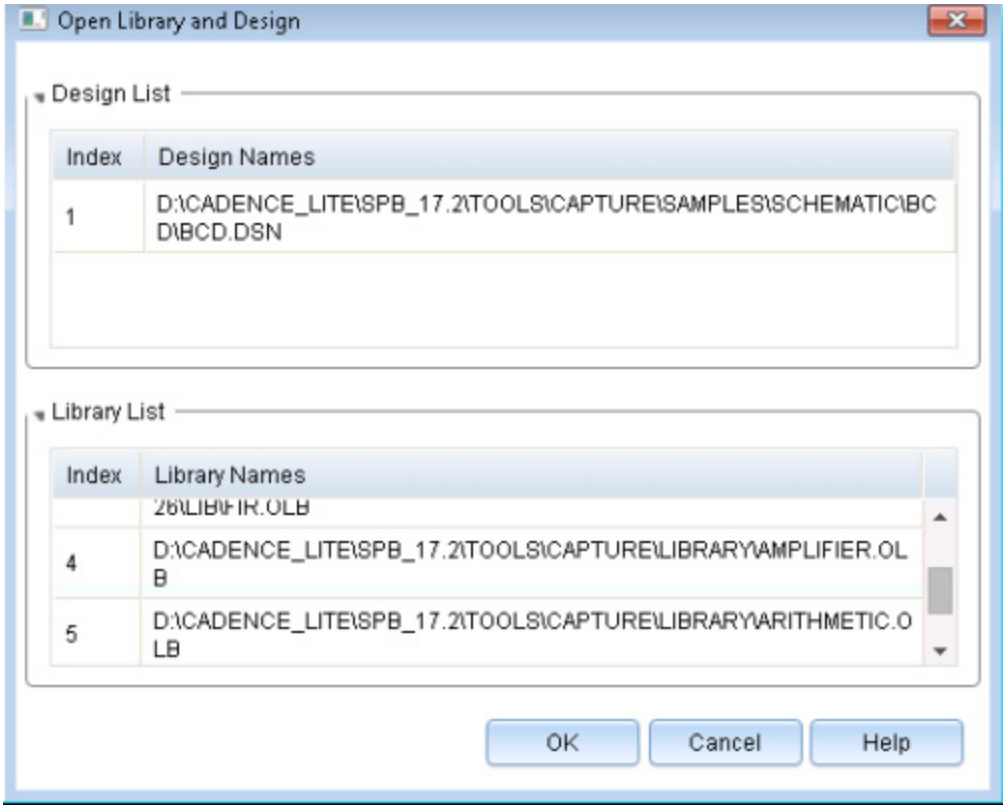
If no library parts are found in the new library path, the Replace Path in Design Cache window will not replace any parts.

You can also replace the design with a new design by selecting *Replace Also .DSN Path*.

Show All Open Libraries and Designs

This utility provides you option to view the designs and libraries opened in the current session of Capture. As you can see in the following figure *BCD.DSN* is currently opened in Capture.

Similarly, in the Library list section, you can see that libraries, such as *Amplifier.olb* and *Arithmetic.olb*, are open in the current session of Capture.

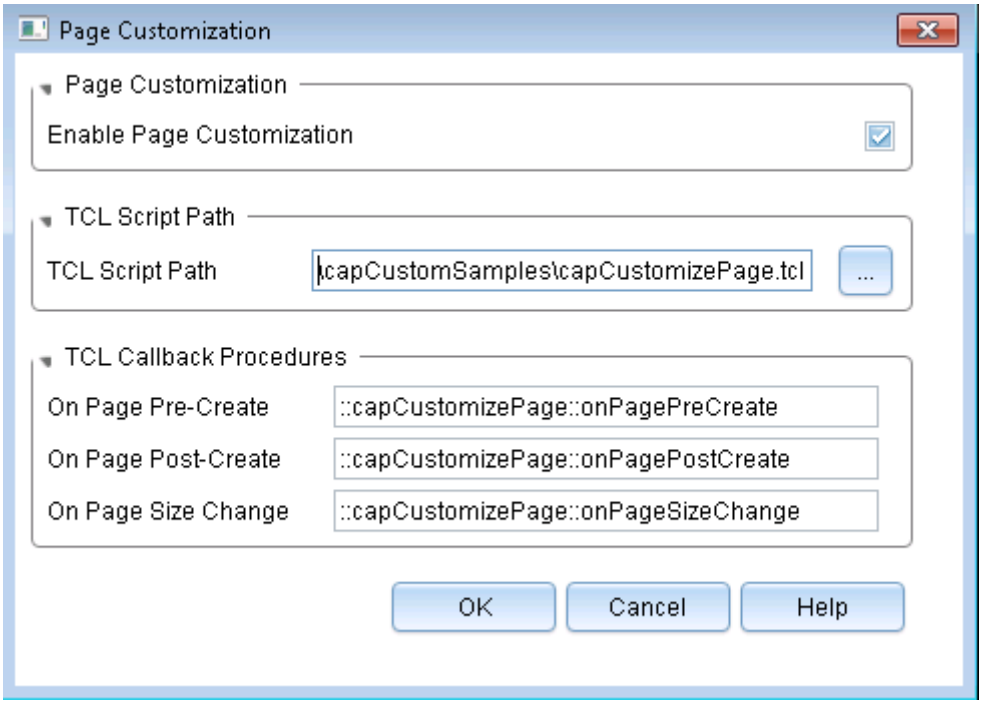


Select *Tools – Utilities – Show All Open Libraries and Designs* for the Open Library and Design window.

Customize Page (On Creation)

This utility allows you to customize the page creation and page size change process using different TCL procedures. The TCL procedures are called at the following instances:

- Before the page is created
- After the page is created
- When the page size changes



One or more TCL Callback Procedures field can be left empty if specific handle to any of these callbacks is not required. Once done, these options are saved in the Capture.ini file.

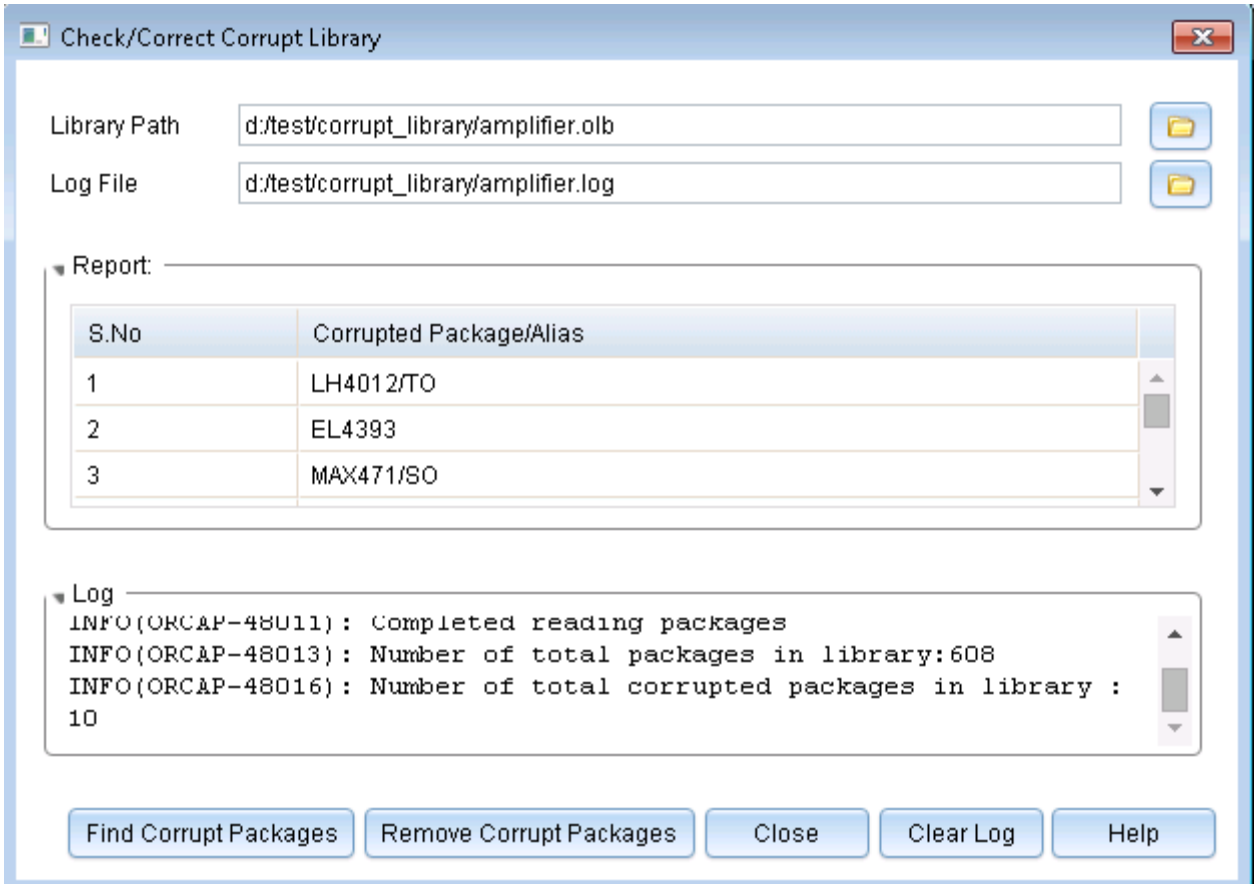
The default TCL script file that is used in the Page Customization window is available at the following path: `<installation path>/tools/capture/tclscripts/capCustomSamples/capCustomizePage.tcl`.

You can open the Page Customization window from *Tools – Utilities – Customize Page (On Creation)*.

Check/Correct Corrupt Library

This utility allows you to check and remove any corrupt packages in a library. Choose *Tools – Utilities – Check/Correct Corrupt Packages* to open this utility.

Click *Find Corrupt Packages* in the Check/Correct Corrupt Library window to display the corrupt packages in the Report section of the window. Click *Remove Corrupt Packages* to remove the listed corrupt packages.



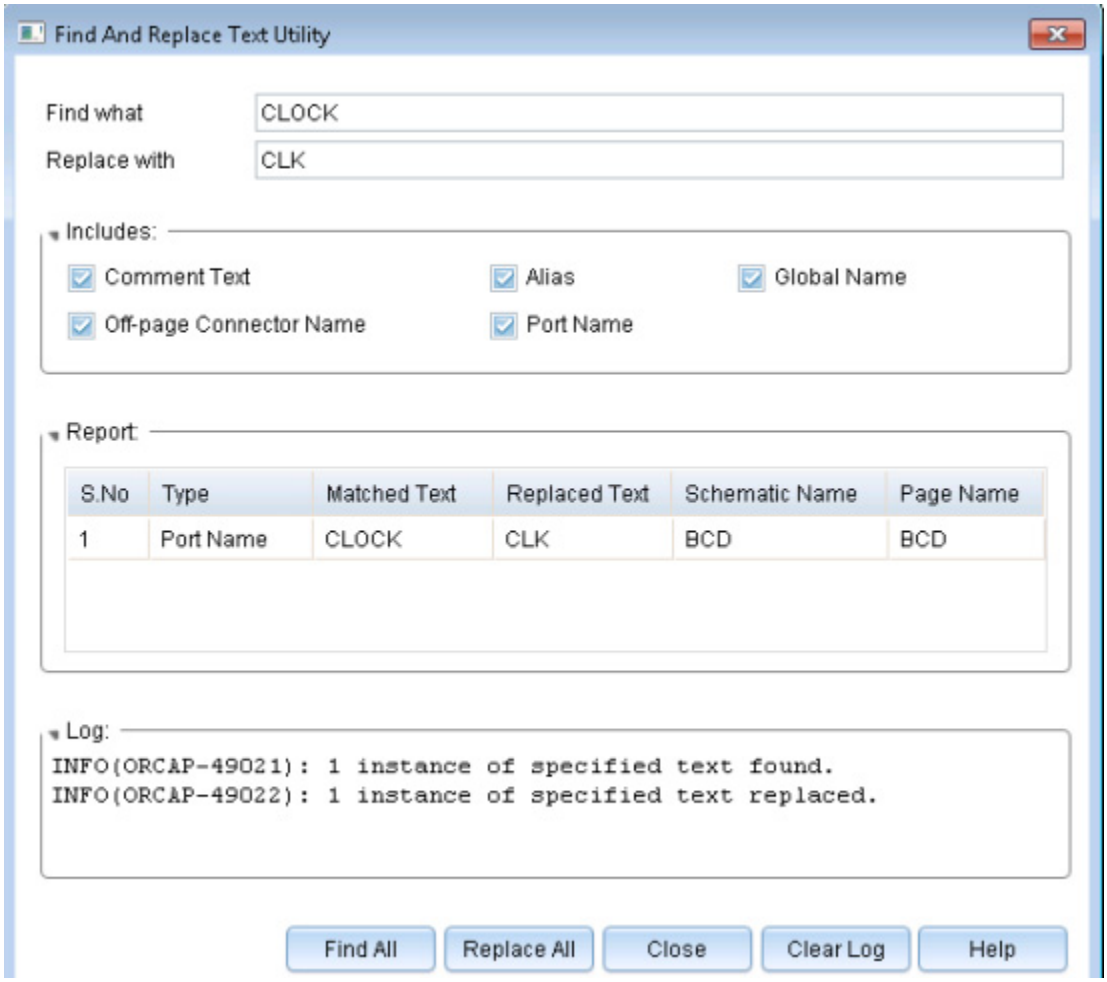
The Log section of the window displays success and failure messages.

Find and Replace Text

This utility allows you to find and replace one or more of the following types of text in a Capture design:

- Alias

- Global Name
- Port Name
- Comment Text
- Off-page Connector Name

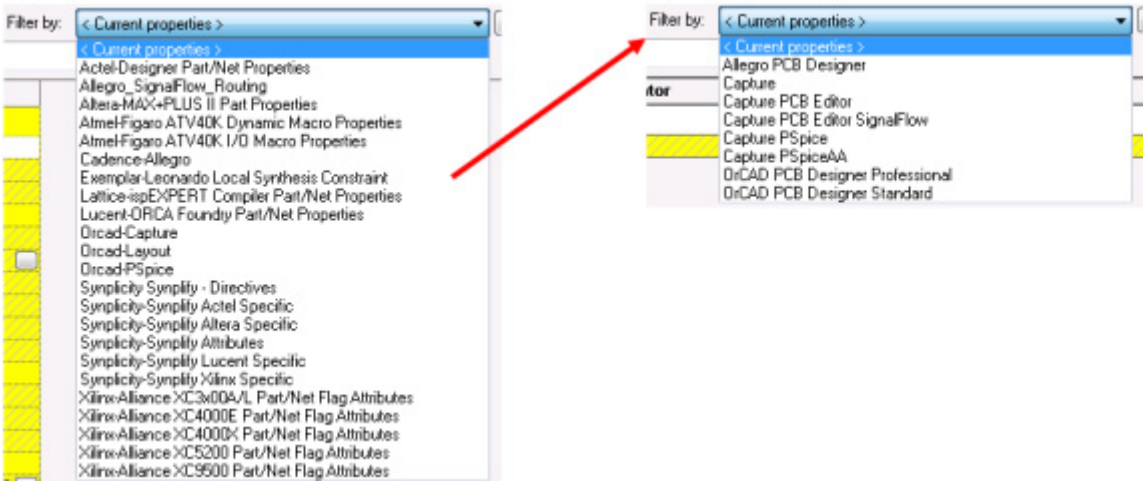


As you can see in the figure, a Port Name has been found and replaced in the design. The report section displays type, matched text, replaced text, schematic name, and page name related to the found and replaced Port Name.

Updated Property Editor Filter in the Properties Editor Window

A large number of filters were added to the Filter by field of the Property Editor window in 17.2-2016. An option has been added in this release to constrain the available properties. The updated limited filter options makes it easier to select the required filter as per the product or Capture's flow with other software.

The following figure illustrates an example of modified set of limited filters in the property editor filter for the Full Adder design. The right image shows full filters list and the left image shows the easier to use constrained filters.

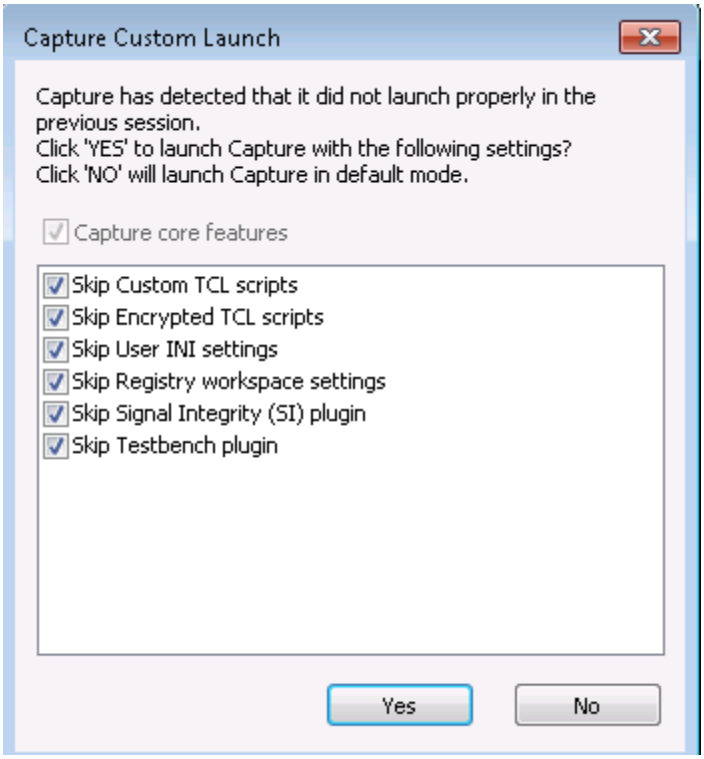


Capture Custom Launch

You can now relaunch Capture in a custom launch mode if Capture fails to launch. You can select different options to skip reading and initializing various settings and registry options in the next Capture launch for safety purpose.

Following are the options that you can skip for the custom launch:

- Custom TCL scripts that are initialized at the start
- Encrypted TCL scripts that are initialized at the start
- Reading the user INI settings
- Reading the registry workspace settings
- Reading the Signal Integrity plugin
- Reading Testbench plugin



You need to click *YES* to enable custom launch.

Note: The Capture Custom Launch window is displayed only if Capture fails to launch.

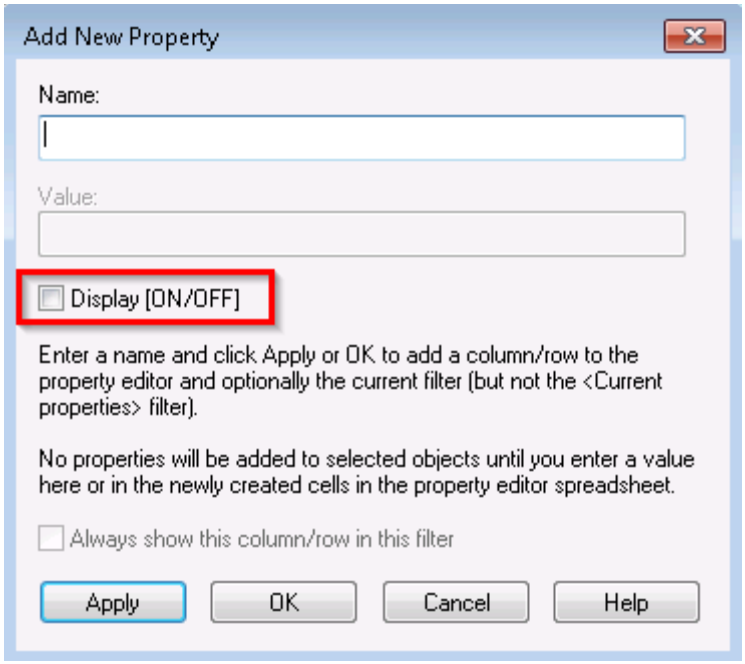
Miscellaneous Enhancements

Following are some of the miscellaneous enhancements in this release:

- Display Option in Add New Property Dialog
- Exclude Properties in a Design PDF
- Global DRC Settings
- New Select Folder Window
- Recovering from Unresponsive License Servers
- Using Cadence Default Library in CIS

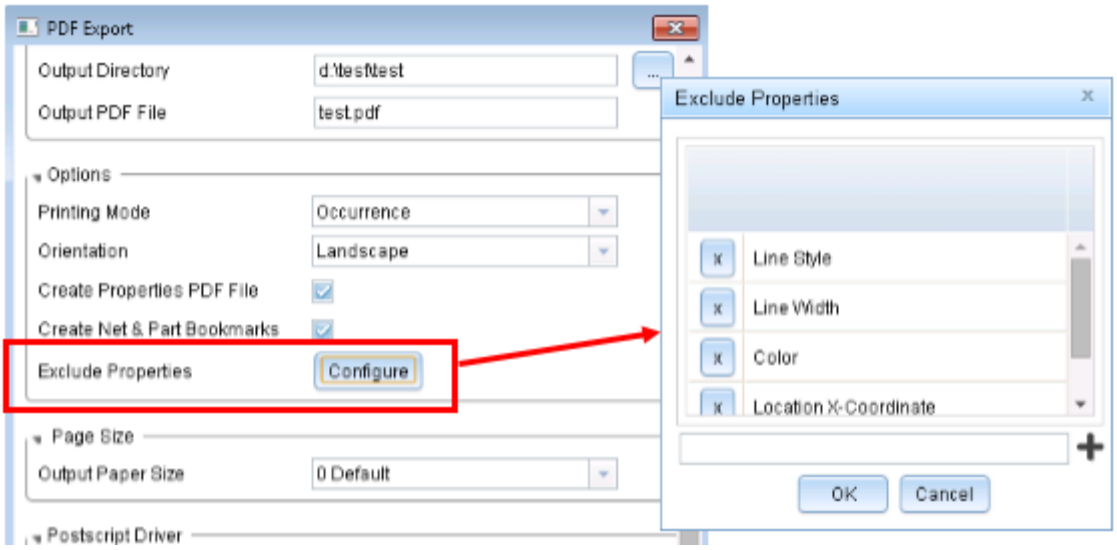
Display Option in Add New Property Dialog

A new option, *Display[ON/OFF]*, has been added in the Add New Property dialog box. If *Display* is selected, the Display Properties dialog opens on clicking *OK* where you can edit the display properties of a part during the part property definition process.



Exclude Properties in a Design PDF

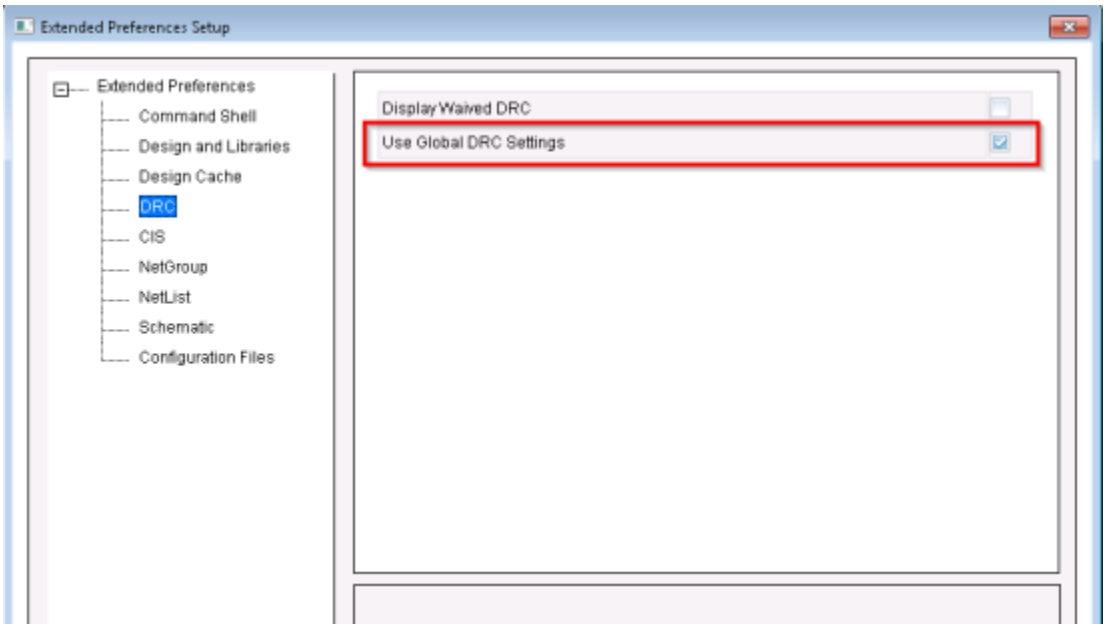
You can exclude all or a selected set of part properties from the design PDF using the *Exclude Properties* option in the PDF Export window.



To exclude any property in the design PDF, add the property in the Exclude Properties window and click *OK*. Once done, the part property will not be added to the design PDF.

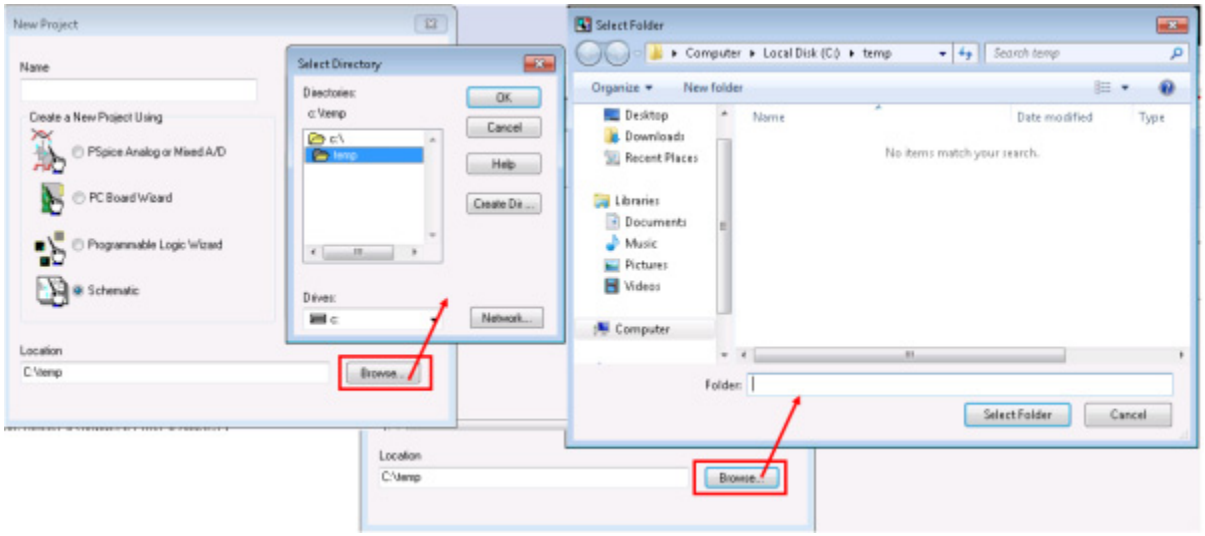
Global DRC Settings

A new option, *Use Global DRC Settings*, has been added in the DRC tab of the Extended Preferences Setup window. By enabling this option, same DRC settings can be used globally for different designs.



New Select Folder Window

The old Select Directory window has been replaced with the new Microsoft Explorer-style Select Folder window. You can now easily browse any location with a single click

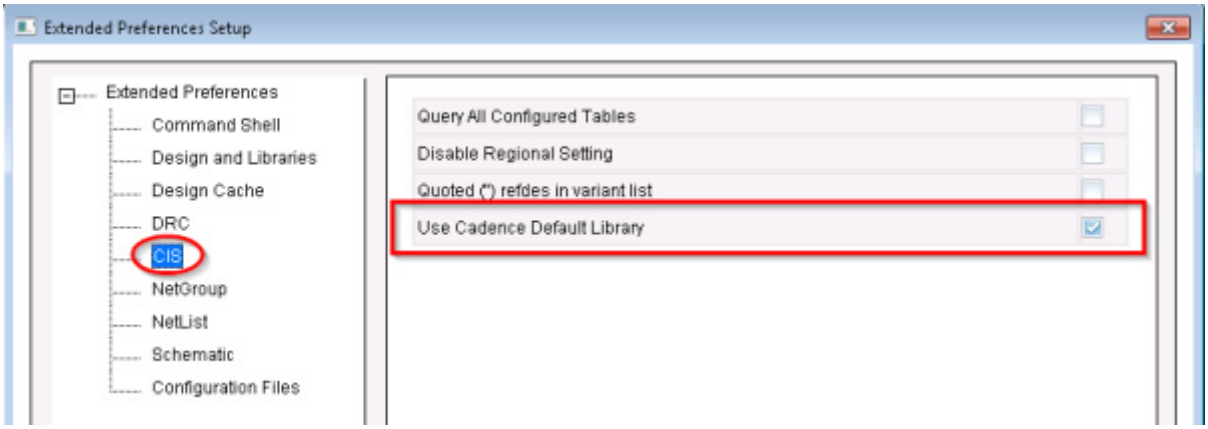


Recovering from Unresponsive License Servers

If there is no response from a license server, by default Capture makes three attempts before waiting indefinitely. Capture now prompts you with a message on the first instance of no response from the server. Click *No* to save the open designs and exit. Click Yes to retry to obtain a license.

Using Cadence Default Library in CIS

A new option, *Use Cadence Default Library,* has been added in the CIS section of the Extended Preferences window. Select this option to configure a CIS Database part from the default Cadence library location if the configured library location is not found.

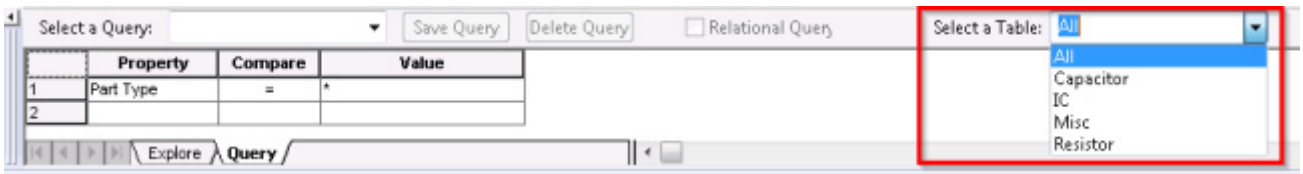


OrCAD Capture CIS

This section describes the new features and enhancements in OrCAD® Capture CIS 17.2-2016 QIR 1.

Updated Select a Table List

Now select CIS part table using the *Select a Table* list without enabling Relational Query.

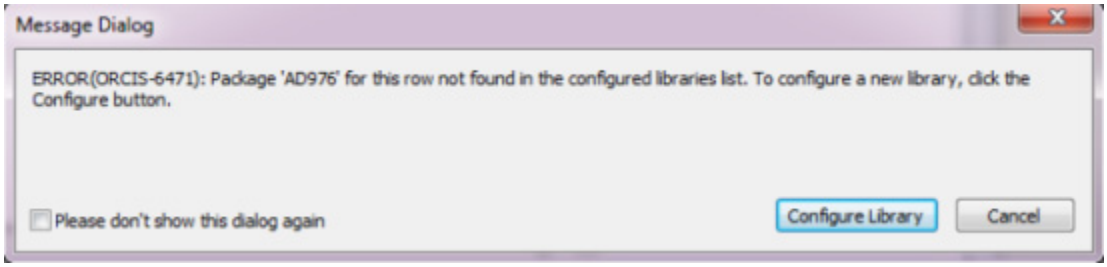


You can select all tables or any individual part table using the Select a Table list.

Configure Library in CIS Part Browser

You can now configure library by clicking *Configure Library* in Message Dialog, which is displayed if the selected CIS database part is not found in the present CIS configured library.

With this option, you can configure a database part and place the part in the design with one click instead of changing the Capture.ini settings.



PSpice

This section describes the following enhancement in PSpice® 17.2-2016 QIR 1.

Documentation Enhancements

The following documents have been added and updated with new content:

■ *PSpice TCL Command Reference*

Describes PSpice and PSpice Advanced Analysis TCL APIs in detail.

■ *PSpice TCL Sample Scripts*

Describes various sample scripts that you can use directly, or with minimum path changes, in PSpice and PSpice Advanced Analysis.

■ *PSpice Device and System Modeling with C/C++ and SystemC*

This document has been updated with the new content with respect to the following four types of PSpice DMI model simulation: Digital C/C++, Analog C/C++, VerilogA, and SystemC

Allegro Sigrity PI

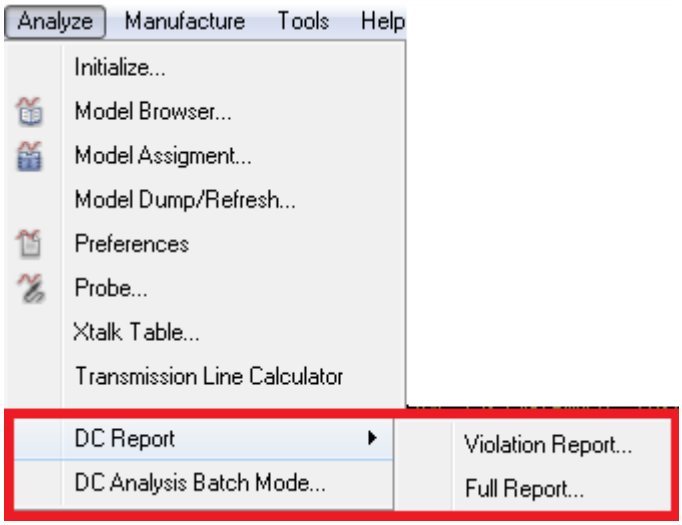
This section describes the new features and enhancements in Allegro® Sigrity™ 2016 products aligned with Cadence® Allegro® and OrCAD® products 17.2-2016 QIR 1.

DC Analysis Functionality Integrated in Allegro PCB Designer

The following DC Analysis functions have been integrated in Allegro PCB Designer with the High-Speed option:

- Displaying PowerDC analysis report in the Allegro environment
- Running DC analysis in batch mode

To load a PowerDC report in Allegro PCB Designer, no extra license is required. However, to run DC Analysis in batch mode, you need the Allegro Sigrity PI license.

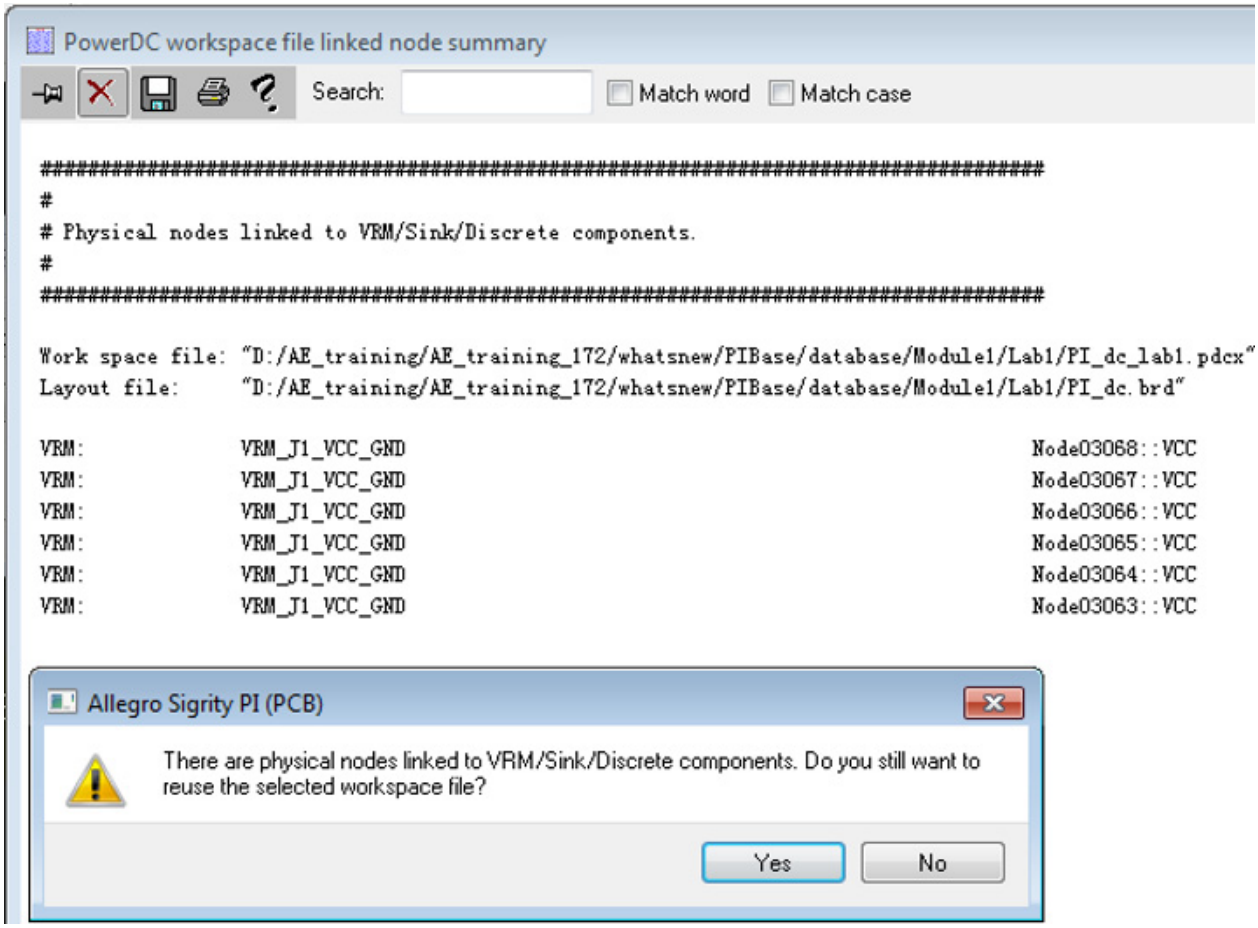


Workspace Reuse Check

In a PowerDC workspace, some physical nodes associated with VRMs/Sinks might not be reusable if changes are made to a shape, trace, or a via in the layout in the Allegro layout environment. This can lead to discrepancies between the updated layout and the original physical node names in the workspace when the design is loaded in the Sigrity environment.

A new check is introduced in this release that flags this situation as a warning if you continue to use the same workspace for DC setup:

There are physical nodes linked to VRM/Sink/Discrete components. Do you still want to reuse the selected workspace file?



Cross-Probing between PowerDC and Allegro Sigrity PI

A tighter integration between Power DC and Allegro Sigrity PI now lets you locate layout issues in Allegro Sigrity PI based on the results of the *E/T co-simulation* or *Thermal Analysis* in PowerDC.

When you launch PowerDC from Allegro Sigrity PI from the *Analyze – PowerDC* menu command, the two application windows (Allegro Sigrity PI and PowerDC) open side by side. When you zoom in or out in one window, the other window automatically syncs up. Similarly, switching layers in one window automatically switches layers in the other.