PADS Professional Release Highlights

Software Version PADS Professional VX.2

August 2016

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Introduction

Built for the independent, multi-discipline hardware engineer who does it all, PADS Professional utilizes Xpedition® technology that can handle the most demanding and complex designs, where other solutions fail.

PADS Professional is powerful, but it's also easy to learn, use, and afford. It's designed to give the experienced user all the horsepower they need, yet intuitive, so casual or occasional users can accelerate their time to productivity.

The full flow of PADS Professional enables you to design, validate and manufacture PCB-centric systems incorporating advanced FPGA devices.

New Products and Features

New Product Options

PADS Professional Multi-Trace HSD Option (Part Number 268117)

Provides additional functionality for the definition, routing and tuning of nets with high speed constraints:

- Select an individual net or group of nets and auto-tune
- Support for Spacers
- Additional reports for batch analysis
- Longest to Shortest Nets
- Nets over Splits
- Coupling by Spacer
- Coupling by Parallelism Factor
- Additional Online Hazard Explorer support for
- Advanced Topology Balancing
- Advanced Topology Mismatch
- Min/Max TOF Delay
- Matched TOF Delay

- Delay Formulas
- Parallelism
- Estimated Crosstalk
- Rise Time is now enabled in Setup Parameters

PADS FloTHERM XT (Part Number 265952)

3D computational fluid dynamic (CFD) solution that supports steady state and transient analysis. Allows electrical/hardware engineers to perform thermal analysis much earlier in the design cycle. Easily import mechanical objects such as product enclosures and heat sinks.

Schematic Capture

OrCAD Netlist

PADS Professional layout can now be front-ended by OrCAD schematic. Forward and back annotation of design changes is fully supported.

PADS Standard/PADS Standard Plus

The configuration of xDX Designer that is delivered with PADS standard and PADS Standard Plus can now be used to front-end and create PADS Professional Layout projects.

Constraint Manager

Constraint Manager now supports add delay, crosstalk and parallelism rules for electrical nets.

Layout

- “Send to LineSim” command is permanently enabled when either a pin, trace segment, complete net or Netline is selected
- Auto Test Point Assignment
-
- Integrated support for Back Drill
- Non Functional Pad removal

- Placement alignment
    - Spread Part
    - General alignment of board objects
    - Snap align
- Copy Circuit Part Number renumber mapping
- Hazards Explorer
- Tabbed Routing
- Net Shorting
- Net Explorer Filter and Color control
- New via types
    - Laser and Photo via types in Padstack Editor
    - Laser and Photo via types in Drill
    - Laser and Photo via types in ODB++
    - Support for Rectangular via in Padstack Editor
- Improved Graphics performance
- Improved Graphics Alpha transparency
- Dimensioning improvements
    - Additional object selection, such as pad edges and arcs
    - Edit placed dimensions
    - GD&T enhancements include move leader, copy stand-alone leaders/FCF's and explicit enclosure size
- Drawing improvements
    - Additional Line Styles
    - WYSIWYG pattern fill patterns for polygons
    - Vector fonts for MentorGDT and MentorSTD
    - Drawing Editor - Place Edit Tables from CSV
    - Drawing Editor - Library Integrity Updates (Enable Compare Local to Central Library, Verify Cell Instance Changes, ECO Reset Cell)

    - Drawing Editor - Copy Sheet Enhancements (prefix, suffix, naming, multi-selection, workspace enabled)

- Layer Stackup improvements
    - Layer Stackup Import from file
    - Multiple Dielectric layers
    - Buildup and Core Layers
    - Sync with Valor NPI Stackup definition for ODB++ output
    - Increase number of User Layers
    - ODB++ support for Layer Stackup improvements

3D

There are general improvements in the 3D design capabilities:

- Automated Bulk model assignment
- Create board outline from STEP
- Surface mating
- Model Assignment / Mapping / Alignment reuse
- Integrated Model Generator flow
- Export metal on top and bottom of board within STEP

RF Design

There significant improvements in several areas of RF design:

- AWR Integration
- AWR RF Via use case
- Mapping one to many objects during import
- Meander improvements
- UI for GND Net and Layer mapping
- Unification UI of RF Parameters in both xDX Designer and PADS Professional layout

Automation

User defined Automation scripts with UI interaction is now supported.

xDX Designer

There are several ease of use improvements and new functionality for the VX.2 release.

- **Windows Layout**
  - There are three layout options delivered that provide increased visibility for Toolbars, Icons, data panes and window layouts as your expertise level increases
    - Default - provides simplified toolbars and windows for basic use
    - Classic - provides even more tool access and additional window navigation controls
    - Symbol Edit – provides access to those most commonly used commands while in the embedded symbol editor
  - Customization is also supported so that users can define and save their own schemes
- **Part Search/Replace**
  - Smart, Google like search across design, libraries and xDX Databook.
  - Replace utilizes the Part Search function, wizard to step through the process.
- **In Line block Editing**
  - Simplified block creation process. Place block by name immediately. Add, delete move, rename pins and rename nets (keep pin names), change pin type.
- **Cross Referencing**
  - Replacement for SCOUT. Supports hierarchy and Xref annotations, uses border zone information and no need to close schematic to run.
- **Color by Net**
  - Capability to color nets and apply across the design with switchable visibility.
- **Embedded Symbol Editor**
  - Developed using PADS DX Designer. Identical look and feel, same settings, Fonts, Grids, Layered Graphics and Color Schemes etc.
  - Same editor engine, all DX Designer functionality inherited: grab handles, Group/Ungroup, Smart shapes etc.

HyperLynx SI/PI/Thermal 9.4

New Signal Integrity Support for Rigid-Flex Designs

Rigid-flex designs pose a unique signal integrity simulation challenge in that the board stackup changes in different areas of the design. As such, HyperLynx has been enhanced to allow for multiple stackups in different areas of the board.

Multiple Stackups Mode

By default, HyperLynx assumes a single stackup for the board. In HyperLynx v9.4, users have the ability to check a selection in the stackup menu to "Enable Multiple Stackups". This enables the Stackup Manager which is used to manage the multiple stackups as well as the Add Stackup Area capability.

Stackup Manager

The new Stackup Manager lists all the stackups in the design, allows addition of new stackups, deleting stackups, and editing stackups. When editing a stackup the existing Stackup Editor is launched from the Stackup Manager to make edits. The Stackup Manager also includes a preview showing all the stackups in the design side by side.

Stackup Areas

The stackup areas define outlines of different areas of the board with unique stackups. These areas can be set up as rectangles or complex polygons, and their vertices are completely editable if desired. You can define these areas directly in HyperLynx, and they can also be imported from Xpedition.

Integration with Xpedition Specific to Rigid-Flex designs

Any design being exported from Xpedition VX.2 to HyperLynx v9.4 (through the default .cce analysis export) will include all relevant rigid/flex design data, including the stackup areas (multiple outlines) and multiple stackup definitions. When such a design is imported into HyperLynx the "Multiple Stackups" mode will be automatically enabled to support this design data.

Other New Signal Integrity Features

Component Model Symbol

The new Component model symbol in LineSim allows for much neater schematics when dealing with schematics with a lot of drivers and receivers. Drivers and receivers on the same component can be grouped together in the Component model symbol.

IPC-2581 File Import

Another PCB output file format, IPC-2581, can now be imported into BoardSim.

New Reports for Generic Batch

In HyperLynx v9.4, Generic Batch simulation adds new HTML-formatted reports, similar to those that were introduced in v9.3 in the DDRx Wizard. The new batch-analysis reports have multiple pages - a Summary page and subsequent pages with details on the individual analyses in the simulations.

ODT Sweeps in DDRx Wizard in LineSim

The ability to sweep on-die termination (ODT) settings in the DDRx Wizard has been added to LineSim in HyperLynx v9.4. Users can set up a series of different ODT settings for the Wizard to sweep through when running the analysis. The settings will include the device, signal group, and ODT status.

New SERDES and 3D-Electromagnetic Features

Automated Support for Series Passive Components in 3D Areas

The 3D Area capability in BoardSim has been enhanced in HyperLynx v9.4 to include better support for series passives, especially DC blocking caps on SERDES links. When a 3D area including a discrete component is created, the ports are adjusted automatically to include the circuit model of the passive in the solved S-parameter model of the entire structure.

New Power Integrity Features

New Reports for DC Drop

In HyperLynx v9.4, DC Drop simulation adds new HTML-formatted reports, similar to those that were introduced in v9.3 in the DDRx Wizard. The new batch-analysis reports have multiple pages - a Summary page and subsequent pages with details on the individual nets analyzed. The reports will have the same data as the old text reports, organized into tables for easier viewing.

Advanced Decoupling Analysis Down to 10KHz

The simulation engine used by Advanced Decoupling Analysis has been enhanced in HyperLynx v9.4 to support accurate AC analysis down to 10KHz.

Loop Inductance Report from Advanced Decoupling Wizard

The Advanced Decoupling Wizard now has the option to output a loop inductance report which details the quality of the connection of the IC pins to the PDN. This report is generated in HTML format.

New Decoupling Capacitor Model Libraries

The HyperLynx v9.4 installation now features a library of models for common capacitor types. These are available in the LIBS directory in the install.

GUI Improvements

Improved Panning Capability

In HyperLynx v9.4, users can now pan in BoardSim and LineSim by holding down the middle mouse button and moving the mouse in the desired direction of panning. The same panning and zooming scheme is used in the board viewer, schematic editor, PDN editor, and DC Drop board viewer.

New Measure Feature in BoardSim

A new feature has been added to the board viewer to allow users to measure between two objects. A crosshair is snapped to a specific location and the cursor moved to measure distances to other objects. This feature works in conjunction with the new panning capability to facilitate measuring large distances on a board.

HyperLynx DRC 6.3

Analysis Client Control

One of the most significant enhancements is that you can run HyperLynx DRC rules from within the PADS Professional Layout user interface by using the Analysis Control add-in. HyperLynx DRC reads design data from PADS Professional Layout, constraint data from Constraint Manager, and writes detailed rule violation locations to the PADS Professional Layout board viewer. When rule checking is complete, you can use Analysis Control to select the violations to display in the PADS Professional Layout board viewer.

Note: Analysis Control in HyperLynx DRC v6.3 is only compatible with Xpedition PADS Professional Layout from VX.2 and both software installs must be either 32-bit or 64-bit, cross installations are not supported.

Usability Improvements

- New Welcome screen
  - Quick access to the user manuals, tutorials, reference guides, recent projects and more
- Better organized object lists branch
  - Separate “classifying” object lists from others
- Layout data grouping for easy and quick access

- Quick finding in Project Explorer (Windows Explorer style)
    - Quickly type a sequence of letters to find and select an object
- Glob (wildcard) filtering condition in addition to regular expression

Broader Data Type Support

- New: support IPC2581 design format
- Improved: ODB++
- New Constraint Classes branch
    - Full hierarchy is available via GUI and AOM

Enhanced Rules

- All rule documents now list both English and Metric default values
- Impedance and Differential Impedance
    - Eliminate false violation around anti-pad areas if “IgnoreViaConnections” is set to yes
- Long Stub
    - Eliminate false violation in area fill areas in certain specific cases
- Net Crossing Gap
    - Now support constant traces in addition to planes and area fills
- Metal Island
    - More accurate to detect violation areas requiring additional vias
- Edge Shield
    - Now a through hole pin is considered as a stitching component
- Termination Check
    - Now support differential pairs

- Vertical Reference Plane Change
    - Better stripline and dual-stripline supports
    - Improved anti-pad recognition
    - Covering reference plane change related to serial discrete components that use via-in-pad
    - Split out Signal Supply check
    - Various bug fixes

Better Integration and Platform Support

- Linux support
    - Console Mode only
        - 32 and 64 bit
        - RedHat Enterprise Linux 6 (through update 7)
        - RedHat Enterprise Linux 7 (through update 2)
        - CentOS 6.6
        - SuSE Linux Enterprise 11 - (update 2 & 3 only) (Enterprise, desktop and server editions)
- Windows console mode
- Integration with PADS Professional Hazards Explorer

HyperLynx DRC Debugger Usability Enhancements

- Object Browser
    - Easy access to HLDRC AOM objects, their properties and methods
    - Add references to external type libraries for developing rules driving external applications (Xpedition, SI/PI, MS Excel, etc.)
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    - Easy access to HLDRC AOM objects, their properties and methods
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- Prefix Manager and intelliSense

- Easy coding and AOM insertion

AOM Enhancements

- New graph engine (apply powerful methods of graph theory on PCB designs and easy write powerful rules as length matching, connectivity walking, maze algorithm, path finding etc.)
  - Available through HLDRC AOM
    - GraphEngine, Graph, GraphEdge, GraphNode, GraphShortestPath
  - Allow to use various graph theory methods on layout designs
    - Shortest path, depth first search, breadth first search, …
  - Some predefined graphs are available
    - Connectivity graph built-in for connectivity building
    - Topology graph for electrical and physical nets
  - Other types of graphs can be created as needed
- Electrical Net: NamedByUser, Clock, LowPower, NetClass, RadiationClass, SusceptibilityClass, Analog, Noisy, Sensitive, SetName, SetVoltage, SetFrequency, SetSwitchFrequency, SetKneeFrequency, GetPinsByType, GetCouplingNetCapacitance, GetCouplingNetInductance
- Component: SetType;\, AssignModelBy, ModelByType, ModelBy
- Cross Section: FieldSolverIgnore, IsFieldSolverIgnored
- Geometry Engine: DistanceEx
- Pin: PackageDelay, PackageLength
- TransLine: RefUpperObjects, RefLowerObjects, RefLeftObjects, RefRigthObjects
- ObjectList: ContentType, Filter, Description
- Pad: ConnectedObjects

More Controls from External Automation

- New Settings object
  - Access via Application.Settings property

- Control most of settings available in Options dialog
- Exclusion: Default Values -> Physical Net; Differential Pairs -> Custom Differential Pairs Builder

Authorization Codes

To use the latest releases, you must be on support contracts for these products as of May 2016. For more information about "Exact Access" authorization code formats, see the explanation on SupportNet at:

`http://www.mentor.com/supportnet/process_policy/exact_access.html`

You may download your site's existing authorization codes from SupportNet at:

`http://www.mentor.com/supportnet/licenses`

Supported Platforms

Overall Notes

- Specified patches below are minimum levels. Later versions of the patches are valid, supported configurations.
- Except as noted, all products are supported on all platforms.
- Processor and Memory requirements vary based on the mix of applications being used, the design complexity, and infrastructure requirements. Individual needs may vary from those published below.

Processor Note for Intel/AMD Processors

All Windows variants run on Intel or AMD x86 or x64 processors. In the past, the processor GHz speed determined the performance, but recent changes in the internal architecture of both Intel and AMD processors have made these comparisons difficult. Therefore, the following recommendations are being made for **all** Windows systems.

- Supported processors and systems are those manufactured since 2006 which conform to the

subsequent requirements.

- Intel Celeron processors are not recommended.
- Minimum requirement is a dual-core (or dual processor) system. A quad core is recommended for improved overall system performance. A hyperthreaded processor should be considered a single processor, not a dual processor.
- For best results, maximize processor speed and L1/L2/L3 processor cache memory.
- Typically, cost is the best indicator of performance, and extra investment in processor capability returns better system performance.

Microsoft Windows 7

Microsoft Windows 7 (32 and 64 bit versions), Professional Edition, Ultimate Edition, and Enterprise Edition are supported.

While there is no known issue with running Microsoft Windows 7 Starter Edition and Microsoft Windows 7 Home Premium Edition, the product has not been tested with these editions, and therefore is not supported.

Kernel Configuration: N/A

Processor: Dual-core Intel or AMD processor minimum. See Processor Note for Intel/AMD Processors above.

Memory: 8GB recommended.

Swap Space: 2x the amount of RAM.

Microsoft Windows 8.1

Microsoft Windows 8.1 Professional Edition, Ultimate Edition, and Enterprise Edition are supported.

Kernel Configuration: N/A

Processor: Dual-core Intel or AMD processor minimum. See Processor Note for Intel/AMD Processors above.

Memory: 8GB recommended.

Swap Space: 2x the amount of RAM

Microsoft Windows 10

Microsoft Windows 10 (32 and 64 bit versions), Enterprise Edition and Pro Edition are supported.

While there is no known issue with running Microsoft Windows 10.0 Home Edition or Educational Edition, the product has not been tested with these editions, and therefore is not supported.

> **Warning:** The new Microsoft Edge Browser delivered with Windows 10 is not supported with PADS Pro VX.1.2.

Kernel Configuration: N/A

Processor: Dual-core Intel or AMD processor minimum. See Processor Note for Intel/AMD Processors above.

Memory: 4GB Minimum, 8GB recommended

Swap Space: 2x the amount of RAM