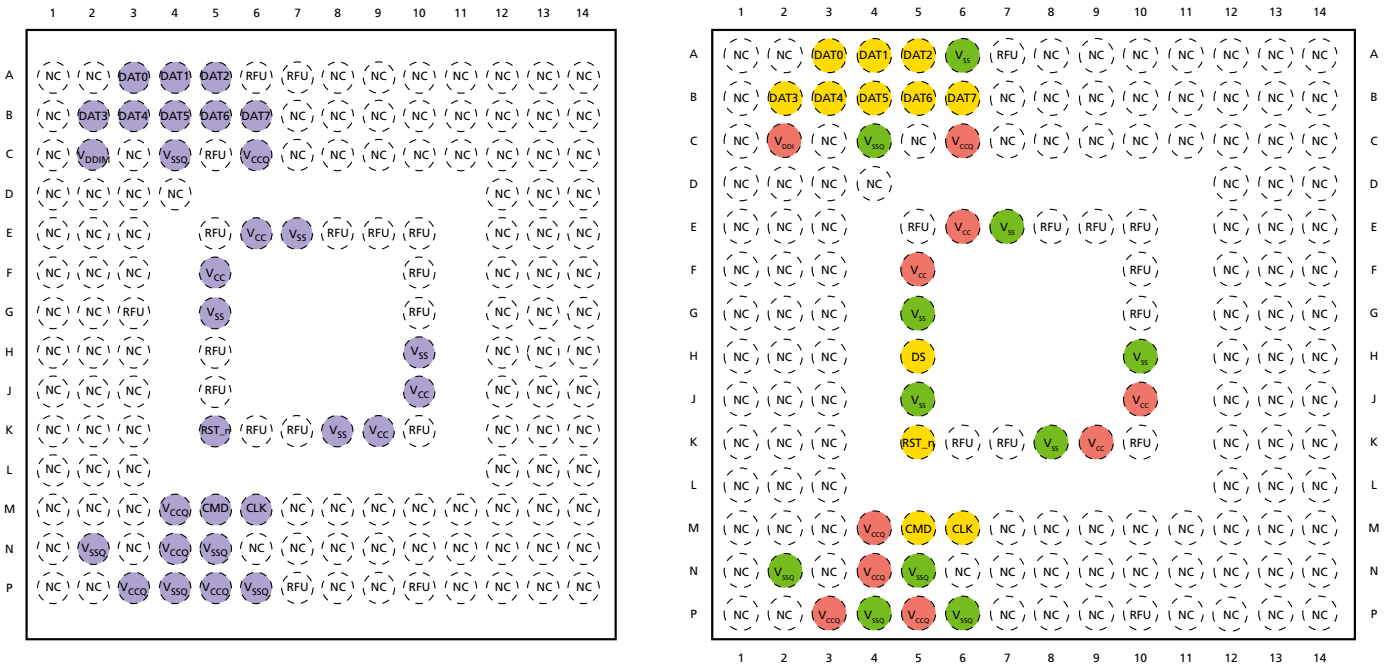
Technical Note

e·MMC PCB Design Guide

Introduction

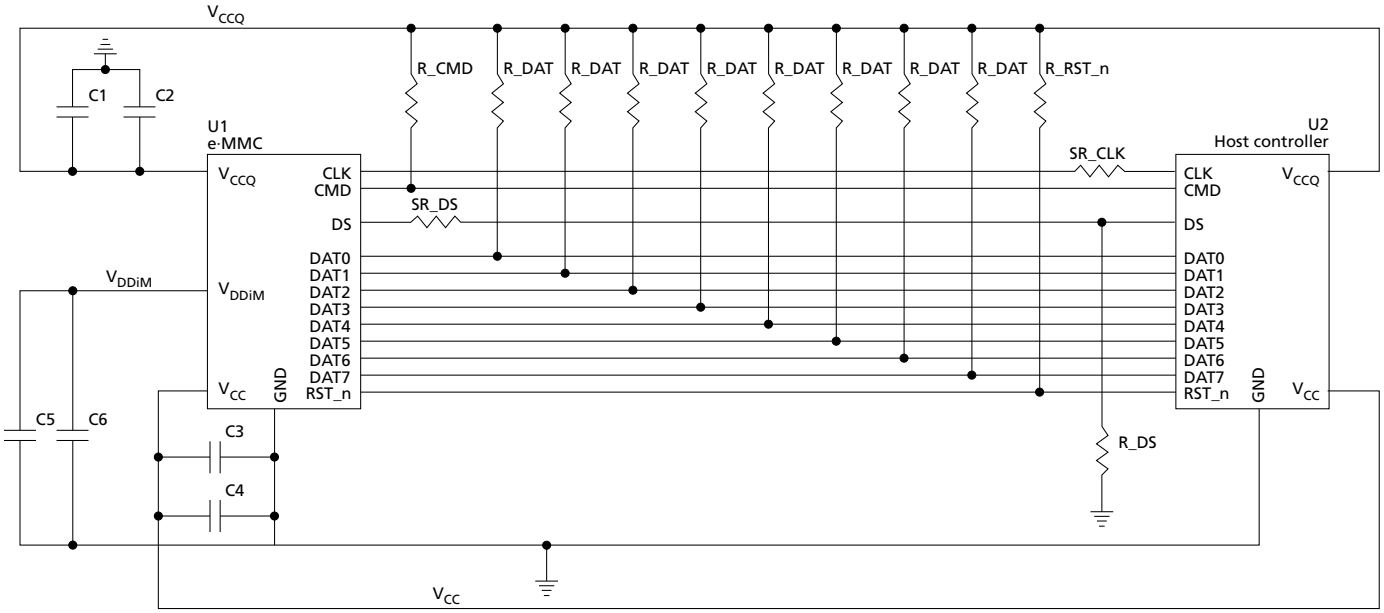
This document is intended as guide for PCB designers using Micron e·MMC devices and will discuss the primary issues affecting design and layout.

Figure 1: e·MMC 4.5 and 5.0 Package Compatibility



Ball	e·MMC 4.51	e·MMC 5.0	Comment
H5	RFU	DS	DS can be floating if HS400 is not used.
A6, J5	RFU	V_{SS}	V_{SS} can be floating if HS400 is not used.
C5	RFU	NC	Used for routing in this technical note only because it is NC internally, and JEDEC redefined it as NC for e·MMC 5.0.

Figure 2: Host to Micron e·MMC 5.0 Connection



Signal and Capacitor Placement

SR_CLK should be close to the host device, and SR_DS should be close to the e·MMC device. e·MMC signals can be fanned out through NC pins. No internal connection is present for NC pins. Micron recommends that e·MMC signals not be fanned out through RFU pins.

The recommended decoupling capacitors should be placed on the bottom side of the PCB across the BGA escape vias in order to minimize the connection inductance seen by the capacitor. The capacitor pad should be connected to the power and ground plane with a larger via to minimize the inductance in decoupling capacitors and allow for maximum current flow. The recommended capacitor values are shown in Table 1 (page 4). Wide, short traces between the via and capacitor pads should be used, or the via placed adjacent to the capacitor pad. Figure 4 (page 4) shows how to connect capacitor pads to the power and ground plane. Method 1 is not recommended, while the others are recommended.

Figure 3: Capacitor Placement and Signal PCB Layout

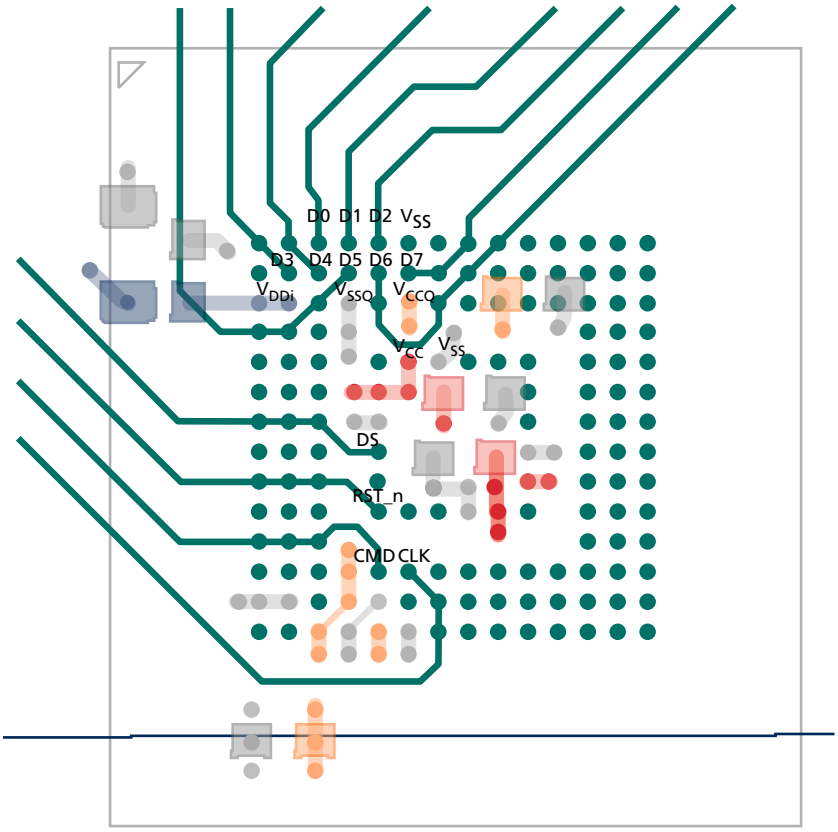
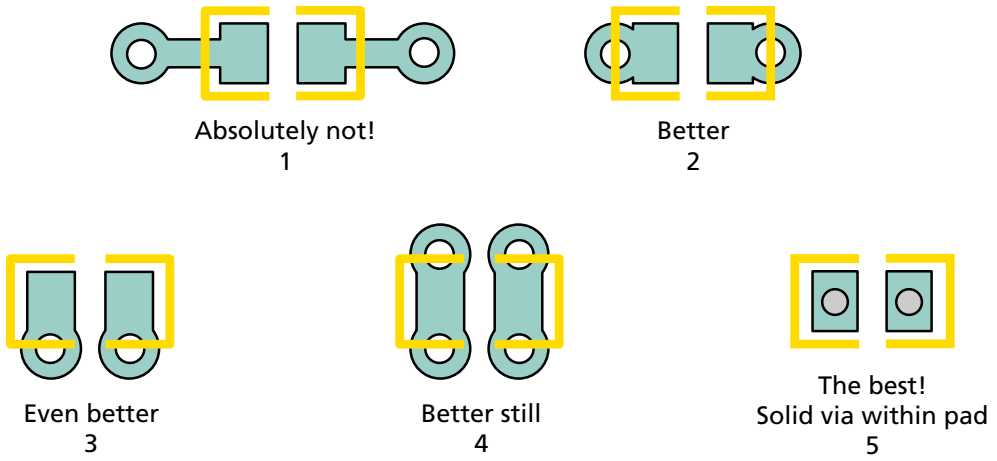


Table 1: Component Parameter Values

Parameter	Symbol	Min	Max	Recommended	Unit	Comments
Pull-up resistance for CMD	R_CMD	4.7	50	10	KΩ	To prevent bus floating
Pull-up resistance for DAT[7:0]	R_DAT	10	50	50	KΩ	To prevent bus floating
Pull-up resistance for RST_n	R_RST_n	4.7	50	50	KΩ	It is not necessary to put pull-up resistance on RST_n line if the host does not use H/W reset.
Pull-down resistance for R_DS	R_DS	4.7	50	50	KΩ	
Impedance of CLK/CMD/DS/DAT[7:0]	–	45	55	50	Ω	Impedance match
Serial resistance on CLK line	SR_CLK	0	47	22	Ω	To stabilize CLK signal
Serial resistance on DS line	SR_DS	0	47	22	Ω	To stabilize DS signal
V_{CCQ} capacitor value	C1, C2	2.2 + 0.1	4.7 + 0.22	2.2 + 0.1	µF	Decoupling capacitor should be connected with V_{CCQ} and V_{SSQ} as closely as possible.
V_{CC} capacitor value (≤8GB)	C3, C4	2.2 + 0.1	4.7 + 0.22	2.2 + 0.1	µF	Decoupling capacitor should be connected to V_{CC} and V_{SS} as closely as possible.
V_{CC} capacitor value (>8GB)				4.7 + 0.22	µF	
V_{DDIM} capacitor value	C5, C6	1 + 0.1	4.7 + 0.1	1 + 0.1	µF	Decoupling capacitor should be connected to V_{DDIM} and V_{SSQ} as closely as possible.

Figure 4: Connecting Capacitor Pads

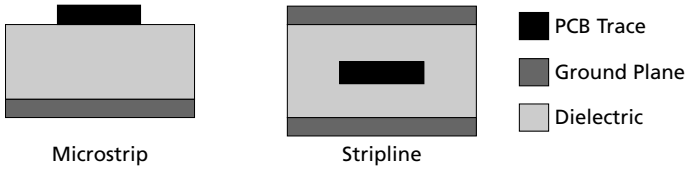


PCB Topology and Layout

The PCB board must have at least four layers.

CLK, CMD, DQ and DS signals should be treated as transmission lines with controlled impedance from 45Ω to 55Ω. The skew of propagation time of these signals should be minimized and the PCB trace length difference kept within ±50 mil. The following figure shows two commonly used PCB transmission line topologies.

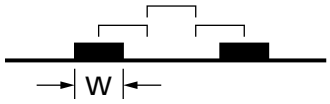
Figure 5: Transmission Line Topologies



The e·MMC signals' trace length should be as short as possible; it is best kept to less than 2000 mil.

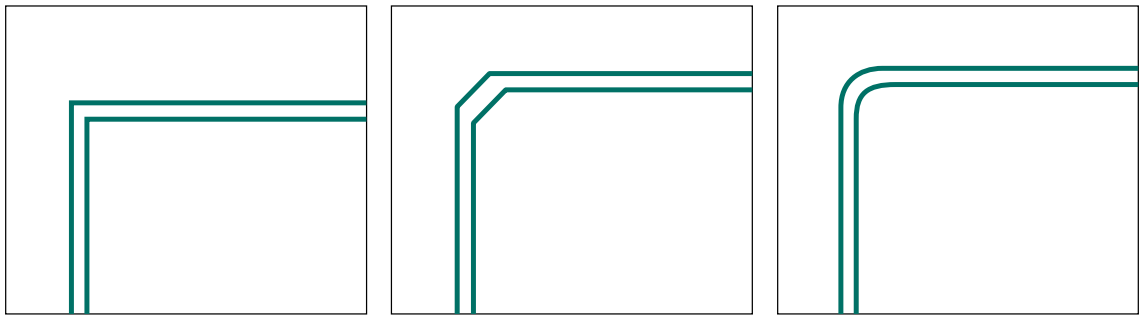
The transmission line should be designed so that the conductor is as close to the ground plane as possible. This technique will couple the transmission line tightly to the ground plane and help decouple it from adjacent signals. It's best to widen spacing between signal lines as much as routing restrictions will allow, trying not to bring traces closer than three times the trace width.

Figure 6: Trace Width Example



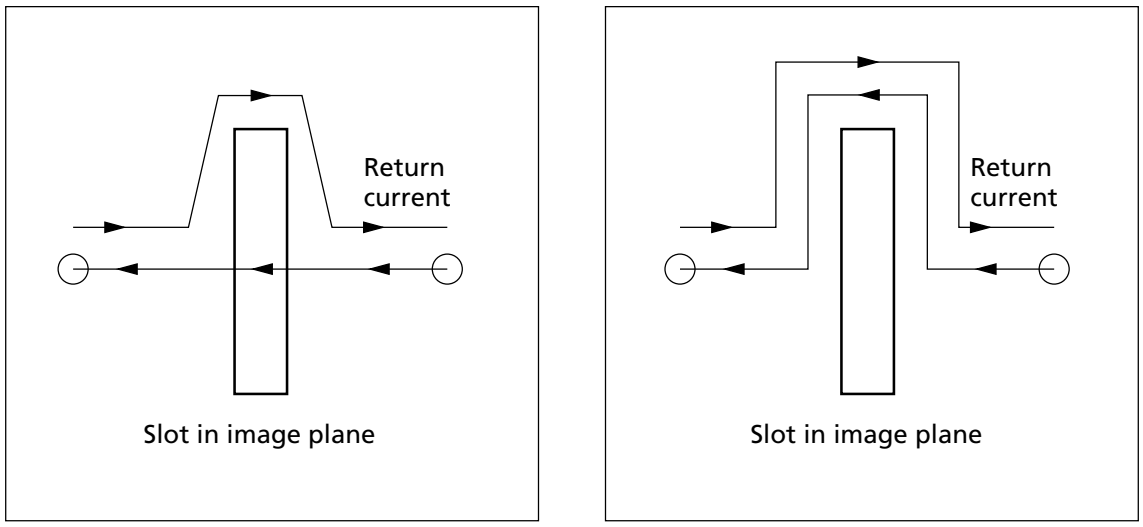
Arc-shaped traces should be used instead of right-angle bends.

Figure 7: Trace Shape



There should be NO breaks or voids in the ground plane under or over the high speed signals.

Figure 8: Avoiding Breaks and Voids

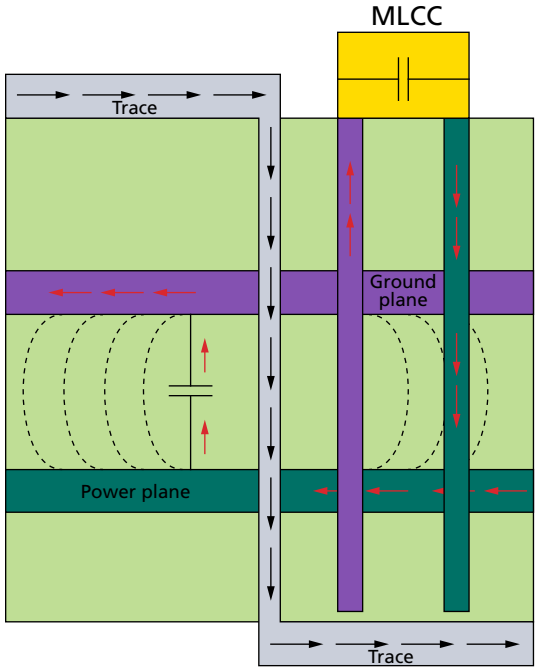


Bad Better

The best signaling is obtained when a constant reference plane is maintained. If a reference plane transition cannot be avoided, we recommend using the following techniques.

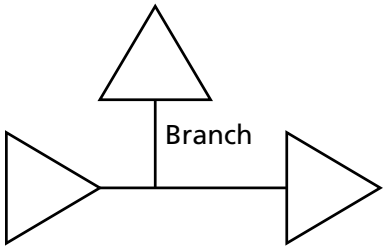
- If the signal reference plane changes from ground plane to power plane, adding capacitors near the via transition site will help support a good return path.
- If the signal reference plane changes from ground plane to another ground plane, ground vias should surround all high-speed signals (two ground vias per clock via; one ground via per high speed signal via).

Figure 9: Additional Capacitor for Return Current



Stubs should be kept short to avoid reflections. Stub propagation delay should be kept to <20% of the rise time of the signal.

Figure 10: Typical Stub Case



Revision History

Rev. B – 01/15

- Updated the Host to Micron e·MMC 5.0 Connection figure

Rev. A – 08/14

- Initial release

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-4000
www.micron.com/products/support Sales inquiries: 800-932-4992